# SONY CX20201/CX20202

## 10-Bit, 100 MHz D/A Converters

### Description

The CX20201/CX20202 are ICs which have been developed for 10-bit high-speed D/A converters. They are suitable for digital VTR, digital measuring instruments, graphic displays, high definition video systems, which require high precision, high resolution and ultra high-speed signal processing.

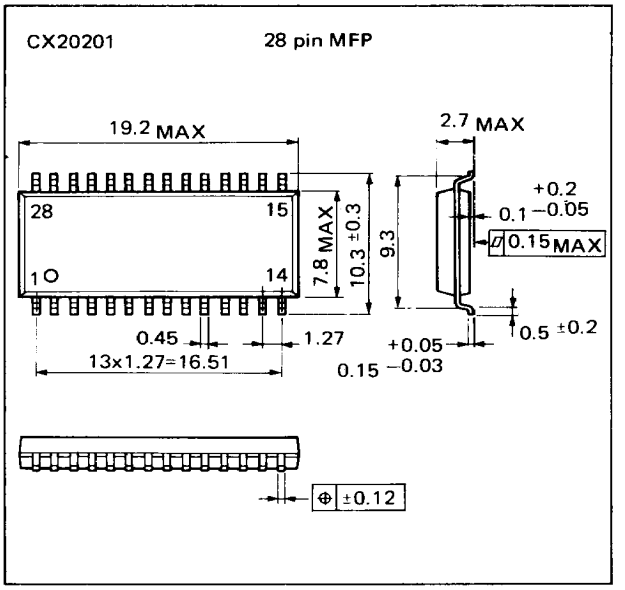
### Features

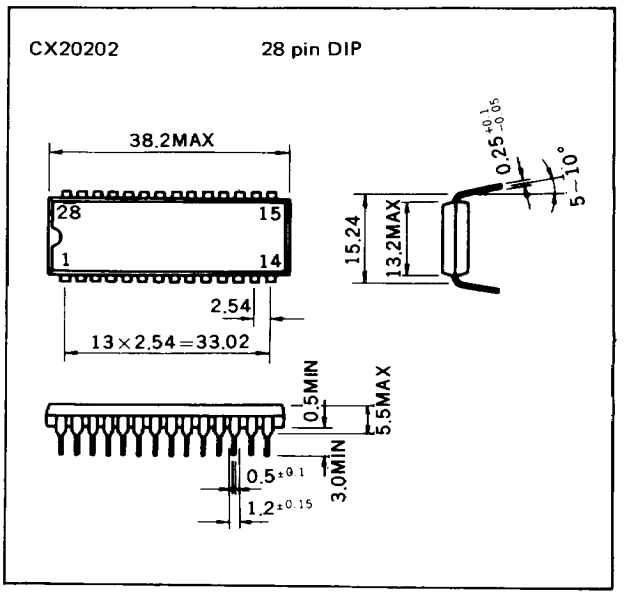
- High resolution: 10 bits
- High-speed: Maximum conversion rate of 100MSPS
- Low-power consumption
- Operates with a single power supply of −5V
- Low glitches
- ECL compatible input
- Small number of external parts
- Enables to invert digital input code
- Multiplying function

### Absolute Maximum Ratings (Ta=25°C)

| | | | | |
|---|---|---|---|---|
| • Power supply voltage | $V_{EE}$ | | −7 | V |
| • Data input voltage | $V_I$ | | VEE to +0.3 | V |
| • Clock input voltage | $V_{CLK}$, $V_{\overline{CLK}}$ | | $V_{EE}$ to +0.3 | V |
| • Invert input voltage | $V_{INV}$ | | $V_{EE}$ to +0.3 | V |
| • Bias input voltage | $V_{BIAS}$ | | $V_{EE}$ to +0.3 | V |
| • Operating temperature | Topr | | −20 to +75 | °C |
| • Storage temperature | Tstg | | −55 to +150 | °C |
| • Allowable power dissipation | | | | |
| | $P_D$ | CX20201 | 870 | mW |
| | | CX20202 | 1480 | mW |

Package Outline Unit: mm




### Recommended Operating Conditions

| | | | |
|---|---|---|---|
| • Power supply voltage | $V_{EE}$ | −5.0 ± 0.25 | V |
| • Data input voltage | $V_{IH}$ | −0.89 ± 0.15 | V |
| | $V_{IL}$ | −1.75 ± 0.15 | V |
| • Clock input voltage | $V_{CLKH}$, $V_{\overline{CLKH}}$ | −0.89 ± 0.15 | V |
| | $V_{CLKL}$, $V_{\overline{CLKL}}$ | −1.75 ± 0.15 | V |
| • Bias voltage | $V_{BIAS}$ | $V_{EE}$ + 0.62 to $V_{EE}$ + 1.02 | V |

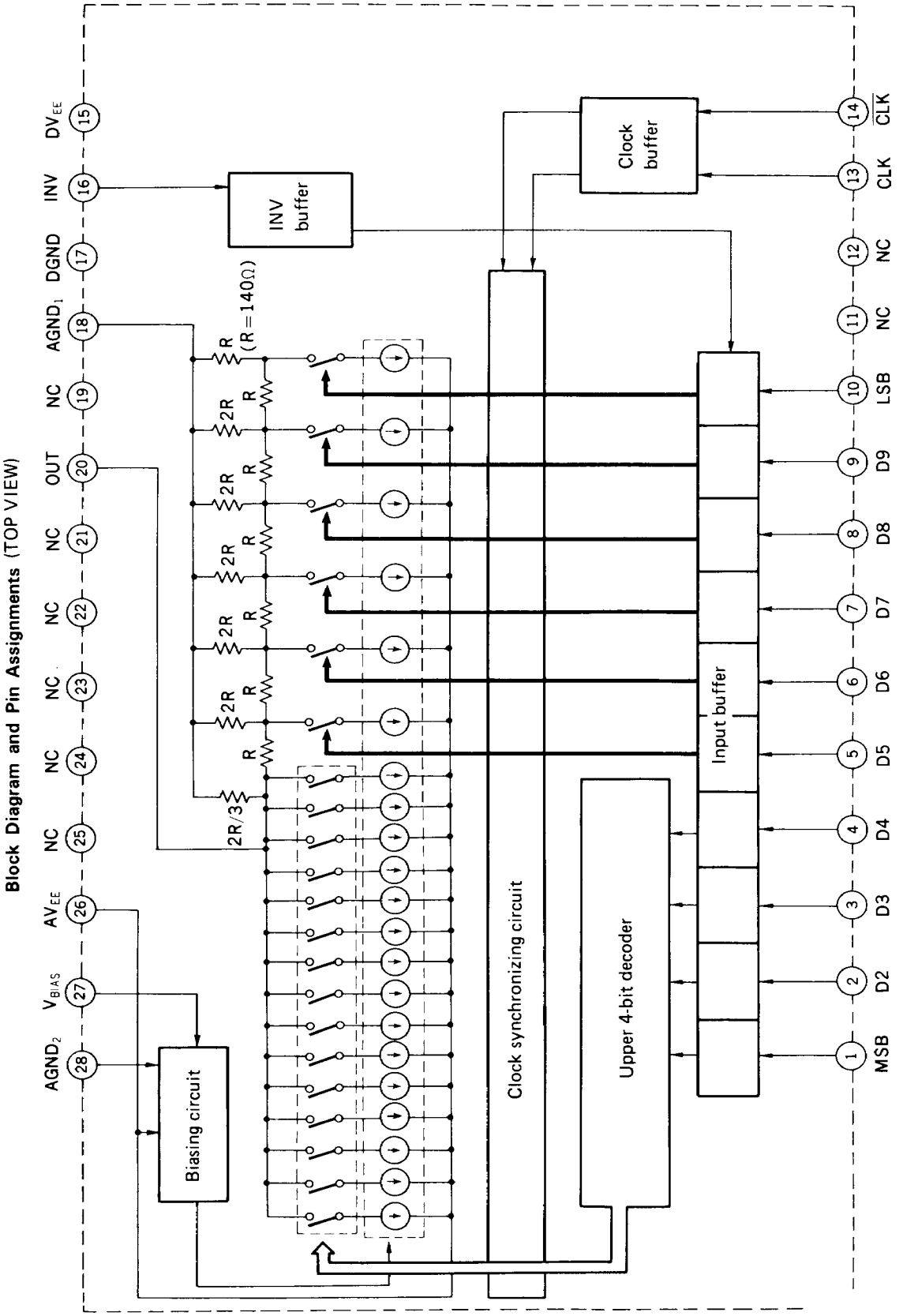

Block Diagram and Pin Assignments (TOP VIEW)
DVEE 15
INV 16
DGND 17
AGND1 18
NC 19
OUT 20
NC 21
NC 22
NC 23
NC 24
NC 25
AVEE 26
VBIAS 27
AGND2 28
CLK 14
CLK 13
NC 12
NC 11
LSB 10
D9 9
D8 8
D7 7
D6 6
D5 5
D4 4
D3 3
D2 2
MSB 1
INV buffer
Clock buffer
R (R=140Ω)
2R
R
2R/3
Biasing circuit
Clock synchronizing circuit
Upper 4-bit decoder
Input buffer

Fig. 1

**Pin Description**

① MSB
② D2
③ D3
④ D4
⑤ D5
⑥ D6
⑦ D7
⑧ D8
⑨ D9
⑩ LSB

10-bit digital data input pin.
If the device is used as n-bit ($n \leqq 9$) D/A converter, pin 1 to pin n are to be used normally, and the rest pins (n+1) to 10 opened or connected to $V_{EE}$.

⑪ ⑫ Non-Connection

⑬ CLK : Digital clock input is to be applied.
⑭ $\overline{CLK}$ : Digital clock bar input is to be applied.
⑮ D.$V_{EE}$ : Power supply pin of digital circuitry.
⑯ INV : Code inverse input pin which inverts the relation between the binary code of digital data and D/A output voltage level. See "Note on use".
⑰ D.GND : Ground pin of digital circuitry.
⑱ A.$GND_1$ : Ground pin connected directly to R-2R output resistance circuit network within the IC.
⑲ Non-connectioln
⑳ OUT : D/A output
㉑ ㉒ ㉓ ㉔ ㉕ : Non-connection
㉖ A.$V_{EE}$ : Power supply pin of analog circuitry.
㉗ $V_{BIAS}$ : Bias pin which controls D/A output voltage range, and to which a proper voltage should be applied externally.
㉘ A.$GND_2$ : Ground pin of the analog circuitry except R-2R output resistance circuit network.

**Electrical Characteristics** (Ta = 25°C, $AV_{EE}$ = $DV_{EE}$ = −5.0V, AGND = DGND = 0V) See Fig. 2

| Item | | Symbol | Min. | Typ. | Max. | Unit | Measuring point |
|---|---|---|---|---|---|---|---|
| Supply current | CX20201 | $I_{EE}$ | 60 | 75 | 90 | mA | I1 |
| | CX20202 | | 65 | 82 | 99 | | |
| Data input current (upper 4 bits) | (H level) | $I_{IH(U)}$ | 0.5 | 1.3 | 3.0 | μA | I2 |
| | (L level) | $I_{IL(U)}$ | 0.5 | 1.3 | 3.0 | μA | |
| Data input current (lower 6 bits) | (H level) | $I_{IH(L)}$ | 0.25 | 0.65 | 1.5 | μA | |
| | (L level) | $I_{IL(L)}$ | 0.25 | 0.65 | 1.5 | μA | |
| Clock input current (H level) | CX20201 | $I_{CLKH}$ | 7 | 21 | 52 | μA | I3 |
| | CX20202 | | 7 | 23 | 54 | | |
| Clock bar input current (H level) | CX20201 | $I_{\overline{CLK}H}$ | 7 | 21 | 52 | μA | I4 |
| | CX20202 | | 7 | 23 | 54 | | |
| Invert input current (H level) | | $I_{INVH}$ | 0.3 | 1.0 | 2.4 | μA | I5 |
| Bias input current | | $I_{BIAS}$ | −1.0 | −0.38 | −0.10 | μA | I6 |
| Output resistance | CX20201 | $R_O$ | 54 | 64 | 74 | Ω | V1 |
| | CX20202 | | 52 | 62 | 72 | | |

| | | | | | |
|---|---|---|---|---|---|
| Resolution | RSL | | 10 | | Bit |
| Differential linearity error | DLE | −1.0 | | +1.0 | LSB |
| Maximum conversion rate | $f_{C\,MAX}$ | 100 | | | MSPS |

**Electrical Characteristics Measuring Circuit Diagram**

**Fig. 2 Supply Current, Input Current and Output Resistance Measuring Circuit**

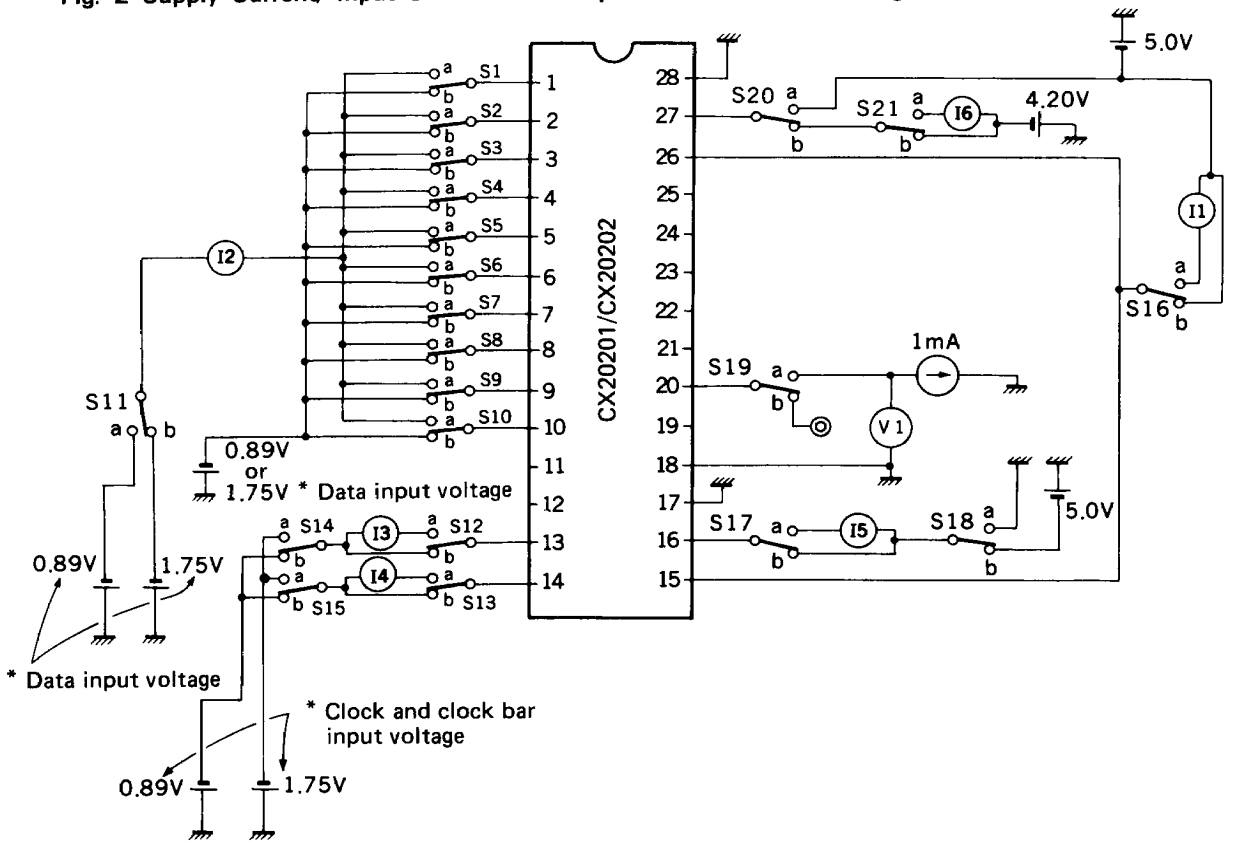
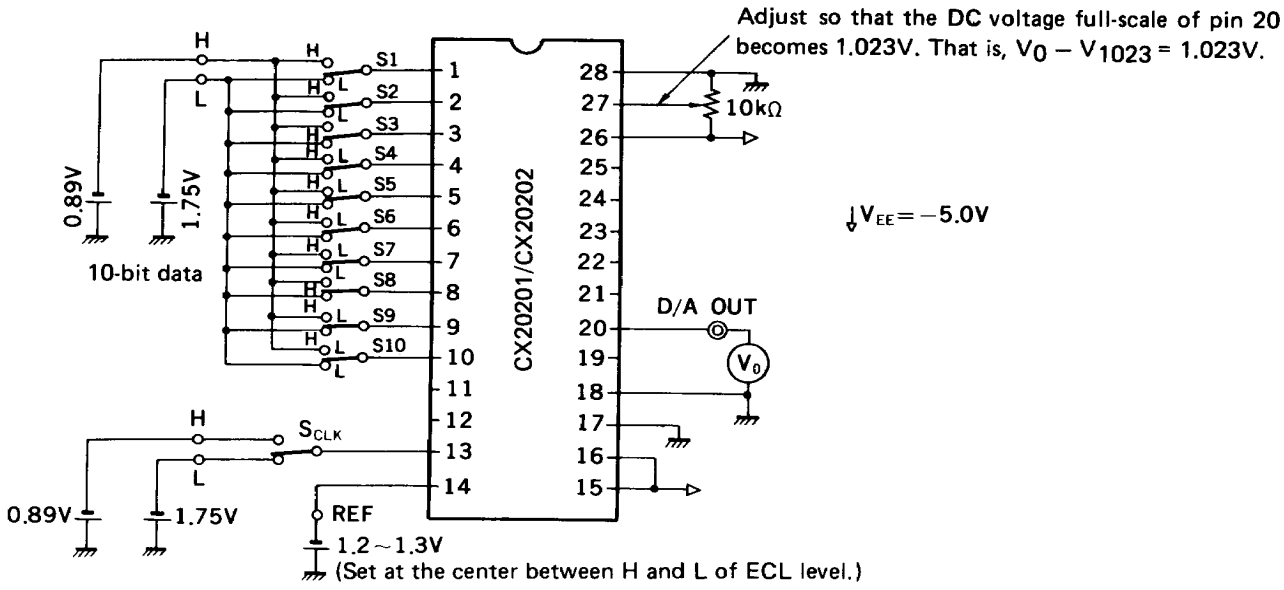


**Fig. 3 Differential Linearity Error Measuring Circuit**




**[Meausuring Circuit Condition of Fig. 3]** (H="1" level; L="0" level)

| Operating order | Switching condition | | | | | | | | | | | Measuring point | Explanation of measuring method |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | $S_{CLK}$ | | |
| 1 | H | H | H | H | H | H | H | H | H | H | L | | |
| 2 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | H | | |
| 3 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | L | $V_0$ | Measuring DC voltage. Measured value $V_0 \equiv$ (Unit: mV) |
| 4 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | L | ↓ | | |
| 5 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | H | | |
| 6 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | L | $V_0$ | Measuring DC voltage. Measured value $V_1 \equiv$ (Unit: mV) |
| 7 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | L | H | ↓ | | |
| 8 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | H | | |
| 9 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | L | $V_0$ | Measuring DC voltage. Measured value $V_2 \equiv$ (Unit: mV) |
| 10 | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | L | ↓ | | |

Proceed the measurement reducing the input data (voltage of pin 1 to pin 10) in regular sequence of binary notation, and continue until the final data becomes LLL . . . L

$\Delta V_{0\text{-}1} \equiv V_0 - V_1$ (Unit: mV)

$\Delta V_{1\text{-}2} \equiv V_1 - V_2$ (Unit: mV)

⋮

$\Delta V_{1022\text{-}1023} \equiv V_{1022} = V_{1023}$ (Unit: mV)

are to be calculated. (See Fig. 4)

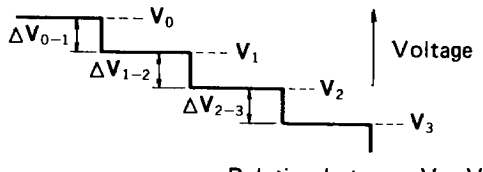


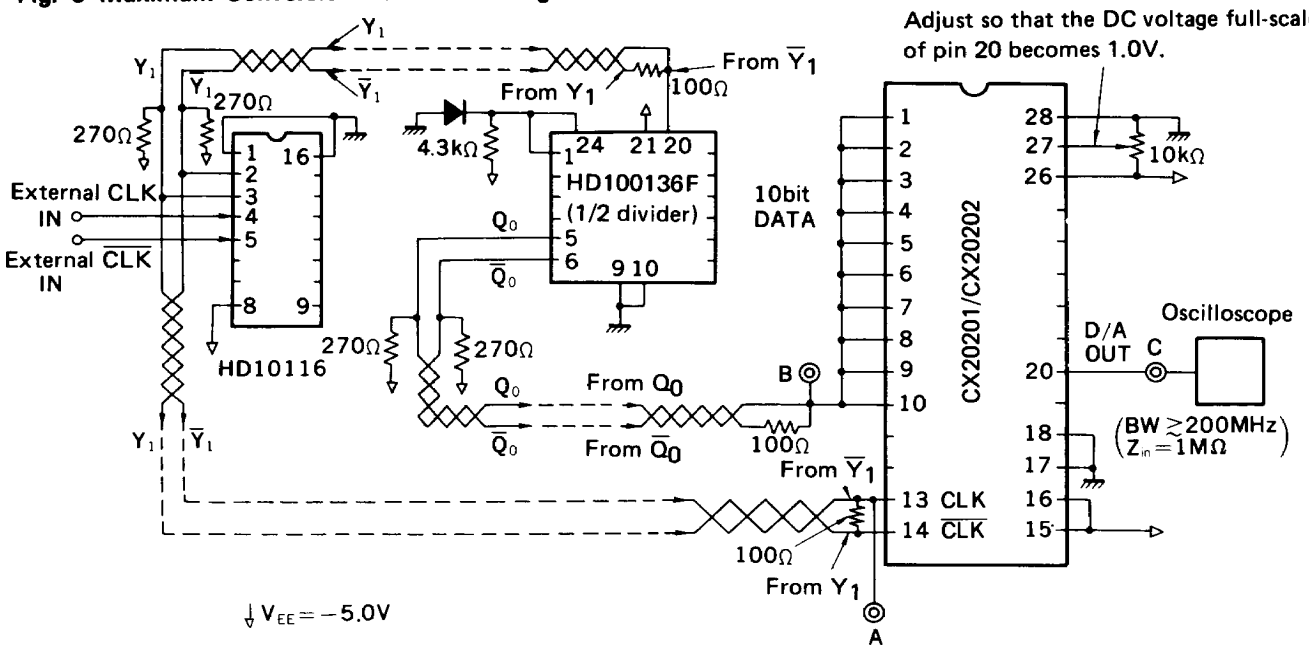

**Fig. 4** Relation between $V_0, V_1, \ldots$ and $\Delta V_{0-1}, \Delta V_{1-2}, \ldots$

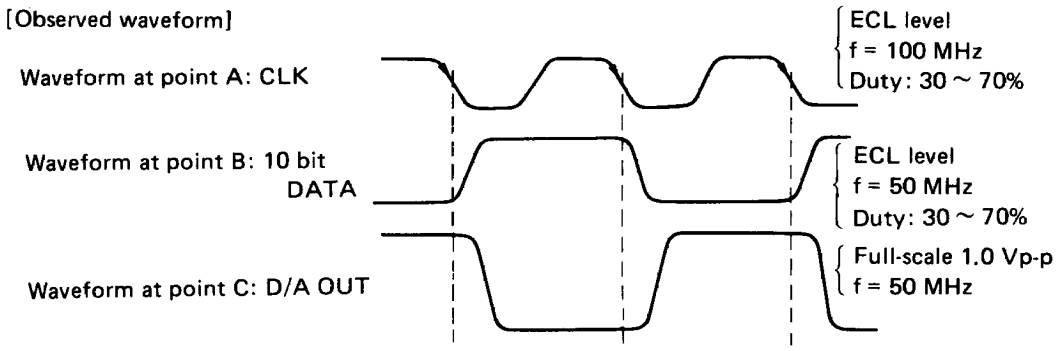
With $\Delta V_{0\text{-}1}, \Delta V_{1\text{-}2}, \ldots,$

$$\varepsilon_{i\text{-}j} \equiv \frac{\Delta V_{i\text{-}j} - 1}{1} \quad (i=0,1,\ldots,1022;\ j=1,2,\ldots,1023) \text{ (Unit: LSB)}$$

are to be obtained. Each of 1023 pieces of $\varepsilon_{i\text{-}j}$ is differential linearity error, respectively.

**Fig. 5 Maximum Conversion Rate Measuring Circuit**




**[Measuring Method of Maximum Conversion Rate]**

The external CLK IN and $\overline{CLK}$ IN should satisfy the following conditions.

- ECL level
- $f_{CLK} \fallingdotseq$ 100 MHz
- Duty $\simeq$ 50%

At point C, a rectangular waveform (1.0 Vp-p, f=50 MHz) is to be obtained.

**Circuit Design Data**

( Ta=25°C, however, * mark is Ta=−20 to +75°C
AVEE=DVEE=−5.0V, AGND=DGND=0V )

| Item | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Integral linearity error | ILE | −0.4 | | +0.4 | % of F.S. | |
| Output voltage full-scale | $V_{O(FS)}$ | 0.890 | 1.000 | 1.110 | Vp-p | Voltage of pin 27 is −4.20V. The load to be connected to pin 20 is $Z_L$>10 kΩ. |
| Output voltage zero offset | $V_{O(OS)}$ | −15 | −4 | −1 | mV | |
| Output voltage full-scale temperature coefficient* | $T_{CF(FS)}$ | 0 | 150 | 500 | ppm/°C | |
| Output voltage zero offset temperature coefficient* | $T_{CF(OS)}$ | 6 | 16 | 22 | μV/°C | |
| Output voltage full-scale dynamic range | DR | −3.3 | 0 | +3.3 | dB | 0dB denotes 1.000V of full-scale output voltage. (This full-scale voltage is set by adjusting the voltage of pin 27.) The load to be connected to pin 20 is $Z_L$>10 kΩ. |
| Glitch energy | GE | | 15 | | pV-sec | See Glitch energy measuring method. |
| Set-up time | ts | 7.0 | | | ns | See measuring circuit and observed waveform diagrams (Fig. 9). Loading : $R_L$ $C_L$<0.1 nS. ($R_L$ : pure resistance, $C_L$ : capacitive load, They are connected to pin 20.) |
| Hold time | th | 1.0 | | | ns | |
| Propagation delay | tpd | | 2.8 | | ns | |
| Rise time | tr | | 1.5 | | ns | |
| Fall time | tf | | 1.5 | | ns | |
| Settling time | tset | | 4.7 | | ns | See Explanation of settling time. |
| Multiplying bandwidth | BWMUL | | | 10 | MHz | The frequency in which the gain of D/A output becomes −3 dB. See Fig. 11. |

**[Measuring Method for Circuit Design Data]**

1. **Integral linearity error**

In differential linearity error measuring circuit (Fig. 3).

$\Delta V_{0\text{-}1} \equiv V_0 - V_1$ (Unit: mV)
$\Delta V_{0\text{-}2} \equiv V_0 - V_2$ (Unit: mV)
$\Delta V_{0\text{-}3} \equiv V_0 - V_3$ (Unit: mV)
.
.
.
$\Delta V_{0\text{-}1023} \equiv V_0 - V_{1023}$ (Unit: mV)

and

$$\varepsilon_{absi} \equiv \frac{\Delta V_{0\text{-}i} - i}{1023} \times 100 \quad (i=1, 2, 3, \ldots, 1023) \text{ (Unit: \%)}$$

Each of 1023 pieces of $\varepsilon_{absi}$ is integral linearity error.

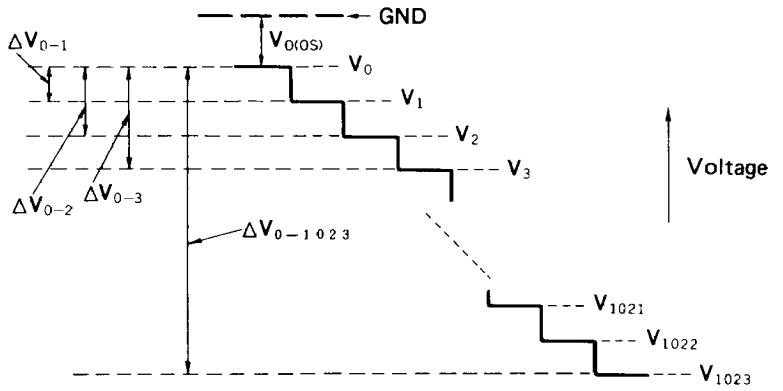



**Fig. 6** Relation between $V_0$, $V_1$ . . . and $\Delta V_{0-1}$, $\Delta V_{0-2}$, . . .

2. **Output voltage zero offset**

In Fig. 6, the potential difference between GND level and Vo is defined as zero offset, $V_{O(OS)}$.

### 3. Glitch energy

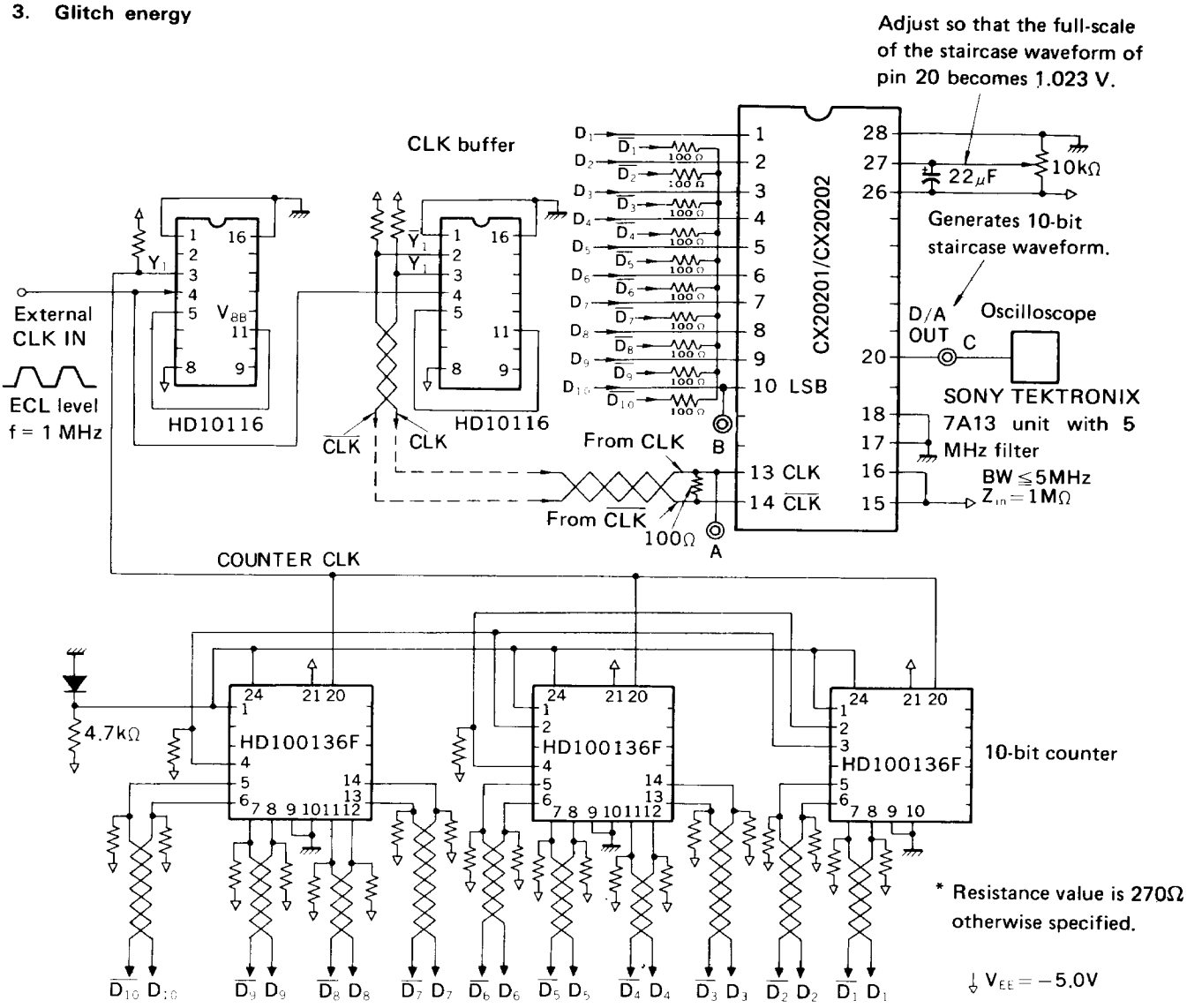



Fig. 7(a) Glitch energy measuring circuit

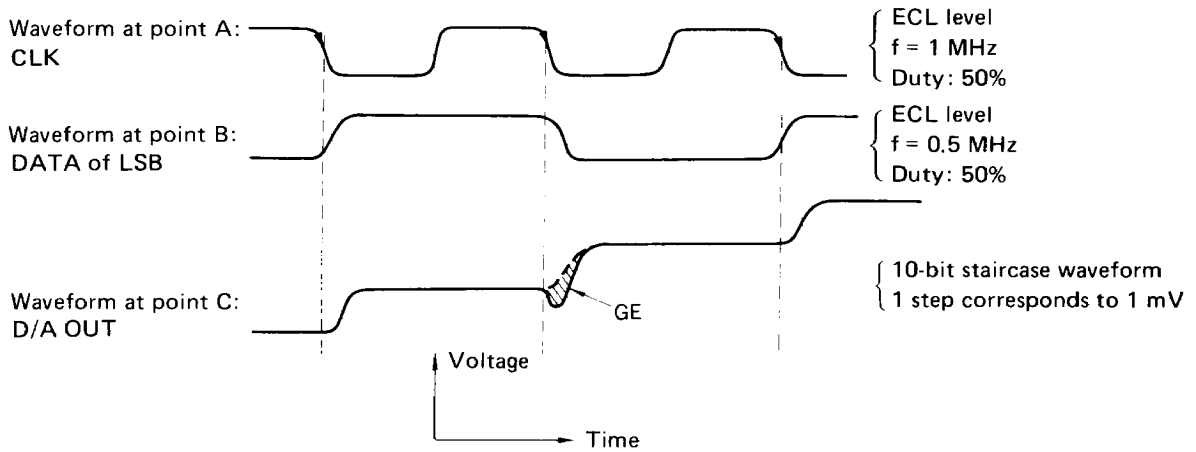



Fig. 7(b) Observed waveforms of the above-mentioned measuring circuit

**[Measuring Method of Glitch Energy]**

The signal to be fed to External CLK IN terminal should satisfy the following conditions.

- ECL level
- $f_{CLK}$ = 1 MHz
- Duty = 50%

In this case, the observed waveforms at points A, B and C become as shown in Fig. 7(b), respectively.

In Fig. 7(b), GE is the integrated value of the difference between an ideal voltage waveform and the overshoot which is generated actually. It is marked with oblique lines.

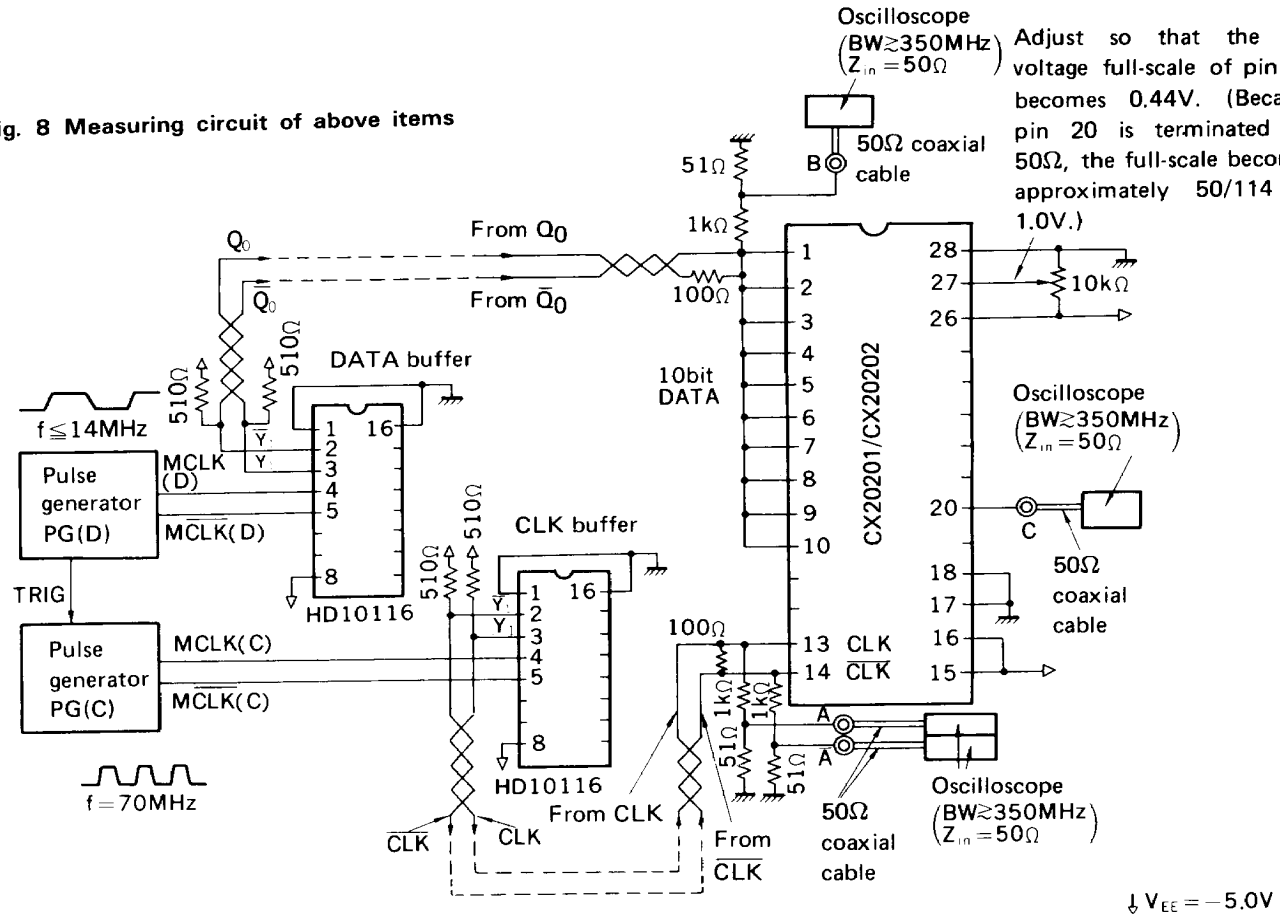
It is measured at the transient points shown in the following table.

| | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_8$ | $D_9$ | $D_{10}$ | | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_8$ | $D_9$ | $D_{10}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | L | L | L | L | H | H | H | H | H | H | → | L | L | L | H | L | L | L | L | L | L |
| 2 | L | L | L | H | H | H | H | H | H | H | → | L | L | H | L | L | L | L | L | L | L |
| 3 | L | L | H | L | H | H | H | H | H | H | → | L | L | H | H | L | L | L | L | L | L |
| 4 | L | L | H | H | H | H | H | H | H | H | → | L | H | L | L | L | L | L | L | L | L |
| 5 | L | H | L | L | H | H | H | H | H | H | → | L | H | L | H | L | L | L | L | L | L |
| 6 | L | H | L | H | H | H | H | H | H | H | → | L | H | H | L | L | L | L | L | L | L |
| 7 | L | H | H | L | H | H | H | H | H | H | → | L | H | H | H | L | L | L | L | L | L |
| 8 | L | H | H | H | H | H | H | H | H | H | → | H | L | L | L | L | L | L | L | L | L |
| 9 | H | L | L | L | H | H | H | H | H | H | → | H | L | L | H | L | L | L | L | L | L |
| 10 | H | L | L | H | H | H | H | H | H | H | → | H | L | H | L | L | L | L | L | L | L |
| 11 | H | L | H | L | H | H | H | H | H | H | → | H | L | H | H | L | L | L | L | L | L |
| 12 | H | L | H | H | H | H | H | H | H | H | → | H | H | L | L | L | L | L | L | L | L |
| 13 | H | H | L | L | H | H | H | H | H | H | → | H | H | L | H | L | L | L | L | L | L |
| 14 | H | H | L | H | H | H | H | H | H | H | → | H | H | H | L | L | L | L | L | L | L |
| 15 | H | H | H | L | H | H | H | H | H | H | → | H | H | H | H | L | L | L | L | L | L |

(H and L mean the high and low of ECL levels.)

4. { **Set-up time**
   **Hold time**
   **Propagation delay**
   **Rise time**
   **Fall time**

**Fig. 8 Measuring circuit of above items**




**[Measuring Method of Above Items]**

The signals which are generated by pulse generators PG(C) and PG(D) should satisfy the following conditions.

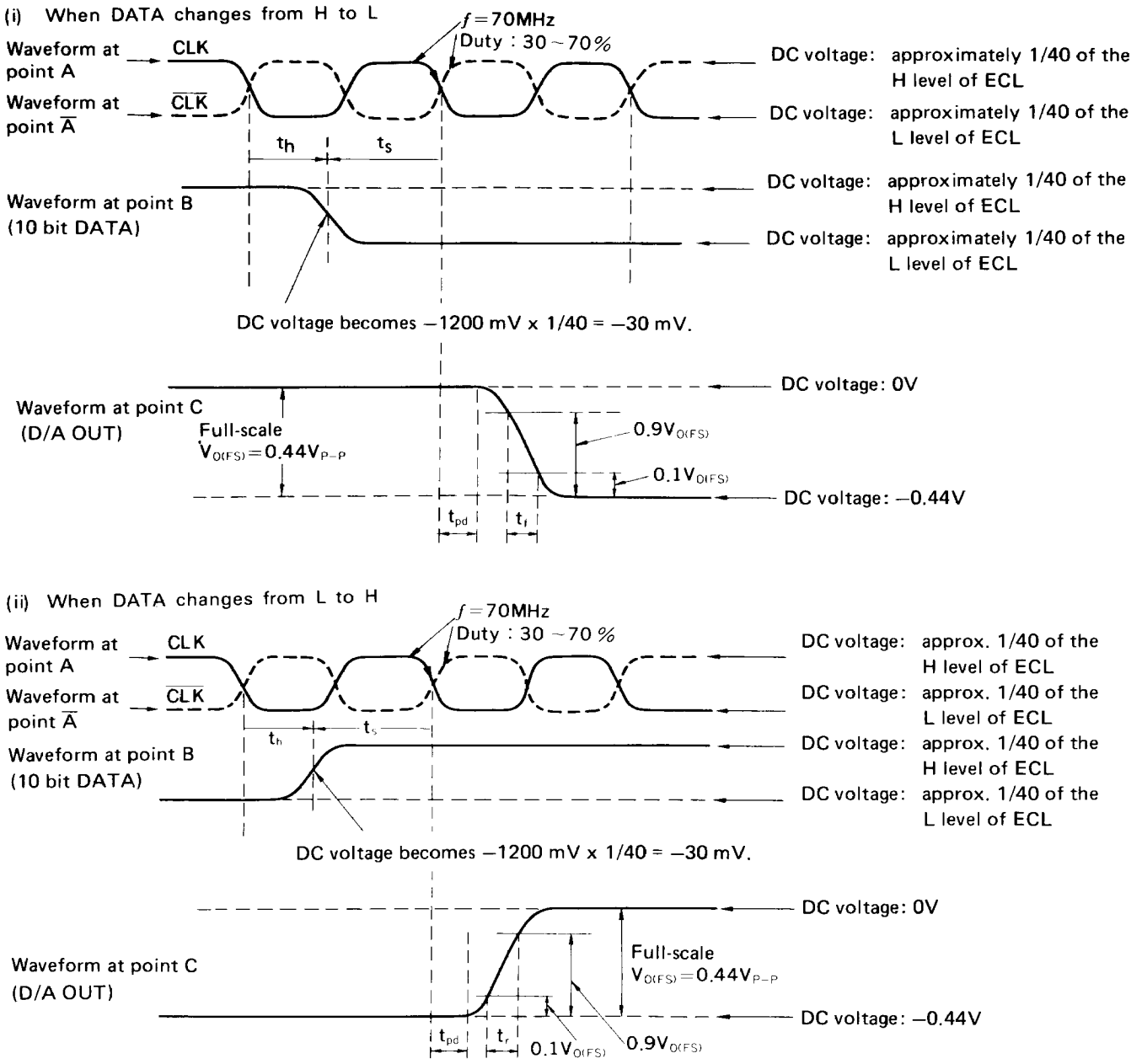
① PG(C)
- ECL level
- f=70 MHz
- Duty ≃ 50%

② PG(D)
- ECL level
- f≦14 MHz
- Duty: 25 ~ 75%

By changing the delay time of the mutual pulses generated from PG(C) and PG(D) , control phase relations among those of observed waveforms at points A, $\overline{A}$ and B. And then, obtain the range of $t_s$ and $t_h$ where D/A output changes at normal timing.

Desired waveforms to be observed at points, A, $\overline{A}$, B and C, are sketched as follows:

**Fig. 9 Observed waveforms**




In addition, measure $t_{pd}$ (The interval between the switchover points of CLK and $\overline{CLK}$, and the time when D/A OUT waveform begins to change by 1 LSB.), and also, rise time $t_r$ and fall time $t_f$ (as shown in Fig. 9).

**5. Settling time**

The settling time described in Circuit Design Data is the value calculated with rise time and fall time.

The calculation method is as shown below.

In the D/A output waveform shown in Fig. 10,

$$V = Vo(1 - e^{-\frac{t}{\tau}})$$

The dotted line is the tangential line at point P. Settling time of 10-bit ($t_{set}$) can be obtained by setting V=0.999Vo in the above equation. Thus,

$t_{set} = 6.91\tau \ldots$ ①

Rise time $t_r$ is the interval in which V varies from 0.1Vo to 0.9Vo.

When V=0.1Vo, $t_{10} = -\tau \ln 0.9$

When V=0.9Vo, $t_{90} = -\tau \ln 0.1$

$t_r = t_{90} - t_{10} = \tau \ln 9$

$\therefore\ t_r = 2.20\tau \ldots$ ②

From eqs. ① and ②

$t_{set} = 3.14 t_r \ldots$ ③

Thus, $t_{set}$ can be calculated.

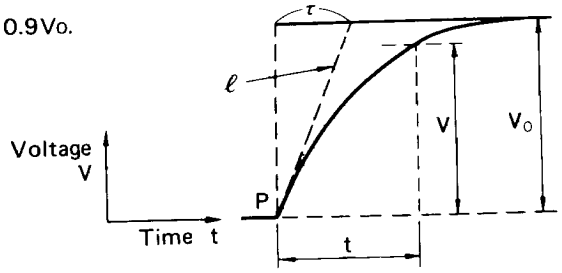
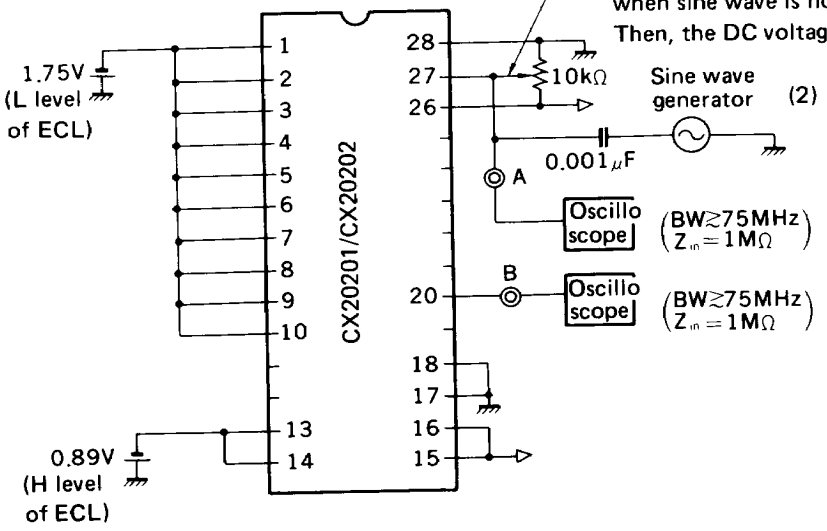



**Fig. 10 D/A output waveform**

**6. Multiplying bandwidth**

**Fig. 11 Multiplying bandwidth measuring circuit**




(1) Adjust so that DC voltage at point B becomes −1.00V when sine wave is not fed.
Then, the DC voltage at point A is defined as $V_{BIAS}$.

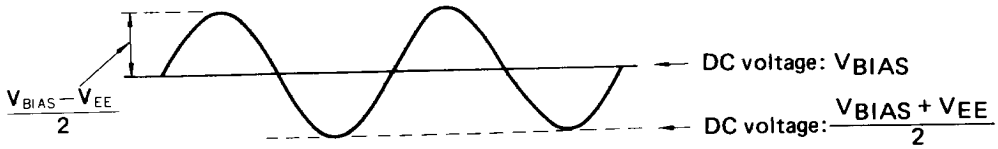
(2) Apply sine wave to pin 27, and adjust the amplitude so that the amplitude of waveform at point A becomes $\frac{V_{BIAS} - V_{EE}}{2}$.

$V_{EE} = -5.0V$

**[Observed waveform]**

Frequency $f_{MUL}$

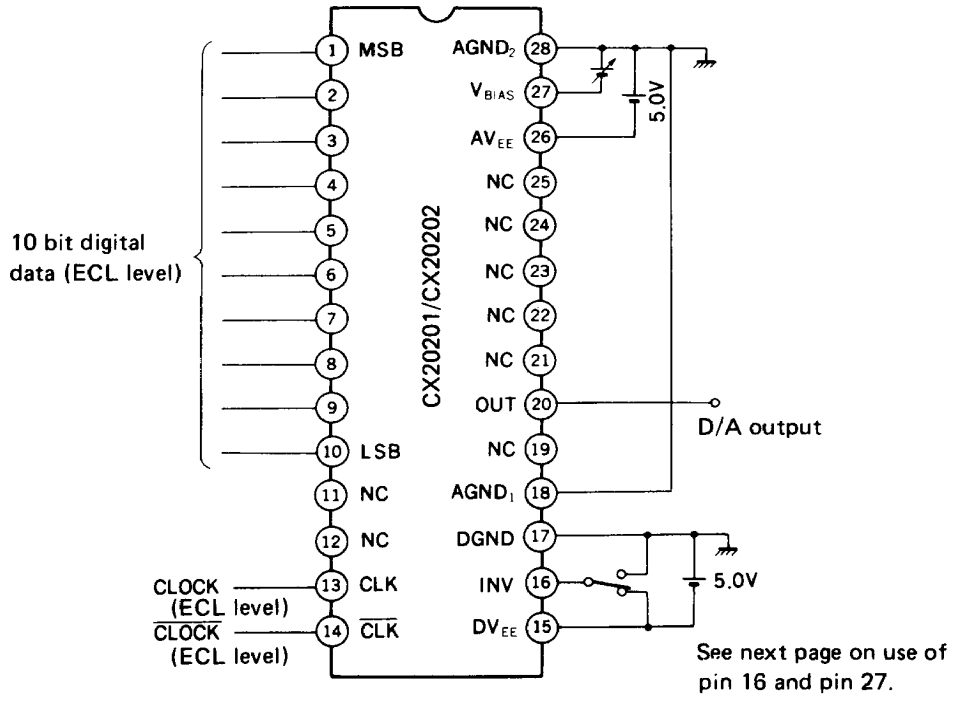
Waveform at point A




Waveform at point B


When $f_{MUL} \leqq 14$ MHz, the following relation is to be satisfied. $0.71 \leqq V_{O(FS)} \leqq 1.00$ (Unit: Vp-p)

**Fig. 12 Typical Circuit Connection**



**Note on use**

See Fig. 12

Supplementary items are described below.

**(1) Setting of pin 16 (INV)**

The relation, between the binary code of digital data and D/A output voltage, can be selected in two ways as shown in the following list.

CASE1: In case pin 16 is connected to D.VEE.

CASE2: In case pin 16 is connected to D.GND.

| Digital data binary code | | | | | | | | | | D/A output voltage (Unit: V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | LSB | CASE 1 | CASE 2 |
| H | H | H | H | H | H | H | H | H | H | $V_{O(OS)}$ | $V_{O(OS)}-1.000$ |
| H | H | H | H | H | H | H | H | H | L | $V_{O(OS)}-0.001$ | $V_{O(OS)}-0.999$ |
| H | H | H | H | H | H | H | H | L | H | $V_{O(OS)}-0.002$ | $V_{O(OS)}-0.998$ |
| | | | | ⋮ | | | | | | ⋮ | ⋮ |
| H | L | L | L | L | L | L | L | L | L | $V_{O(OS)}-0.500$ | $V_{O(OS)}-0.502$ |
| L | H | H | H | H | H | H | H | H | H | $V_{O(OS)}-0.501$ | $V_{O(OS)}-0.501$ |
| L | H | H | H | H | H | H | H | H | L | $V_{O(OS)}-0.502$ | $V_{O(OS)}-0.500$ |
| | | | | ⋮ | | | | | | ⋮ | ⋮ |
| L | L | L | L | L | L | L | L | L | L | $V_{O(OS)}-1.000$ | $V_{O(OS)}$ |

This is the case when the voltage at pin 27 is so adjusted that the full-scale output voltage becomes 1.000V.

$V_{O(OS)}$ is the voltage of zero offset.

**(2) Setting of pin 27 ($V_{BIAS}$)**

Pin 27 to be fed a reference voltage externally.

The full-scale of D/A output voltage is determined by the reference voltage.

There is a range in which a linear relation is established between the reference voltage $V_{BIAS}$ and the full-scale $V_{O(FS)}$.

The range is

$0.50 \leqq V_{O(FS)} \leqq 1.50$ (Unit: V)

(It is a typical value at $V_{EE}=-5.0V$ and $Ta=25°C$.)

As a concrete circuit to apply reference voltage externally to pin 27, several kinds of circuits are conceivable. The example are shown below. Provided that $Z_L$, to be connected to pin 20, is considerably larger than 10 kΩ.

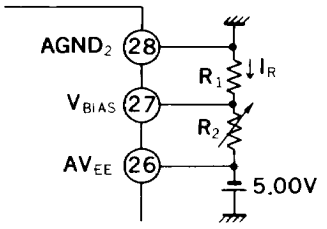



Fig. 13

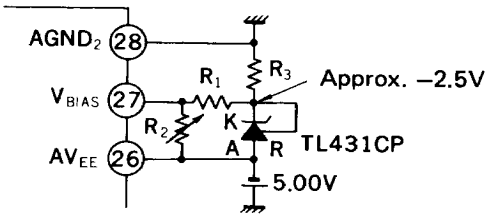



**Fig. 14 Example using the TL431CP regulator.**

**(Ex.1) An example of comparatively simpler circuit**

In Fig. 13, adjust $V_{BIAS}$ so that the full-scale of D/A output voltage becomes 1.000V.

In this case, it is necessary to determine $R_1$ and $R_2$ so as to obtain $I_R > 500\ \mu A$. For example, $R_1 = 8.2\ k\Omega$ and $R_2 \simeq 1.5\ k\Omega$.

When $V_{EE} = -5.00V$, $V_{BIAS}$ becomes nearly $-4.20V$.

**(Ex.2) An improved example of Ex.1** (Countermeasure against power supply voltage fluctuation)

Fig. 14 is an example which is improved in the sensitivity of D/A output to power supply voltage fluctuation.

Make $R_2$ variable and adjust $V_{BIAS}$ so that the full-scale of D/A output voltage becomes 1.000V. In this case, too, it is necessary to determine constants of $R_1$, $R_2$ and $R_3$ so as to be $I_R \gtrsim 500$ uA. $R_1 = 3.6\ k\Omega$, $R_2 > 1.5\ k\Omega$ and $R_3 = 5.1\ k\Omega$ are suitable values.

**Dependence of Output Voltage Full-scale on Power Supply Voltage**

The relation between $V_{O(FS)}$ and $V_{BIAS} - V_{EE}$ is shown in Fig. 20.

$V_{BIAS}$ is set with the circuit shown in Fig. 14.

From the figure, relational equation is derived, as follows.

$$\Delta V_{O(FS)} = K \cdot \Delta (V_{BIAS} - V_{EE}) \qquad K = 1.29$$

where $\Delta V_{O(FS)}$ and $\Delta (V_{BIAS} - V_{EE})$ denote changed values.

$V_{BIAS} - V_{EE}$ is also fluctuated by the fluctuation of both $V_{BIAS}$ and $V_{EE}$.

As a result, the fluctuation of D/A output voltage full-scale occurs, which will be obtained by the equation.

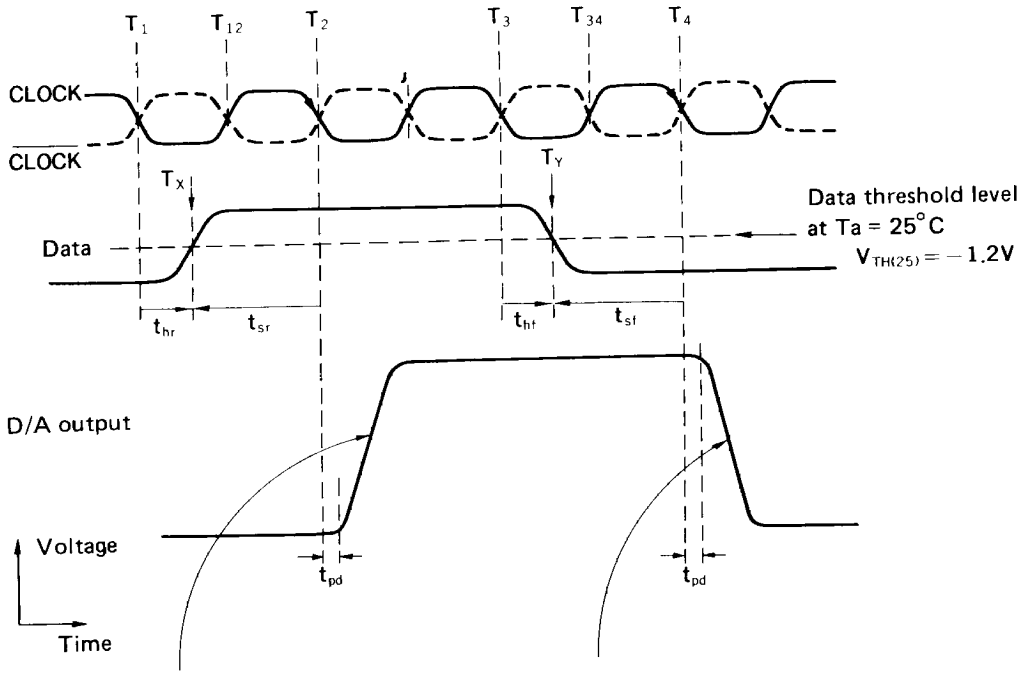
**(3) Phase relation between digital data and clock**

To obtain the specified characteristics as a D/A converter, it is necessary to establish correctly phase relation between data and clock externally applied.

The phase relation among data clock and D/A output voltage waveforms are shown in Fig. 15.

The relation between data and D/A output corresponds to the case when pin 16 (INV) is connected to D.$V_{EE}$

Fig. 15 Timing chart




At $t=T_1+t_{hr}=T_2-t_{sr}$, data of individual bits run across $V_{TH(25)}$, and at $t=T_2$, CLK and $\overline{CLK}$ are switched over, then D/A output changes synchronized. D/A output is synchronous with the falling edge of CLK. Data are taken inside at the rising edge of CLK (at $t=T_{12}$).

At $t=T_3+t_{hf}=T_4-t_{sf}$, data of indicidual bits run across $V_{TH(25)}$, and at $t=T_4$, CLK and $\overline{CLK}$ are switched over, then D/A output changes synchronized. D/A output is synchronous with the falling edge of CLK. Data are taken inside at the rising edge of CLK (at $t=T_{34}$).

The phase relation between data of individual bits and clock should satisfy the following conditions, ① and ② .

**[Conditions]**

In the above figure, when each data are switched over from L to H at $t=T_x$, and from H to L: at $t=T_y$,

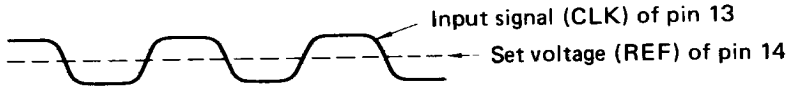
① $t_{hr} \geqq 1.0$ (Unit: ns), and also, $t_{sr} \geqq 6.7$ (Unit: ns)
with, $t_{hr}=T_x-T_1$, $t_{sr}=T_2-T_x$.

② $t_{hf} \geqq 1.0$ (Unit: ns), and also, $t_{sf} \geqq 6.7$ (Unit: ns)
with, $t_{hf}=T_y-T_3$, $t_{sf}=T_4-T_y$.

**(4) Another method of feeding clock signals**

Instead of using clock and clock bar, inverse in phase each other, it is also possible to feed clock of ECL level to pin 13 (CLK), setting the voltage of pin 14 ($\overline{CLK}$) at the central value between H and L of ECL level. In this case, the setting voltage of pin 14 has to be supplied externally.

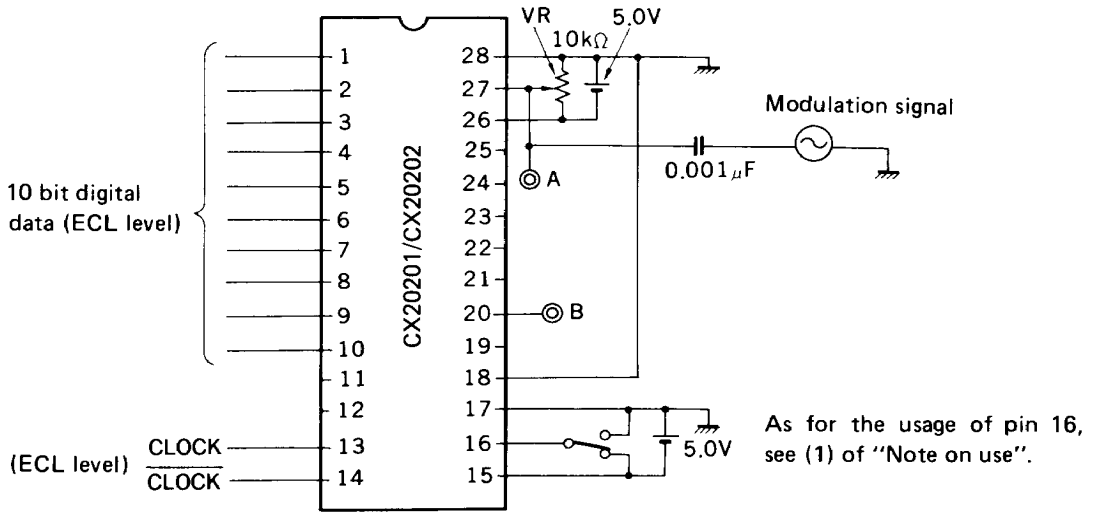
Fig. 16 Another method of feeding clock signal



**(5) Multiplying**

It is possible to apply amplitude modulation to D/A output, with multiplying signal fed to pin 27 ($V_{BIAS}$) externally. In normal usage, after setting the voltage of pin 27 and holding steady the full-scale of D/A output voltage, change digital data. As against this, in the use of multiplying method, D/A conversion is carried out while varying the full-scale of D/A output voltage, by fluctuating the voltage at pin 27 with multiplying signal.
As for the input and output characteristics of the multiplying, see Fig. 21.
An example of the circuit of standard use is shown in Fig. 17.

**Fig. 17 Example of multiplying circuit of standard use**




**Adjustment Method**

① Set pins 1 to 10, 13, 14 and 16 in accordance with the conditions shown in Fig. 11.
② Adjust VR so that DC voltage at point B becomes −1.00V, with no sine wave fed to pin 27. Then, the DC voltage at point A is defined as $V_{BIAS}$ (Unit: V).
③ Apply sine wave to pin 27, and adjust the amplitude so that the amplitude of the waveform observed at point A becomes ($V_{BIAS}$+5.0)/2 (Unit: V).

**(6) Load of D/A output terminal**

The value of the temperature coefficient $T_{CF(OS)}$ of D/A output voltage full-scale and the value of the temperature coefficient $T_{CF(OS)}$ of output voltage zero offset are those in condition that load $Z_L$ of output terminal (pin 20) satisfies $Z_L > 10$ kΩ. When $Z_L \leqq 10$ kΩ, the temperature coefficient of the load resistance exerts an effect, and both $T_{CF(FS)}$ and $T_{CF(OS)}$ shift. In addition, $T_{CF(FS)}$ and $T_{CF(OS)}$ change in accordance with the kind of loads to be connected. Accordingly, in order to obtain the above-mentioned $T_{CF(FS)}$ and $T_{CF(OS)}$, it is necessary to make $Z_L$ to be $Z_L > 10$ kΩ. That is, pin 20 should be connected to the high impedance as mentioned above.

**(7) Noise reduction countermeasure**

Since 1 step of the D/A output voltage is such a small voltage of approx. 1 mV, it is necessary to reduce noises coming into from outside, as much as possible. Accordingly, the following are to be considered:

- When the device is mounted on a circuit board, the board layout should have a ground plane and $V_{EE}$ plane as large as possible in order to reduce sheet resistance and inductance.
- It is desirable that A GND (Analog Ground) and D GND (Digital Ground) are separated each other, and so as, A $V_{EE}$ and $DV_{EE}$ are. It is recommended that, for example as shown in Fig. 18, the wiring of A GND and D GND, A $V_{EE}$ and D $V_{EE}$ should be separated each other except the power supply, and they should be made common very close to the source.
- The coupling capacitors, 47 $\mu$F (tantalum) and 1000 pF (ceramic) in parallel, should be utilized between the $V_{EE}$ and GND plane which are placed next to each other. (As shown in Fig. 18 Ⓐ.) Also, it is desired that they should be placed between the $V_{EE}$ and GND plane in the vicinity of the IC. (As shown in Fig. 18 Ⓑ.) These parts are needed to prevent bad effects in characteristics of the IC caused by noises coming inside.
- It is recommended to insert a capacitor of over 0.1 $\mu$F between pin 27 and pin 26, in order to reduce spurious noise which disturbs D/A output. This is only applicable when multiplying is not needed.

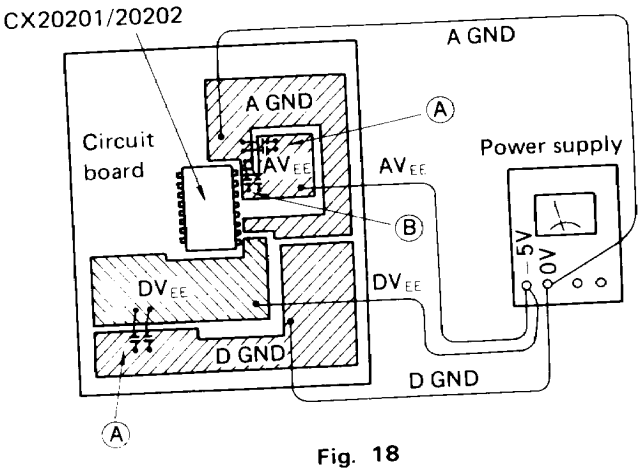



Fig. 18

**Output voltage full-scale v.s. Bias voltage**

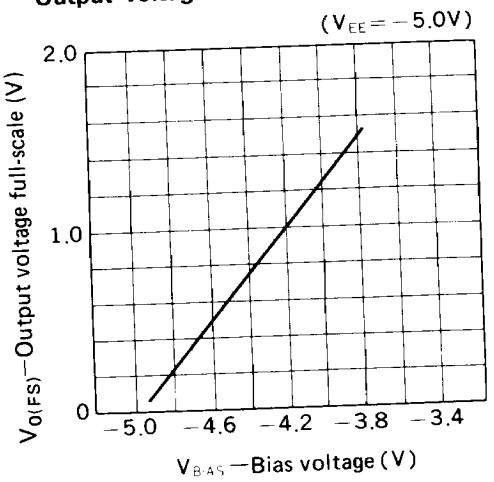



Fig. 19

**Output voltage full-scale v.s. $V_{BIAS}-V_{EE}$**
($V_{O(FS)}$=1.00V, with $V_{EE}$=−5.00V, see Fig. 14.)

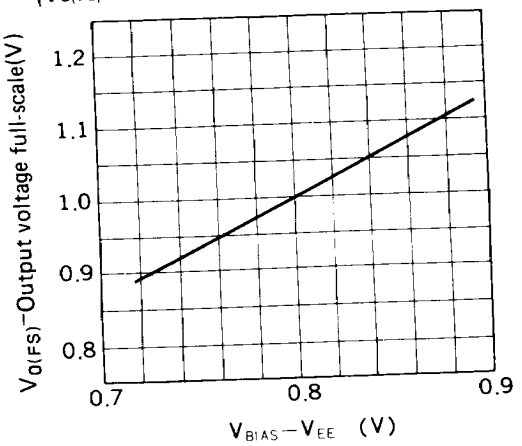



Fig. 20

**Multiplying input/output characteristics**

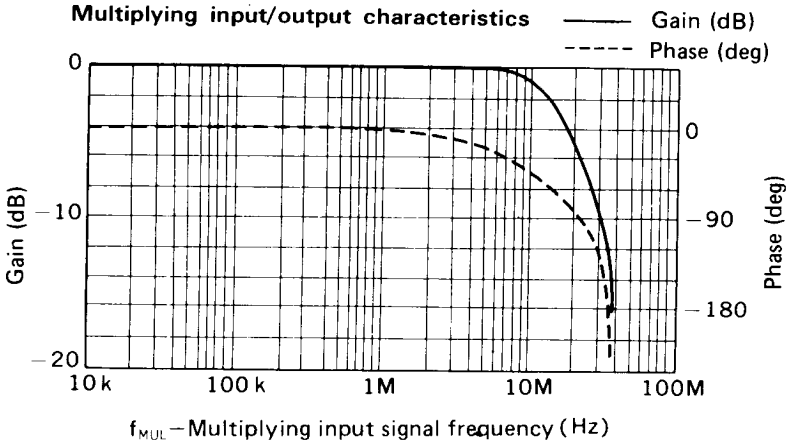



**Fig. 21**

**Power dissipation decreasing curve**

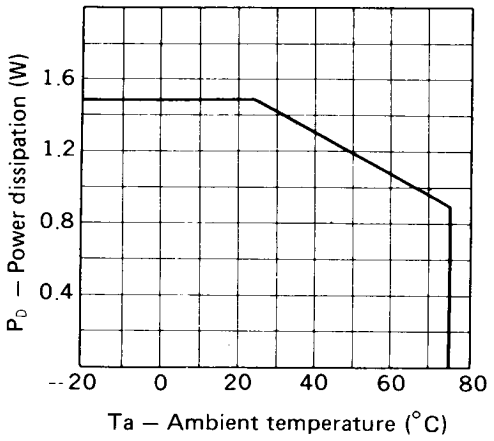



**Fig. 22**



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