CX65001

160 – 700 MHz Linear Power Amplifier Driver

Skyworks′ CX65001 Microwave Monolithic Integrated Circuit (MMIC) power amplifier driver offers a desirable combination of features that provide superb performance and ease of use in a low-cost Surface-Mounted Technology (SMT) package. The Gallium Arsenide (GaAs) Heterojunction Bipolar Transistor (HBT) power amplifier driver was developed and optimized for extreme linear performance in a variety of applications. It is ideal as a driver or output stage for transceivers and repeaters for Trans-European Trunked Radio (TETRA), GSM400 and paging base stations, mobile radios, and many other applications.

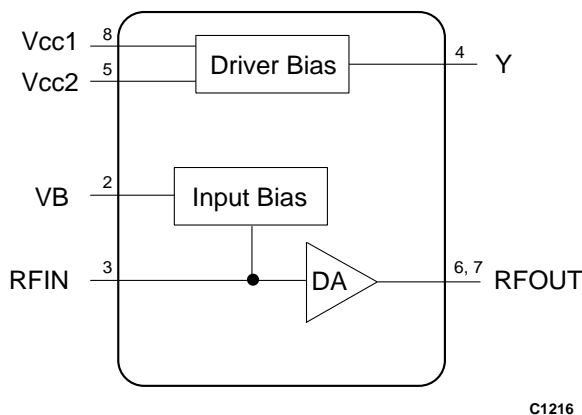Figure 1 shows a functional block diagram for the CX65001. The device package and pinout are shown in Figure 2.

Features

- 5 V single supply operation
- Linear Pout of 24 dBm
- OIP3 of 45 dBm
- Internal bias circuits
- Surface mounted Small Outline Integrated Circuit (SOIC) 8-pin package with downset ground paddle

Applications

- TETRA transceivers
- GSM400
- Wireless Local Loop (WLL) and Industrial, Scientific, Medical (ISM) bands
- Repeaters
- Paging
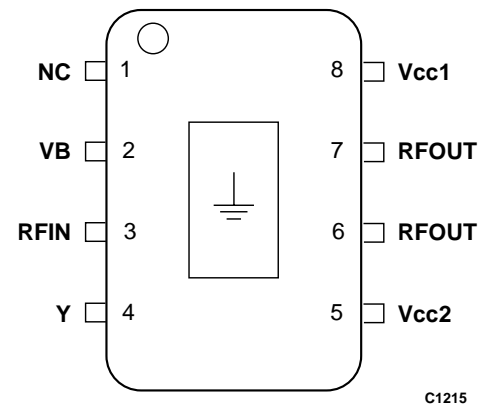- Mobile radios
- VHF/UHF TV broadcast

Figure 1. CX65001 Functional Block Diagram

Figure 2. CX65001 Pinout – 8-Pin SOIC Package (Top View)

Electrical and Mechanical Specifications

The signal pin assignments and functions are described in Table 1. The absolute maximum ratings of the CX65001 are provided in Table 2. The recommended operating conditions are specified in Table 3 and electrical specifications are provided in Table 4.

Typical performance characteristics of the CX65001 are illustrated in Figures 3 through 11.

Table1. CX65001 Signal Descriptions

Pin #	Name	Description
1	NC	No connection
2	VB	Input bias for driver amplifier
3	RFIN	RF input
4	Y	Output of internal bias circuit
5	Vcc2	Supply voltage
6	RFOUT	RF output
7	RFOUT	RF output
8	Vcc1	Supply voltage
9	GND	Ground

Table 2. CX65001 Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Units
RF input power	P_{IN}			6	dBm
Supply voltage	Vcc			5.5	V
Supply current ($I_D + I_{BIAS}$)	Icc			240	mA
Power dissipation				1.3	W
Case operating temperature	T_C	–40		+85	°C
Storage temperature	T_{ST}	–55		125	°C
Junction temperature	T_J			150	°C
Note: No damage to device if only one parameter is applied at a time with other parameters at nominal conditions.					

Table 3. CX65001 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
Supply voltage	Vcc		5		V
Frequency range	F	160		700	MHz
Junction temperature	T_J			140	°C
Maximum bias condition =	$(V_{CC} \times I_D) < (T_{J\_RECOMMENDED} - T_C)/R_{TH,J-C}$				

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Table 4. CX65001 Electrical Characteristics
(Vcc = 5 V, Tc = 25 °C)

Parameter	Symbol	Test Conditions	Min	Typical	Max	Units
OIP3 match, Frequency = 450 MHz (Note 1)						
Supply current (I$_D$ + I$_{BIAS}$)	I$_{CC}$	R$_{BIAS}$ = 270 Ω		120	130	mA
Small signal gain	G	P$_{IN}$ = –15 dBm	21	22		dB
Linear output power (Note 2)	P$_{OUT}$	P$_{IN}$ = +3 dBm	23	24		dBm
Power Added Efficiency	PAE	P$_{IN}$ = +3 dBm	35	42		%
Noise Figure (NF)	NF			4	5	dB
Output IP3	OIP3	Two CW tones with 1 MHz spacing P$_{IN}$ = –16 dBm per tone	42	45		dBm
Thermal resistance (junction – case)	R$_{TH,J-C}$			91		°C/W
Note 1: Device matched for optimum OIP3 according to circuit shown in Figure 12.						
Note 2: For reliable operation, do not violate the maximum input drive level specified in Table 2.						
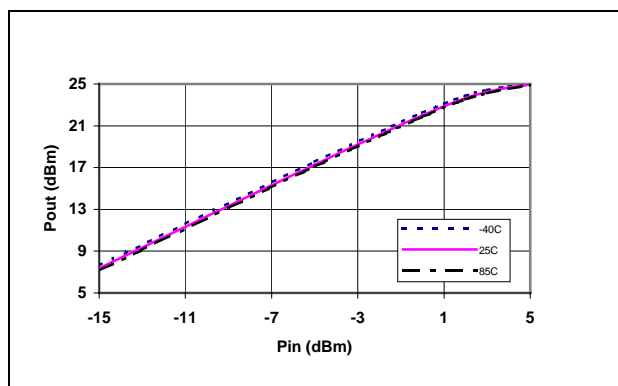
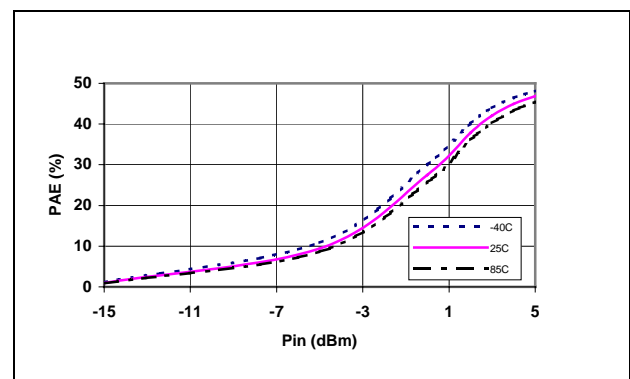Figure 3. Typical Pout vs Pin @ 450 MHz Over Temperature (Circuit Match for Optimum OIP3)

Figure 4. Typical PAE vs Pin @ 450 MHz Over Temperature (Circuit Match for Optimum OIP3)
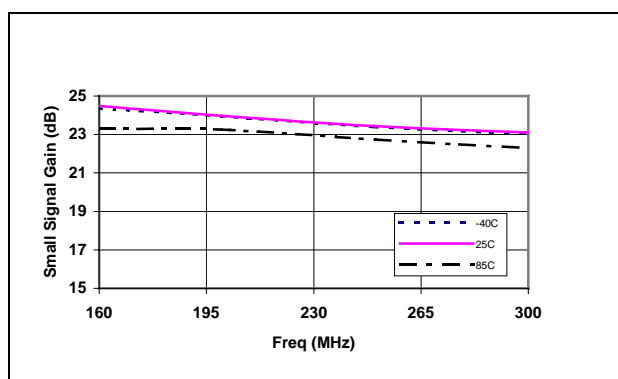

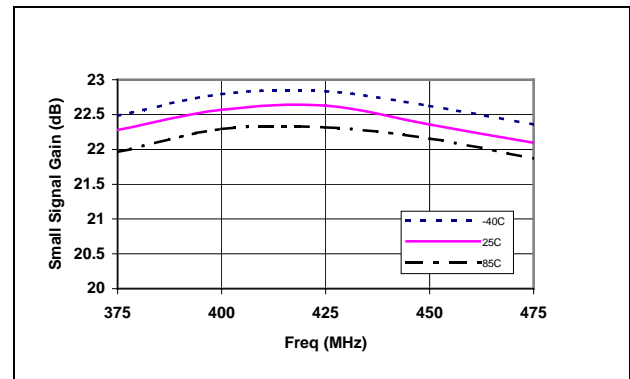Figure 5. Typical Small Signal Gain From 160 to 300 MHz Over Temperature (Circuit Match for Optimum Gain)

Figure 6. Typical Small Signal Gain From 375 to 475 MHz Over Temperature (Circuit Match for Optimum OIP3)
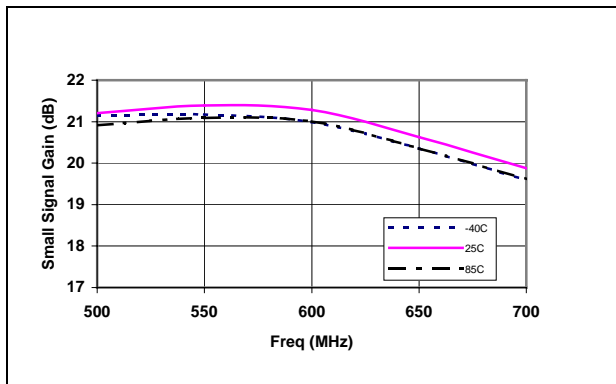
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Figure 7. Typical Small Signal Gain From 500 to 700 MHz Over Temperature (Circuit Match for Optimum Gain)
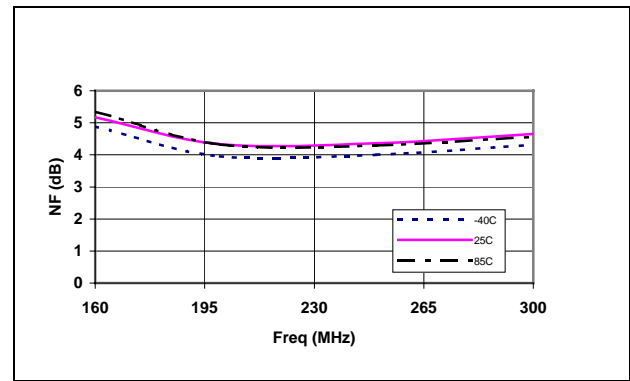
Figure 8. Typical Noise Figure From 160 to 300 MHz Over Temperature (Circuit Match for Optimum Gain)
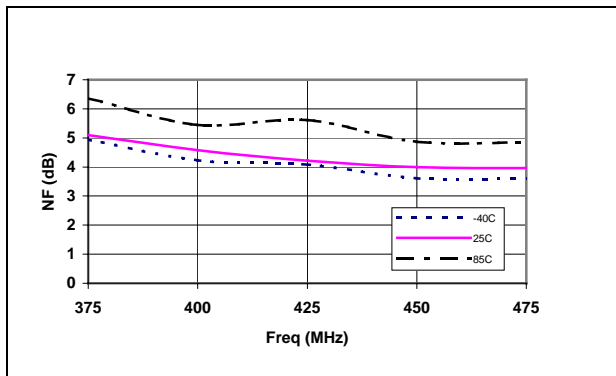
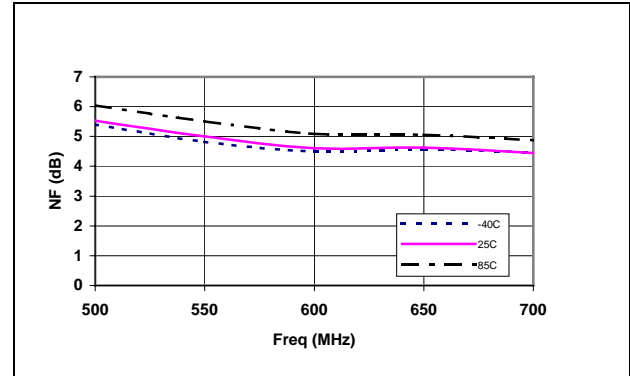Figure 9. Typical Noise Figure From 375 to 475 MHz Over Temperature (Circuit Match for Optimum OIP3)

Figure 10. Typical Noise Figure From 500 to 700 MHz Over Temperature (Circuit Match for Optimum Gain)
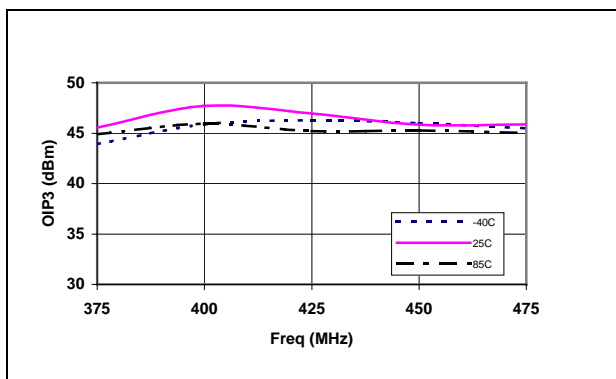
Figure 11. Typical OIP3 From 375 to 475 MHz Over Temperature (Circuit Match for Optimum OIP3)

Evaluation Board Description

The CX65001 Evaluation Board is used to test the CX65001 power amplifier's performance. The CX65001 Evaluation Board schematic diagram is shown in Figure 12. The schematic shows the basic design of the board for the 375 to 475 MHz range. The Evaluation Board assembly diagram is shown in Figure 13 and the Evaluation Board layer detail is shown in Figure 14. Figure 15 provides the mounting footprint for the CX65001.

Circuit Design Configurations _____

The following design considerations need to be followed regardless of final use or configuration:

1. Paths to ground should be made as short as possible.

2. The ground pad of the CX65001 power amplifier has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the amplifier. As such, design the connection to the ground pad to dissipate the maximum wattage produced to the circuit board. Multiple vias to the grounding layer are required (see Figures 14 and 15).

Note: Junction temperature (T_J) of the device increases with a poor connection to the slug and ground. This reduces the lifetime of the device.

3. Five external bypass capacitors, a 1 μF and four 100 pF capacitors, are required on the Vcc line and on pin 4, pin 5, and pin 8. Capacitors C7 (100 pF) and C8 (1 μF) are placed in parallel between the supply line and ground, C4 (100 pF) is placed between pin 4 and ground, C5 (100 pF) is placed between pin 8 and ground, and C6 (100 pF) is placed between pin 5 and ground.

4. A bias resistor, R1 (270 Ω), is used to control Vcc1 (reference voltage of the bias circuit) at pin 8. The nominal total current with a 270 Ω bias resistor is 125 mA with Vcc1 and Vcc2 equal to 5 V. Inductor L3 (39 nH) is placed between the RF output transmission line and Vcc supply voltage line.

5. Inductor L2 (27 nH) is placed between pin 4 (bias circuit output) and pin 2 (base of RF transistor) for bias circuit and RF transistor connection.

6. Inductor L1 (15 nH), and capacitors C1 (12 pF) and C2 (15 pF) are the input matching components and capacitor C10 (56 pF) is the output matching component. Use a short transmission line (about 100 mils) between the RF input pin (pin 3) and RF input matching components (C1, C2, and L1). Also use a short output transmission line (about 100 mils) between the RF output pins (pin 6 and pin 7) and the RF output matching component (C10).

Testing Procedure _____

Use the following procedure to set up the CX65001 Evaluation Board for testing, Refer to Figure 16 for guidance:

1. Connect a 5.0 V supply to Vcc. If available, enable the current limiting function of the power supply to 240 mA.

2. Connect a signal generator to the RF signal input port. Set it to the desired RF frequency at a power level of –15 dBm or less to the Evaluation Board but do NOT enable the RF signal.

3. Connect a spectrum analyzer to the RF signal output port.

4. Enable the power supply.

5. Enable the RF signal and take measurements.

Caution: *If any of the input signals exceed the rated maximum values, the CX65001 Evaluation Board can be permanently damaged.*
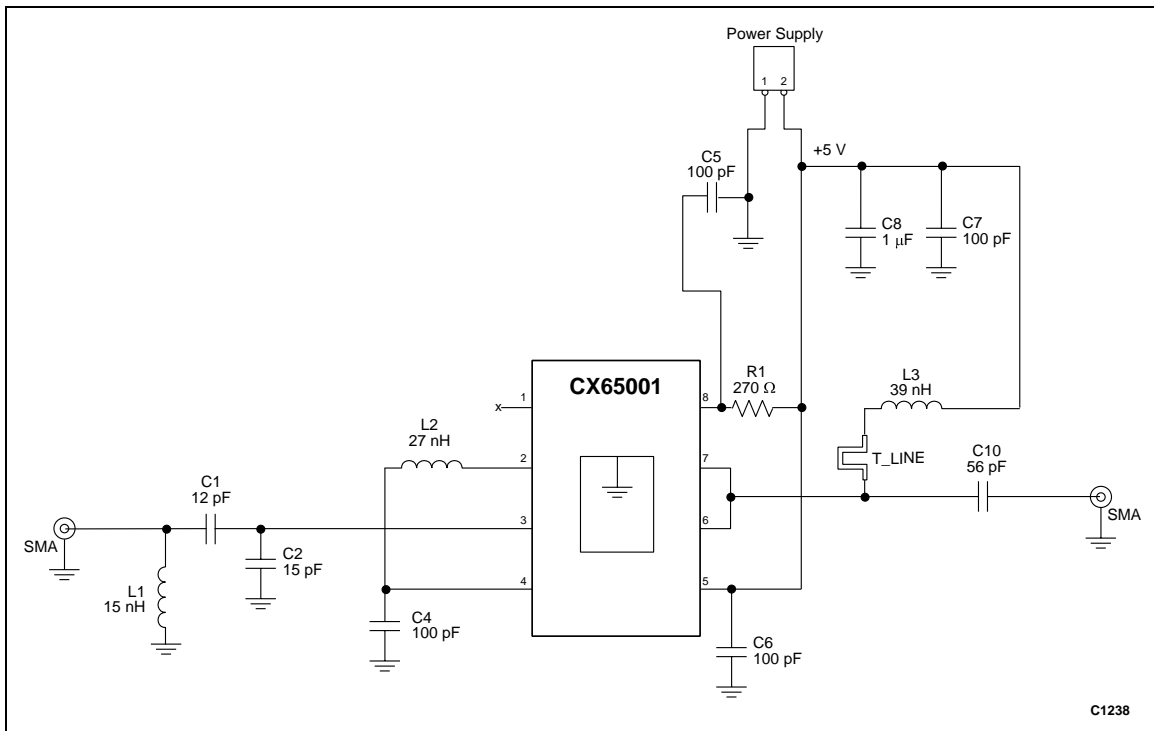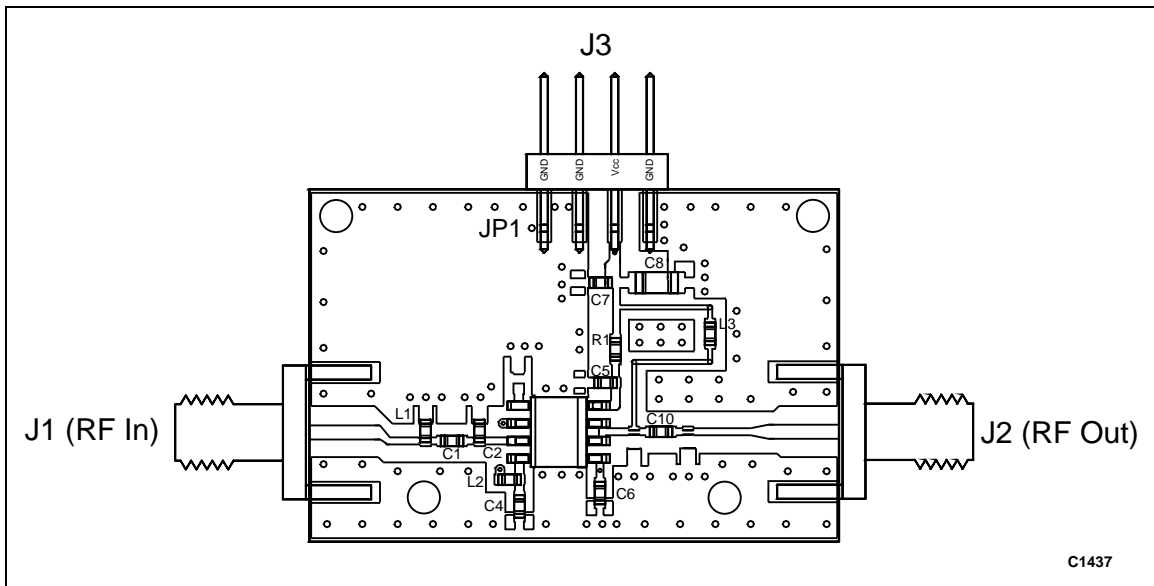

Figure 12. Application Schematic Optimized for OIP3 @ 450 MHz
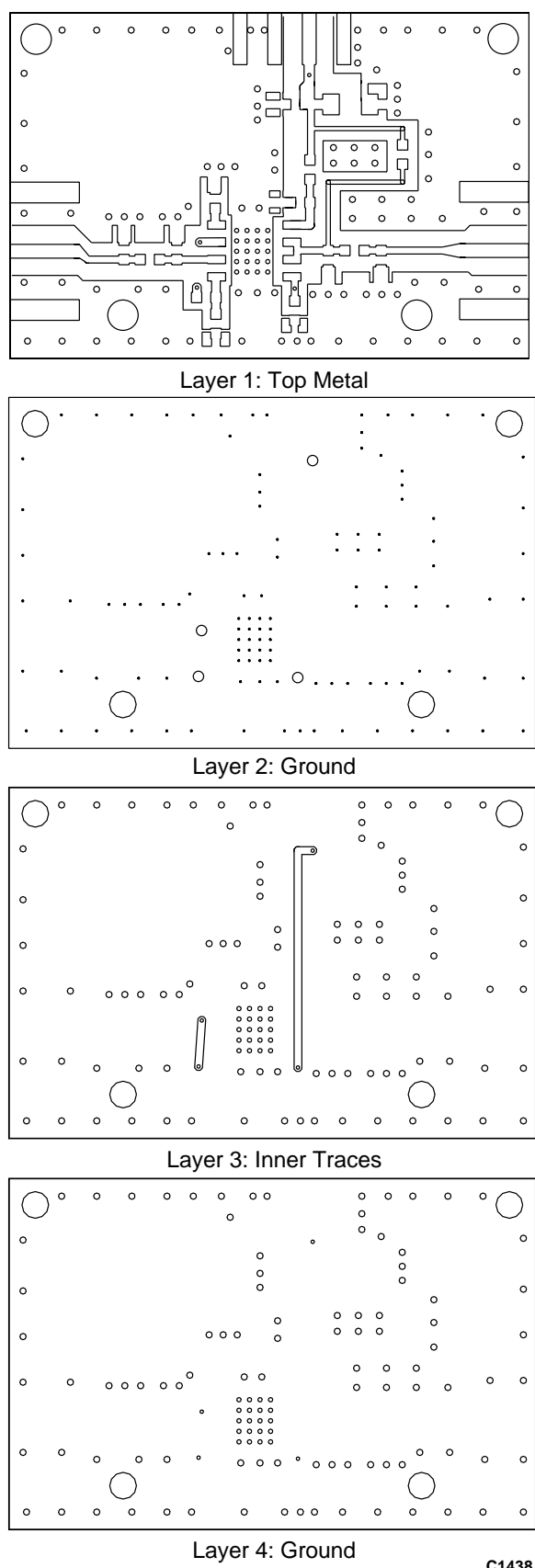

Figure 13. Evaluation Board Assembly Diagram
(Top View)

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Layer 1: Top Metal

Layer 2: Ground

Layer 3: Inner Traces

Layer 4: Ground

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Figure 14. Evaluation Board Layer Detail
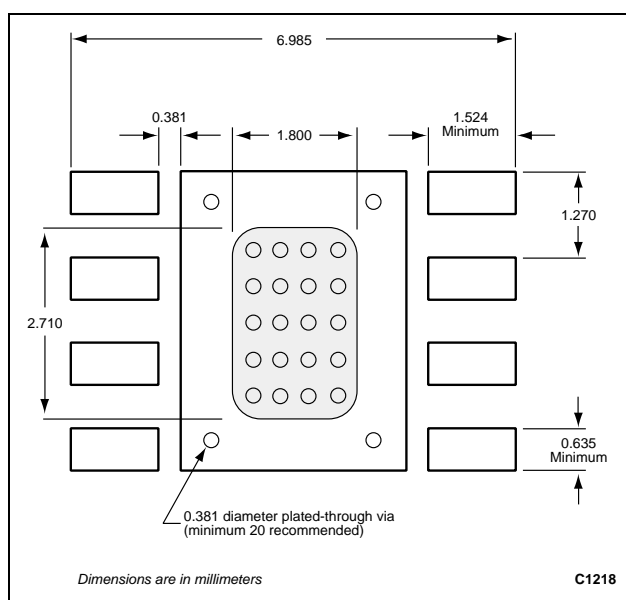
Figure 15. PCB Mounting Footprint
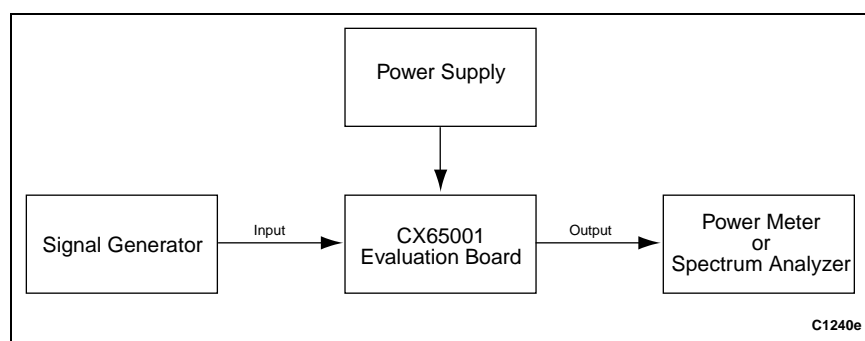
Figure 16. CX65001 Evaluation Board Testing Configuration

Package Dimensions

Figure 17 shows the package dimensions for the 8-pin SOIC and Figure 18 provides the tape and reel dimensions.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second. Maximum temperature should not exceed 225 °C and the time spent at a temperature that exceeds 210 °C should be limited to less than 10 seconds. If the part is manually attached, precaution should be taken to ensure that the part is not subjected to a temperature that exceeds 300 °C for more than 10 seconds.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. For additional details on both attachment techniques, precautions, and recommended handling procedures, refer to the Skyworks document *Solder Reflow Application Note*, document number 101536.

Production quantities of this product are shipped in a standard tape and reel format. For packaging details, refer to the Skyworks document *Tape and Reel Information Application Note*, document number 101568.

Electro-Static Discharge (ESD) Sensitivity

The CX65001 is a static-sensitive electronic device. Do not operate or store near strong electrostatic fields. Take proper ESD precautions.
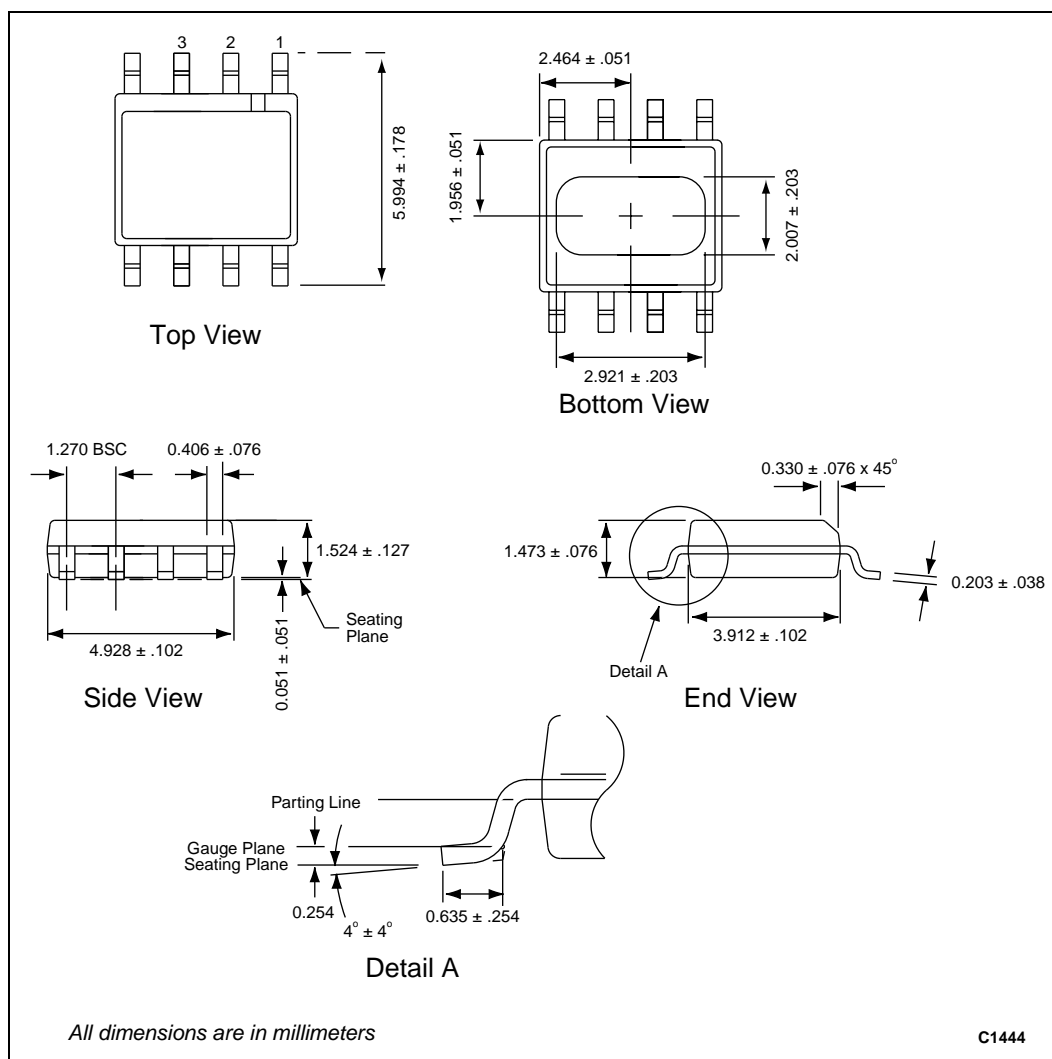
3 2 1

5.994 ± .178

Top View

2.464 ± .051

1.956 ± .051

2.007 ± .203

2.921 ± .203

Bottom View

1.270 BSC   0.406 ± .076

1.524 ± .127

0.051 ± .051

Seating Plane

4.928 ± .102

Side View

0.330 ± .076 x 45°

1.473 ± .076

0.203 ± .038

3.912 ± .102

Detail A

End View

Parting Line

Gauge Plane
Seating Plane

0.254

4° ± 4°

0.635 ± .254

Detail A

All dimensions are in millimeters

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Figure 17. CX65001 8-Pin SOIC Package Dimension Drawing

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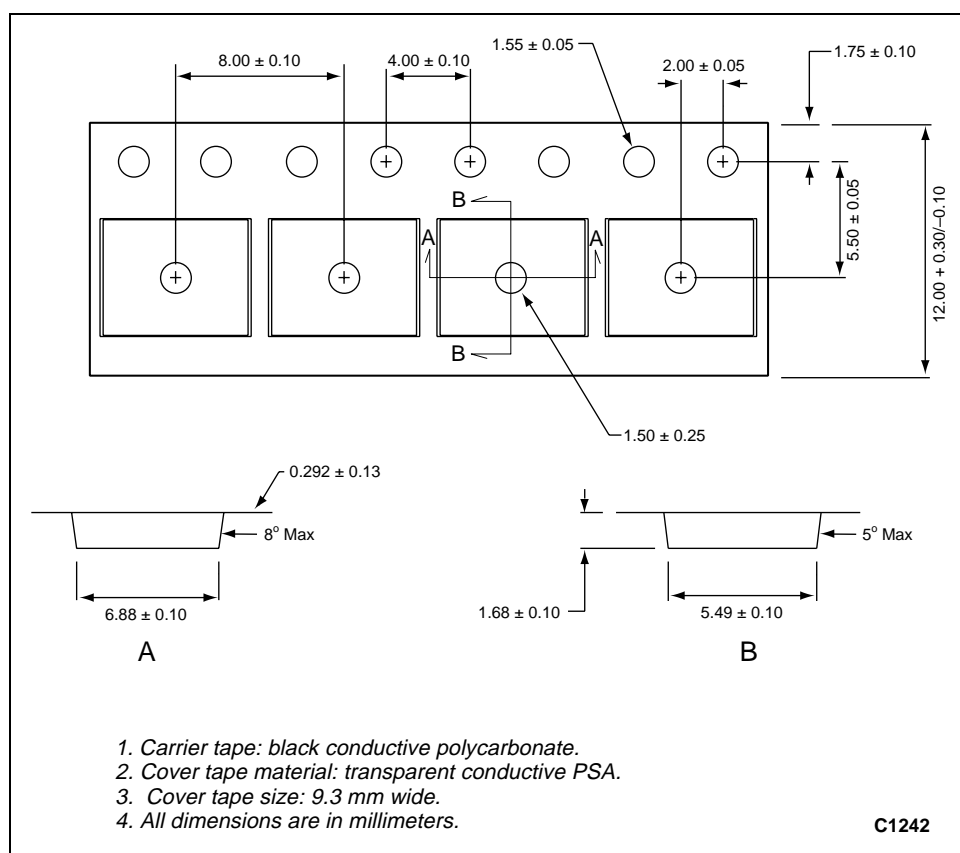
Figure 18. CX65001 8-Pin SOIC Tape and Reel Dimensions

1. Carrier tape: black conductive polycarbonate.
2. Cover tape material: transparent conductive PSA.
3. Cover tape size: 9.3 mm wide.
4. All dimensions are in millimeters.

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Ordering Information

Model Name	Ordering Part Number	Evaluation Kit Part Number
CX65001 160-700 MHz Linear Power Amplifier Driver	CX65001-12	TW10-D282 (tuned for optimum OIP3 @ 450 MHz)

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