# Dual Fractional-N Synthesizers/PLLs Frequently Asked Questions

This document provides answers to the following frequently asked questions (FAQs) related to fractional-N synthesizers in general, and to Skyworks' CX72300, CX72301, CX72302, and CX74038 fractional-N synthesizers and their respective Evaluation Boards, specifically:

### General Questions



### CX7230x and CX74038 Evaluation Boards



### Skyworks' Synthesizer Package Types



### Synthesizer Functioning



**What are the design trade-offs associated with fractional-N synthesizers?**

This subject is fully discussed in the *Basics of Dual Fractional-N Synthesizers/PLLs* White Paper (document number 101463) available at http://www.skyworksinc.com/.

**What is the primary benefit of fractional-N synthesizers?**

Fractional-N synthesizers afford a greater design flexibility over integer-N synthesizers. This flexibility allows:

- very fine step size
- very high comparison frequency
- wide loop bandwidth implementations
- rapid lock-up times
- good phase noise performance

**Can I use a lower reference frequency with the fractional-N synthesizers?**

When a fractional-N synthesizer is used, it is best to use the highest possible reference source. This yields the lowest N value (i.e., best phase noise). Also, $\Delta\Sigma$ modulator quantization noise is subject to maximum attenuation. The quantization noise peaks at a frequency equal to 1/3 the comparison frequency from the carrier with a null at 1/2 the comparison frequency.

Quantization noise rises at 60 dB/decade. Depending on the loop bandwidth and the reference frequency, quantization noise may appear in the VCO output spectrum. Generally, if the comparison frequency is 10 MHz or above, with a loop bandwidth of 80 to 100 kHz, quantization noise does not present a problem.

**What spurs can be expected from fractional-N synthesizers versus integer-N synthesizers?**

The primary spurs associated with integer-N Phase Locked Loops (PLLs) are reference spurs. The relationship between the comparison frequency (step size) and loop bandwidth ultimately determines the level of attenuation afforded. Fractional-N synthesizers can exhibit fractional, reference, or integer-N boundary spurs.

**Fractional Spurs**. The most serious spurs found on fractional-N synthesizers (but not present on the Skyworks' synthesizer designs) are fractional spurs. They appear all around the Voltage-Controlled Oscillator (VCO) carrier regardless of the frequency to which it is programmed.

The spacing of these spurs is usually equal to the channel step size of the fractional-N synthesizer (or half the channel step size). For example, an 18-bit fractional-N implementation using a 10 MHz comparison frequency would have fractional spurs spaced at 10 MHz/$2^{18}$ (38 Hz) around the carrier.

Fractional spurs are buried in the phase noise of all Skyworks' fractional-N synthesizers.

**Reference Spurs**. With fractional-N synthesizers, the comparison frequency is very high, which allows large loop filter attenuation of the reference spur (even with a wide loop bandwidth implementation).

**Integer-N Boundary Spurs**. Integer-N boundary spurs appear when the VCO/PLL is programmed to frequencies that are near harmonic multiples of the comparison frequency. They exhibit an amplitude of between –55 to –65 dBc when measured inside the loop bandwidth on the CX7230x (or –30 dBc when measured on the CX74038).

The exact mechanism that precipitates these spurs is not entirely understood. The spurs tend to lessen when the VCO drive level into the VCO divider port is lowered. The spurs are spaced a distance equal to the comparison frequency. For example, a 10 MHz comparison frequency yields a spur-free VCO/PLL tuning range of nearly 10 MHz.

All fractional-N synthesizers exhibit these spurs. However, the Skyworks' family of CX7230x synthesizers offer the best integer-N boundary spur performance currently available.

There may also be a spur that occurs near divide values of 1/2, 1/4, 1/8...1/$2^n$ (e.g., 41.5, 41.25, 41.125). If present, these spurs have lower amplitude than the primary integer-N spur located at the harmonic of the comparison frequency. For example, with a 10 MHz comparison frequency and a VCO divider value of 41.5005 yields a VCO output frequency of 415.005 MHz. The spur, if present, would appear at 415.000 MHz.

Whether or not these spurs can pose a problem is dependent on the following:

- required frequency band plan (actual LO channel frequency assignments)
- comparison frequency
- loop bandwidth
- system's spur specification

**What is meant by the term "spur-free"?**

The term "spur free" refers to the fact that there are no fractional spurs. Fractional spurs are buried in the phase noise of all Skyworks' fractional-N synthesizers.

Integer-N boundary spurs occur at harmonic multiples of the internal reference (comparison) frequency and are typically –55 to –65 dBc as measured inside the loop bandwidth (CX7230x, measured inside the loop bandwidth of 80 kHz @ 10 kHz offset from spur). A spur may also occur near divide values of 0.5 (e.g., N = 41.50005). If present, these spurs have a lower amplitude than the primary integer-N boundary spur located at a harmonic of the comparison frequency.

The use of a 25 MHz comparison frequency would offer nearly 25 MHz of spur-free VCO tuning spectrum. All fractional-N synthesizers are subject to integer-N boundary spurs.

Spur performance specifications for fractional-N synthesizers usually refer to the fractional spurs that occur all around the VCO carrier regardless of the VCO frequency. There are no fractional-N spurs present with any of the Skyworks' synthesizers (both the CX7230x family and the CX74038).

**Does fractional-N offer improved phase noise over integer-N?**

Yes. Depending on the channel step size (and system architecture), a fractional-N design may offer improved phase noise due to the high comparison frequency.

If a channel step size of 200 kHz is needed at 1800 MHz, use of an integer-N PLL yields an N value of 9000. The use of a fractional-N PLL offers an N value of only 180 (assuming a 10 MHz comparison for the fractional-N implementation).

This translates into a 20log(N) gain of 34 dB (20log[9000/180]). If this figure is applied to the phase detector noise floor of a good integer-N PLL phase detector (e.g., –165 dBc/Hz), a typical noise floor value would be: –165 + 34 = –131 dBc/Hz. This is the typical phase noise floor of Skyworks' fractional-N synthesizers when operating at a high comparison frequency (up to 25 MHz). In this particular case the resulting phase noise is identical (comparing integer-N versus fractional-N implementation).

However, when Skyworks' fractional-N synthesizers are used at comparison frequencies greater than 10 MHz, the resulting N value is smaller (<180). This further improves the system phase noise beyond that achievable with an integer-N PLL.

**Does fractional-N offer improved switching time over integer-N?**

Yes. If small step size and a fast lock-up time are the design goals, integer-N solutions do not provide the needed performance. As the loop bandwidth is broadened to achieve the switching time on an integer-N PLL, reference spurs rise excessively. The VCO divider value is also large (a large N) due to the low comparison frequency. Therefore, the phase noise is also poor in this case.

Fractional-N synthesizers have been applied to the next generation 2.5 and 3G handsets because they offer rapid switching times with small channel step size (and good phase noise).

Compare an integer-N PLL with a fractional-N PLL that use the same comparison frequency (10 MHz, for example) and the same loop bandwidth. Both exhibit similar switching times and reference spur attenuation (all other system parameters being equal). However, the integer-N PLL has a much larger step size, equal to the comparison frequency of 10 MHz. The fractional-N PLL offers a step size of <5 Hz (assuming a 21-bit $\Delta\Sigma$ modulator).

If the design goal is for a very large channel step size (10 MHz or more), an integer-N implementation may yield suitable switching time performance.

**Where do I purchase Evaluation Boards?**

Evaluation Boards for Skyworks' line of fractional-N synthesizers are available from any authorized distributor. Refer to http://www.skyworksinc.com/ for the nearest distributor.

**The CX7230x Evaluation Boards use baluns on the VCO divider inputs. Are the baluns necessary?**

No. However, if operation of the VCO divider is single-ended, the effective operating range limits of the VCO divider input increase by 6 dB.

**I noticed the CX7230x package is a 28-pin EP-TSSOP. What does "EP" mean?**

Exposed Pad. This pad, located on the bottom side of the IC, provides a ground return path for the auxiliary synthesizer VCO divider power supply. There are several other substrate pads connected to the pad for ground connection.

It is good design practice to attach this pad, even though it is not necessary when only the main synthesizer is going to be used.

**Are the CX7230x synthesizers available in other package types?**

No. The CX72300, CX72301, and CX72302 are only available as 28-pin Exposed Pad Thin Shrink Small Outline Packages (EP-TSSOPs).

**In what package type is the CX74038 available?**

The CX74038 is available in both a 20-pin TSSOP and a 24-pin 3.5 x 4.5 mm Chip Scale Package (CSP).

**What are the differences between the CX7230x group of synthesizers and the CX74038?**

The CX7230x and CX74038 designs are the result of two completely different efforts from different design facilities. As such, the system architectures are completely different. Their only similarity is that they both apply $\Delta\Sigma$ fractional-N techniques.

The CX74038 evolved out of the Global System for Mobile communications (GSM™) chipset group. Therefore, it offers power consumption and package size conducive to battery operated/portable/handheld applications. It is currently being used in Code Division for Multiple Access (CDMA) and Wideband CDMA (W-CDMA) handset designs.

The CX7230x synthesizer designs evolved out of Skyworks' Bluetooth™ design effort. These components offer broader, general purpose applications and do not specifically address the handset market. The CX7230x devices have additional features (such as an on-board crystal oscillator circuit and Direct Digital Modulation) that allow the generation of low bit rate

FSK/MSK/GMSK/FM modulation schemes by writing to a device register to control the instantaneous frequency deviation.

The two designs are similar in terms of phase noise performance. The main difference is that the CX74038 offers an integer-N synthesizer on the auxiliary/IF side, and the CX7230x devices offer both integer-N and 10-bit fractional-N modes on the auxiliary/IF side.

The typical integer-N boundary spurs on the CX7230x devices are also better than those on the CX74038.

**I am only interested in using the CX7230x main synthesizer. Do I need to apply power to the auxiliary supply pins?**

If the auxiliary synthesizer is not going to be used on the specific CX7230x device, power it down using the registers. Alternatively, leave the VCCcp_aux and VCCcml_aux pins disconnected.

Note that if a charge pump pin is left disconnected while the synthesizer is powered, poor spectral performance occurs with the other synthesizer (all Skyworks' synthesizers are dual devices).

**Does charge pump current setting affect phase noise?**

No. However, Evaluation Board loop filters are designed to be used with maximum charge pump settings. Operating the Evaluation Board with a lower charge pump current may give the appearance of degraded near-in phase noise performance due to the modified loop dynamics.

**Is there a charge pump polarity reversal function?**

The CX7230x family of synthesizers does not have a charge pump polarity reversal function. However, the CX74038 synthesizer does have this ability. An external, low noise op-amp must be used to implement polarity reversal on the CX7230x devices.

**What is the CX7230x VCO divider input impedance?**

CX72300 (balanced measurement through balun):

| | |
|---|---|
| 2500 MHz | 64 – j86 Ω |
| 2000 MHz | 101 – j141 Ω |
| 1500 MHz | 142 – j205 Ω |

CX72301(unbalanced measurement, one input ground through capacitor):

| | |
|---|---|
| 1200 MHz | 94 – j141 Ω |
| 1000 MHz | 117 – j156 Ω |
| 800 MHz | 151 – j168 Ω |
| 600 MHz | 198 – j176 Ω |
| 400 MHz | 270 – j164 Ω |

(divider input impedance for the CX72302 has not been precisely measured)

**When the CX7230x is in power-down mode, is the crystal oscillator still operable?**

When the entire device is in power-down mode (address 0x7, bit 0 is set to 1), the crystal circuitry is also powered down and draws minimal current (see below). However, if the main and auxiliary synthesizers are in power-down (address 0x7, bits 4 and 1 are set to 1), the crystal oscillator is left running.

Current consumption is shown below except for the VCCxtal which is approximately 1.3 mA.

Typical current consumption (in μA) of a CX7230x device in power-down mode:

| Power Pin Signals | 2.7 V (Min) | 3.3 V (Max) |
|---|---|---|
| VCCcml_main | 0.1 | 1.1 |
| VCCcp_main | 0.4 | 1.0 |
| VCCxtal | 0.4 | 1.1 |
| VCCcp_aux | 0.4 | 1.1 |
| VCCcml_aux | 0.2 | 1.2 |
| VCCdigital | 0.5 | 1.2 |
| Total: | 2.0 | 6.7 |

**What is the expected lock-up time?**

Lock-up time for large frequency steps (approximately 30 MHz or more) is approximately equal to 10 divided by the loop bandwidth.

**How do I calculate loop filter component values?**

Calculations for loop filter components are described in the respective CX7230x Evaluation Board User Guide available at http://www.skyworksinc.com/.

**What is the Direct Digital Modulation feature of the CX7230x synthesizers?**

Direct Digital Modulation eliminates many previously required components from a radio transmitter, which creates a simple, flexible, cost-effective alternative. This feature of Skyworks' fractional-N synthesizers allows quick stepping of the carrier (VCO) through a range of frequencies to effectively create an FM/FSK/MSK/GMSK (or other constant envelope) continuous phase signal.

For details on this feature, refer to the Skyworks' Application Note *CX72300, CX72301, CX72302 Direct Digital Modulation*, document number 101349.

**How does the CX7230x "frequency power steering" feature operate?**

The intent of the power steering feature is to provide a 30 to 40 percent reduction in acquisition time from other fractional-N synthesizers. When programmed for this mode (address 0x6, bits 5 and 11 set to 1), the LD/PSmain and LD/PS aux pins are configured for power steering operation.

An external hardware circuit connection needs to be made between the LD/PSmain and LD/PS aux pins and the loop filter (simplest configuration is to install a low-value resistor between each of the pins and the largest capacitor of the loop filter). These pins have three possible states. Under a locked condition, the state is high impedance. This allows the charge pump circuitry to control the VCO. During an out of lock condition, the pins drive high to VCC or low to ground, effectively steering the VCO. These pins actually toggle between high impedance and either VCC or ground at the comparison frequency rate during the out of lock condition.

The LD/PSmain and LD/PS aux pins are not current limited as with the charge pump circuitry. Therefore, they can slew the VCO at a faster rate. When the VCO frequency is close to its final destination frequency, the synthesizer switches back to normal charge pump control mode.

A resistor value of a few hundred Ohms is a good starting point if an external hardware circuit connection is made. If the impedance value is too low, the system becomes unstable and is not able to lock.

When programmed for power steering, there is no Lock Detect function. Systems that require a Lock Detect signal cannot use the power steering feature.

**While using the CX74038, I have noticed a pulsating phase noise effect when viewing the VCO output spectrum (on a 1 MHz span setting). It appears like a wave washing in towards the carrier from both sides and then it washes out, away from the carrier and repeats at a slow rate of about once every second. Is this normal behavior? How can it be eliminated?**

Yes. This is normal behavior when the CX74038 synthesizer is programmed for an integer VCO divide value (N = 89, 90, 91, 92.. 260...300, etc.). Internal dithering causes the phase noise to pulsate at a slow rate. This can be eliminated by disabling internal dithering when N is an integer value.

To disable dithering, bits $D_{21}$ and $D_{20}$ of word $00_2$ must be programmed for $11_2$. For all fractional (non-integer) values of N, these bits should be programmed to $10_2$.

**Why is there a dithering disable function on the CX74038?**

See the previous question.

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