CCD Camera Matrix

Description

CXA1338Q-Z and CXA1338R are matrix ICs for CCD cameras and are used for the system with complementary color checkers coding imager ICX026AK. They perform the vertical correlation process by using 1HDL and outputs the RGB signal from the magenta, green, yellow, and cyan input signals.

Features

- Excellent color reproduction as a result of the primary color separation system.
- Two modes are provided for the matrix factor; PRESET and CONTROL.
- The aperture signal in the V direction is output.
- The chroma suppress signal is output.
- The Y_H and Y_L-Y_H signals are output.

Structure

Bipolar silicon monolithic IC

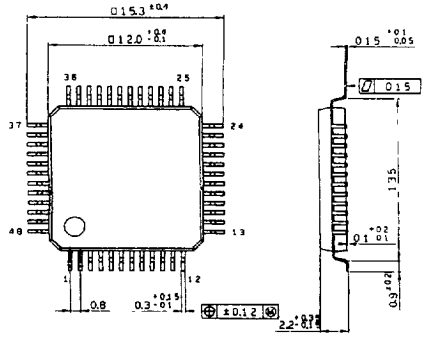
Application

- Complementary color checkers CCD color camera

Package Outline

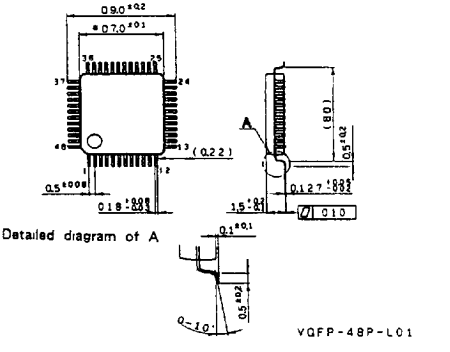
Unit . mm

CXA1338Q-Z 48 pin QFP (Plastic)



QFP-48P-L04

CXA1338R 48 pin VQFP (Plastic)



VQFP-48P-L01

Note) Dimensions marked with * does not include residual resin.

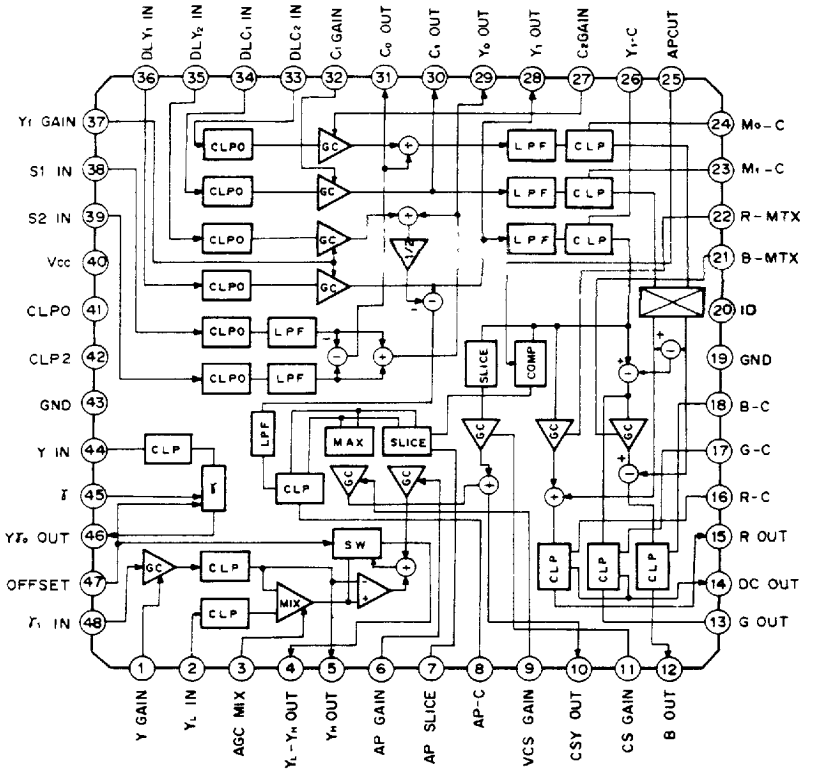
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	7	V
• Storage temperature	Tstg	−55 to +150	°C
• Operating temperature	Topr	−20 to +75	°C
• Allowable power dissipation	PD	600	mW

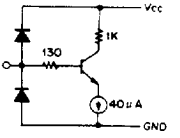
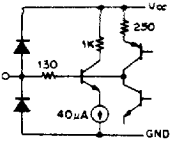
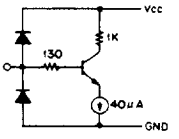
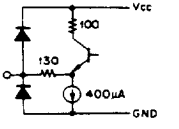
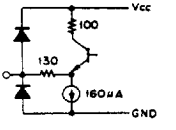
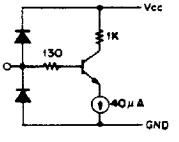
Recommended Operating Condition

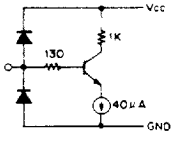
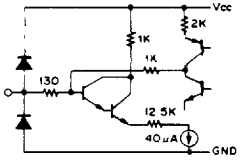
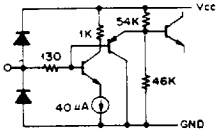
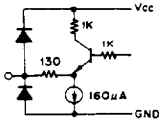
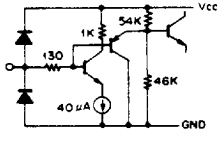
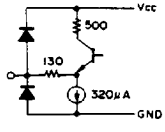
• Supply voltage	Vcc	4.75 to 5.25	V

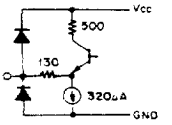
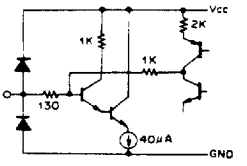
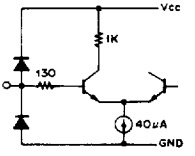
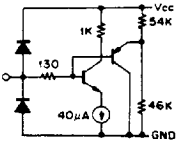
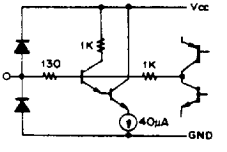
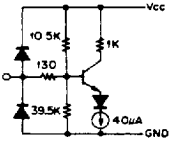
Block Diagram and Pin Configuration

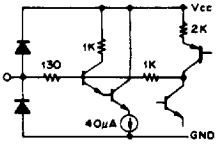
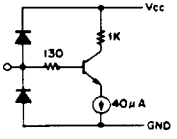
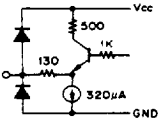
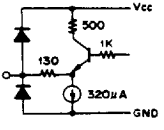
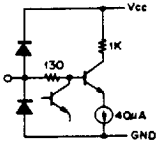
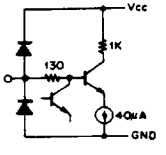
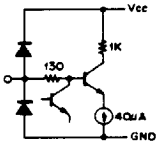


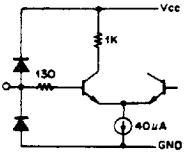
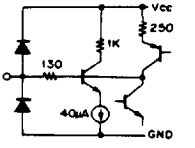
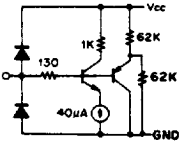
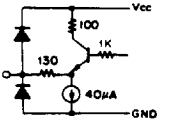
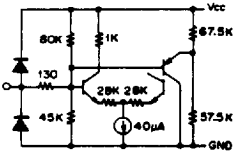
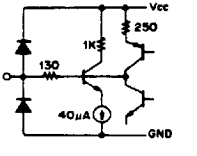
Pin Description

No.	Symbol	Voltage	Equivalent circuit	Description
1	Y GAIN	3.0V		Gain control pin for the signal input to Y Y 1IN. 1.8V (Min.) to 5.0V (Max.)
2	Y_L IN	3.4V		Y_L input, which is clamped by the input connected to the capacitor. 250mV (Typ.)
3	AGC MIX	3.0V		Y_M factor (Y_L/Y_H ratio) control. 3.0V (Y_L) to 4.0V (Y_H)
4	Y_L-Y_H OUT	2.9V		Y_L-Y_H signal and V aperture signal output pin. Black level 3V. If the 47 pin OFFSET pin is set to GND in test mode, Y_M signal (that has mixed Y_L and Y_H) is output.
5	Y_H OUT	2.2V		Y_H output. 1000mV (Typ.), 1300mV (Max.) Black level 2.4V
6	AP GAIN	3V		V aperture gain control. 1.8V (Max.) to 5.00V (OFF)

No.	Symbol	Voltage	Equivalent circuit	Description
7	AP SLICE	3V		V aperture slice level control. 1.8V (Min.) to 5.0V (Max.)
8	AP-C	3.7V		Pin that connects the V aperture signal capacitor CLP capacitor
9	VCS GAIN	3V		Chroma suppress signal level control with V aperture. 1.8V (Min.) to 5.0V (Max.) GND : OFF
10	CSY OUT	2.1V		Chroma suppress signal output.
11	CS GAIN	3V		Chroma suppress signal level control with Y signal. 1.8V (Min.) to 5.0V (Max.) GND : OFF
12 13 15	B OUT G OUT R OUT	1.9V 1.9V 1.9V		R, G, B output pin. Black level 1.9V. If the 21-pin B MTX pin is set to GND in test mode, each pin outputs a signal as shown below. R OUT ··· C_R signal B OUT ··· C_B signal G OUT ··· Y signal The C_R, C_B, and Y signal are provided before the matrix.

No.	Symbol	Voltage	Equivalent circuit	Description
14	DC OUT	1.9V		DC output of 1.9V that is equivalent to R, G, B OUT black level.
16 17 18	R-C G-C B-C	3.2V 3.3V 3.3V		Pin that is connected to the R, G, B OUT clamping capacitor.
19	GND	0V		
20	ID			Inverted pulse is input every 1H. The C1 signal is output to B OUT for HI. The C1 signal is output to R OUT for LOW. V_{TH} = 2.5V
21 22	B MTX R MTX	3V 0V		Matrix factor control for B and R. 1.8V (Max.) to 3.9V (Min.) In test mode : B MTX : C_R/C_B mode with GND R MTX : MTX preset mode with GND
23 24	M_1-C M_0-C	3.0V 3.0V		M_1-C : Connects the 1H line chroma signal clamping capacitor. M_0-C : Connects the 0H/2H line chroma signal clamping capacitor.
25	APCUT	3.95V		Controls the level that suppresses the V aperture signal. Internally biased to 3.95V in preset mode.

No.	Symbol	Voltage	Equivalent circuit	Description
26	Y_1-C	3.0V		Pin that connects the 1H line Y signal clamping capacitor.
27 32 37	C_2- GAIN C_1- GAIN Y_1- GAIN	3V 3V 3V		C_1, C_2, Y_1 signal gain control. 1.8V (Min.) to 5.0V (Max.)
28 29	Y_1 OUT Y_0 OUT	2.6V 2.6V		1H/0H line Y signal output. Inverted output 200mV (Typ.)
30 31	C_1 OUT C_0 OUT	2.6V 2.6V		1H/0H line chroma signal output. Inverted output ± 100mV (Typ.)
33 34	DLC_2 IN DLC_1 IN	2.9V 2.9V		2H/1H line chroma signal input. Positive phase input ± 75mV (Typ.)
35 36	DLY_2 IN DLY_1 IN	2.9V 2.9V		2H/1H line Y signal input. Positive phase input 150mV (Typ.)
38 39	S_1 IN S_2 IN	3.3V 3.3V		S_1/S_2 signal input. 500mV (Typ.) 1500mV (Max.)

No.	Symbol	Voltage	Equivalent circuit	Description
40	Vcc	5V		Vcc
41 42	CLP0 CLP2	5V 0V 5V 0V		Clamp pulse input V_{TH} = 2.5V
43	GND	0V		GND
44	Y IN	2.7V		Y signal input. 220mV (Typ.) 660mV (Max.)
45	γ	0V		γ curve control. 1.8V to 5.0V GND : Preset
46	$Y_{\gamma 0}$ OUT	3.0V		Yγ signal output. Inverted output 400mV (Typ.) 520mV (Max.)
47	OFFSET	1.8V		γ offset control. 1.8V to 5.0V If the pin is set to OPEN, bias to 1.8V is internally performed. If the pin is set to GND in test mode, the Y_M signal is output from the 4 pin, Y_L-Y_H OUT pin.
48	$Y_{\gamma 1}$ IN	2.9V		1H line Yγ signal output. 150mV (Typ.)

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{CC}	Vcc=5V	20	33	45	mA
S_1, S_2 LPF	$F_{S1, S2}$	4.77MHz gain for ㊳ S_1IN→㉓ Y_0OUT 300kHz	−28	−20	−11	dB
S_1-Y_0 gain	$G_{S1\text{-}Y0}$	㊳ S_1IN→ ㉓ Y_0OUT gain	−14.2	−13.0	−11.8	dB
Gain difference between S_1 -Y_0 and S_2-Y_0	ΔG_{Y0}	Gain difference between ㊳ S_1IN→㉓ Y_0OUT and ㊴ S_2IN→ ㉓ Y_0OUT	−0.7	0	0.7	dB
S_1-C_0 gain	$G_{S1\text{-}S0}$	㊳ S_1IN→㉛ C_0OUT gain	−3.2	−1.9	−0.8	dB
Gain difference between S_1-C_0 and S_2-C_0	ΔG_{C0}	Gain difference between ㊳ S_1IN→ ㉛ C_0OUT and ㊴ S_2IN→㉛ C_0OUT	−0.7	0	0.7	dB
Y_1 gain Min.	G_{Y1}Min.	㊱ DLY1IN→㉘ Y_1OUT gain ㉗ Y_1GAIN=1.8V	−	−2.5	−1.3	dB
Y_1 gain Max.	G_{Y1}Max.	㊱ DLY1IN→㉘ Y_1OUT gain ㉗ Y_1GAIN=5V	8.8	12.0	−	dB
C_1 gain Min.	G_{C1}Min.	㉞ DLC1IN→㉚ C_1OUT gain ㉜ C_1GAIN=1.8V	−	−2.5	−1.3	dB
C_1 gain Max.	G_{C1}Max.	㉞ DLC1IN→㉚ C_1OUT gain ㉜ C_1GAIN=5V	8.8	12.0	−	dB
C_2 gain Min.	G_{C2}Min.	㉞ DLC1IN→⑮ ROUT GAIN that is twice as much as ㉝ DLC2IN →⑮ ROUT, ㉑ BMTX=GND, ⑳ ID=GND, ㉗ C_2GAIN=1.8V for ㉑ BMTX=GND, ID=5V⑳	−	−2.8	−1.3	dB
C_2 gain Max.	G_{C2}Max.	㉞ DLC1IN→⑮ ROUT Gain that is twice as much as ㉝ DLC2IN →⑮ ROUT, ㉑ BMTX=GND, ⑳ ID=GND, ㉗ C_2GAIN=1.8V for ㉑ BMTX=GND, ⑳ ID=5V	8.8	12.0	−	dB
Y_2 gain Min.	G_{Y2}Min.	Ratio of the output of ㉟ DLY2IN (200mV) →④ Y_L-Y_HOUT, ㊲ Y_1GAIN=1.8V to the output of ㊱ DLY_1IN (100mV) → ④ Y_L-Y_HOUT, ㊲ Y1GAIN=1.8V	−1.4	0	1.4	dB
Y_2 gain HI	G_{Y2}Max.	Ratio of the output of ㉟ DLY2IN (100mV) →④ Y_L-Y_HOUT, ㊲ Y_1GAIN=1.8V to the output of ㊱ DLY_1IN (50mV) → ④ Y_L-Y_HOUT, ㊲ Y GAIN=3.9V	−1.4	0	1.4	dB
C_0 LPF	F_{C0}	4.77MHz gain for ㉝ DLC2IN→⑮ ROUT, ⑳ ID=GND, 300kHz	−28	−18	−8	dB
C_1 LPF	F_{C1}	4.77MHz gain for ㉞ DLC2IN→⑮ ROUT, ⑳ ID=5V, 300kHz	−28	−18	−8	dB

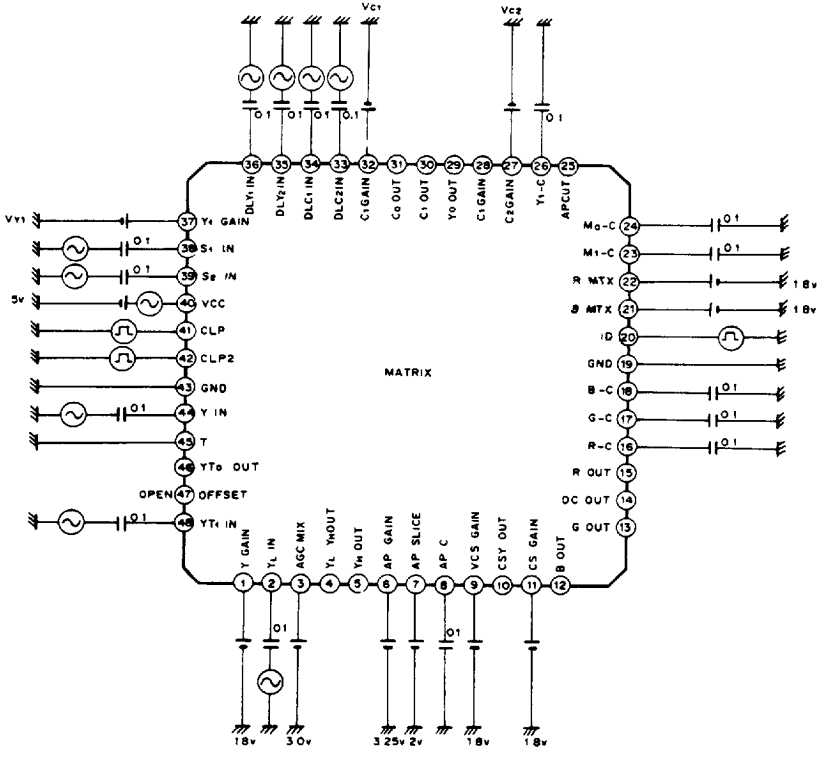
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Y_1 LPF	F_{Y1}	4.77MHz gain for ㊱ DLY1 IN→⑬ GOUT, 300kHz	−28	−18	−8	dB
V apperture LPF	F_{AP}	4.77MHz gain for ㊱ DLY_1 IN→ ④ Y_L-Y_H OUT, 300kHz	−28	−18	−8	dB
DLY_1 → Y_L-Y_H gain	G_{DLY1}	㊱ DLY1 IN (100mV) →④ Y_L-Y_H OUT gain ⑥ APGAIN=3.25V	6	8.3	11	dB
V aperture level Max.	G_{AP}Max.	㊱ DLY_1 IN (30mV) →④ Y_L-Y_H OUT Output level ratio for ⑥ APGAIN=3.25V to 1.5V	8	11	−	dB
V aperture slice Mid.	V_{APS} Mid.	㊱ DLY_1 IN (100mV) →④ Y_L-Y_H OUT Output level difference between ⑦ APSLICE=2V and 3V	85	120	155	mV
V aperture cutting input level	V_{APCUT}	㊱ DLY1 IN input level when the ④ Y_L-Y_H OUT output is cut ⑥ APGAIN=1.5V	225	260	295	mV
Chroma suppress Y output level Max.	V_{CSY} Max.	㊱ DLY_1 IN (350mV) →⑩ CSYOUT ⑨ VCSGAIN=GND, ⑪ CSGAIN=1.8V	400	760	−	mV
Chroma suppress Y gain Min.	G_{CSY} Min.	㊱ DLY_1 IN (350mV) →⑩ CSYOUT ⑨ VCSGAIN=GND Output level ratio for ⑪ CSGAIN=5V to 1.8V	−14.2	−12.0	−10.8	dB
Chroma suppress VAP level Max.	V_{CSVAP} Max.	㊱ DLY_1 IN (50mV) →⑩ CSYOUT ⑪ CSGAIN=GND, ④ VCSGAIN=5V	740	920	−	mV
Chroma suppress VAP gain Min.	G_{CSVAPM} Min.	㊱ DLY_1 IN (50mV) →⑩ CSYOUT ⑪ CSGAIN=GND Output level ratio for ⑨ VCSGAIN=5V to 1.8V	−14.2	−12.0	−9.3	dB
C_R gain	G_{CR}	㉞ DLC_1 IN→⑮ ROUT gain ㉒ RMTX=GND	3.6	5.3	7.0	dB
RMTX Y factor presetting	K_{RY}	㉞ DLC_1 IN (100mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㊱ DLY IN (220mV) →⑮ ROUT, ⑳ ID=5V ㉑ RMTX=GND output level set to V_2 (V_2/V_1) ×1/8 is calculated.	0.094	0.12	0.131	V/V
C_B gain	G_{CB}	㉞ DLC_1 IN→⑫ BOUT gain ⑳ ID=GND, ㉒ RMTX=GND	3.6	5.3	7.0	dB
BMTX Y factor presetting	K_{BY}	㉞ DLC_1 IN (100mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_1 ㊱ DLY_1 IN (220mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_2 (V_2/V_1) ×1/8 is calculated.	0.173	0.20	0.222	V/V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BMTX C_R factor	K_{BCR}	㉞ DLC1 IN (100mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_1 ㉞ DLC1 IN (100mV) →⑫ BOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_2 V_2/V_1	0.173	0.20	0.222	V/V
Y_1 gain	G_{Y1}	㊱ DLY1 IN→⑬ GOUT gain ⑳ ID=5V, ㉒ RMTX=GND	6.6	8.3	10.0	dB
GMTX C_R factor	K_{GCR}	㊱ DLY1 IN (220mV) →⑬ GOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㉞ DLC1 IN (100mV) →⑬ GOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_2 $V_2/V_1 \times 8$	0.78	1.0	1.22	V/V
GMTX C_B factor	K_{GCB}	㊱ DLY1 IN (220mV) →⑬ GOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㉞ DLC1 IN (100mV) →⑬ GOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_2 $V_2/V_1 \times 8$	0.78	1.0	1.22	V/V
RMTX Y factor HI	K_{RYMI}	㉞ DLC1 IN (100mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㊱ DLY1 IN (220mV) ⑮ ROUT, ⑳ ID=5V ㉒ RMTX=1.8V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.192	0.225	0.253	V/V
BMTX Y factor LOW	K_{RYLO}	㉞ DLC1 IN (100mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㊱ DLY1 IN (220mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=3.9V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.042	0.056	0.070	V/V
BMTX Y factor HI	K_{BYMI}	㉞ DLC1 IN (100mV) →⑫ BOUT, ⑳ ID=GMD ㉒ RMTX=GND output level set to V_1 ㊱ DLY1 IN (220mV) →⑫ BOUT, ⑳ ID=GND ㉑ BMTX=1.8V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.337	0.380	0.413	V/V
RMTX Y factor LOW	K_{BYLO}	㉞ DLC1 IN (100mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_1 ㊱ DLY1 IN (220mV) →⑫ BOUT ⑳ ID=GND ㉑ BMTX=3.9V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.068	0.09	0.117	V/V
DC OUT DC	V_{CC}	⑭ DCOUT pin voltage	1.73	1.85	1.97	V
R, G, B OUT offset	V_{RGBO}	Potential difference between ⑮ ROUT/ ⑬ GOUT, ⑫ BOUT and ⑭ DCOUT	−10	0	10	mV
Y preset standard level	$V_{Y\,PRE}$	㊹ YIN (220mV) →㊻ Y Y OUT	365	410	455	mV

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
γ preset curve	$G_{\gamma PPE}$	Ratio of ㊶ YIN (55mV) →㊺ Y γ OUT output level to ㊶ YIN (220mV) → ㊺ Y γ OUT output level	−8.2	−7.0	−5.8	dB
Y_H OUT DC	$V_{\gamma HOUT}$	⑤ Y_HOUT pin voltage	2.0	2.3	2.6	V
Y_H gain Min. (Y_H OUT)	G_{YH}Min1	㊸ Y γ1IN→⑤ Y_HOUT gain ① YGAIN=1.8V ③ AGCMIX=4V ㊼ OFFSET=GND	–	10	12.2	dB
Y_H gain Max. (Y_H OUT)	G_{YH}Max1	㊸ Y γ1IN→⑤ Y_HOUT gain ① YGAIN=5V ③ AGCMIX=4V ㊼ OFFSET=GND	20.8	23.0	–	dB
Y_L-Y_H OUT DC	V_{YL}OUT	Y_L-Y_H pin voltage	2.6	2.9	3.2	V
Y_H gain Min. (Y_L-Y_H OUT)	G_{YH}Min2	㊸ Y γ1IN→④ Y_L-Y_H OUT gain ① YGAIN=1.8V ③ AGCMIX=4V ㊼ OFFSET=GND	–	2.1	4.2	dB
Y_H gain Max. (Y_L-Y_H OUT)	G_{YH}Max2	㊸ Y γ1IN→④ Y_L-Y_H OUT gain ① YGAIN=5V ③ AGCMIX=4V ㊼ OFFSET=GND	12.8	15.0	–	dB
Y_L gain	G_{YL}	② Y_LIN→④ Y_L-Y_H OUT gain ③ AGCMIX=3V	4.3	6.0	7.7	dB

Electrical Characteristics Test Circuit

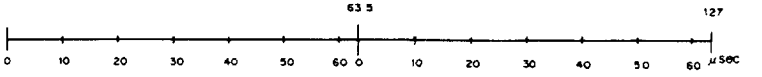
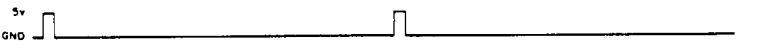
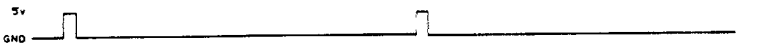
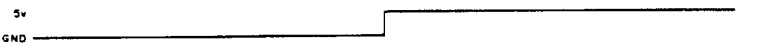
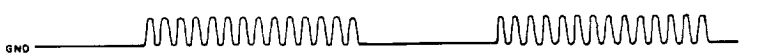
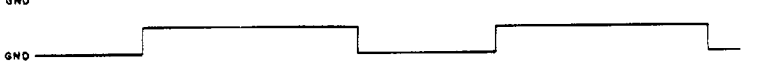
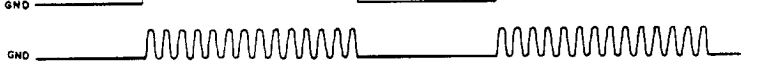
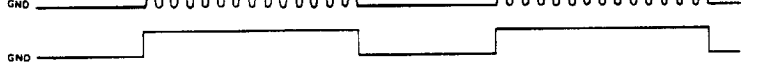
Standard setting conditions



Note)

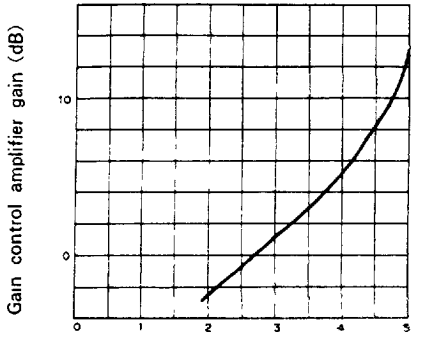
1. Conditions only that are different from standard setting conditions are described.
2. Adjust V_{C1}, V_{C2}, and V_{Y1} so that the signal levels will be equivalent between DLC_1IN and C_1OUT, DLC_2IN and between DLY_1IN and Y_1OUT.
3. Signal sources other than ID, CLP0, and CLP2 are not input in standard setting but set to GND.
4. If measurement conditions specify ID=5V and ID=GND, measure at the ID=5V timing and ID=GND timing.

Input Signal Timing Chart

Pin	Input signal
	
41 CLPO	
42 CLP2	
20 ID	
38 S_1 IN	
39 S_2IN	
36 DLY_1 IN	
35 DLY2 IN	
34 DLC_1 IN	
33 DLC2 IN	
44 YIN	
48 Y_{Y1} IN	

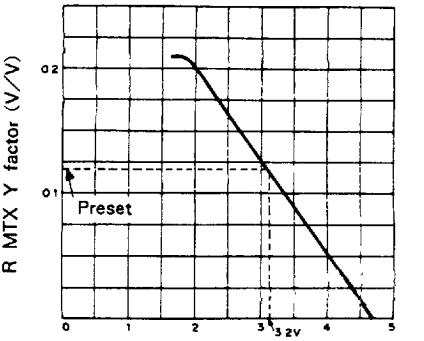
Note) 1. The signal level and frequency are listed in another table.
2. The sine wave intermittent signal is used for measurement of LPF characteristics

Delay line gain control amplifier characteristics



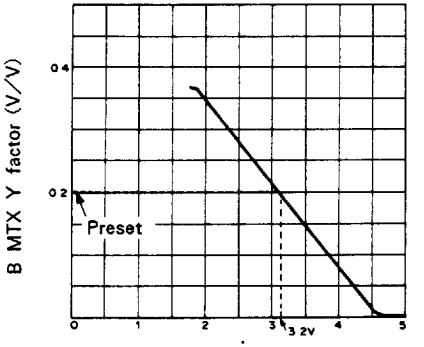
37, 32, 27 pins Y_1, C_1, C_2GAIN pins (Y)

R MTX control characteristics (Y factor)



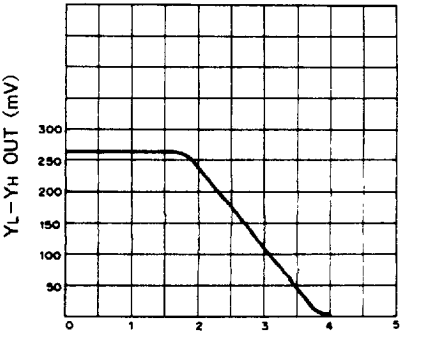
22 pin RMTX (V)

B MTX control characteristics (Y factor)



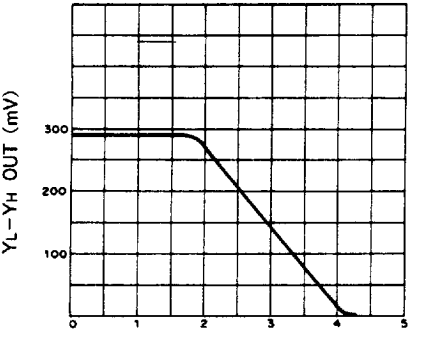
21 pin BMTX (V)

AP GAIN control characteristics



6 pin AP GAIN (V)

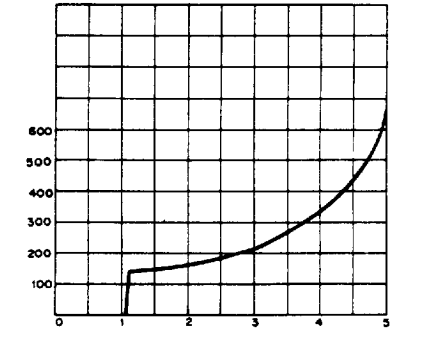
AP SLICE control characteristics



7 pin AP SLICE (V)

(6 pin AP GAIN=3.25V
Input pin 36 DLY1IN 100mV)

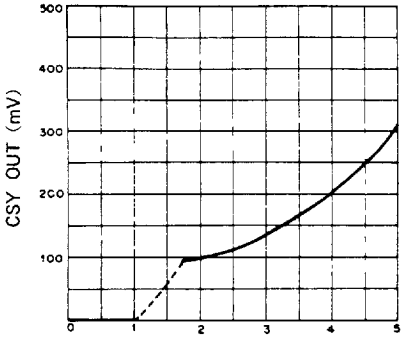
CSY GAIN control characteristics



11 pin CS GAIN (V)

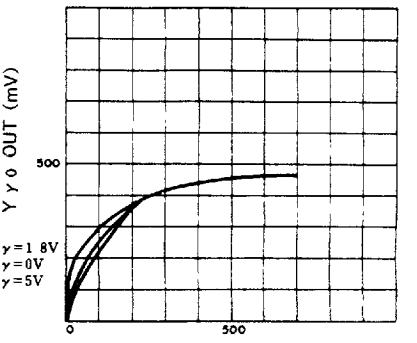
(Input pin 36 DLY1IN=350mV)

CSY VAP control characteristics



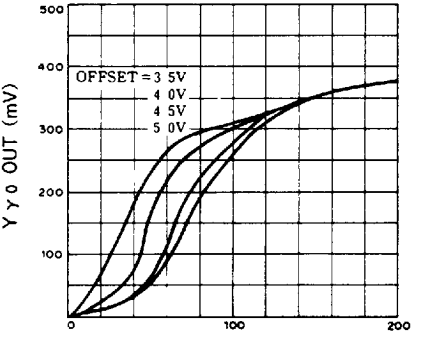
9 pin VCS GAIN pin (V)
(Input pin 36 DLY1IN=50mV)

γ control characteristics



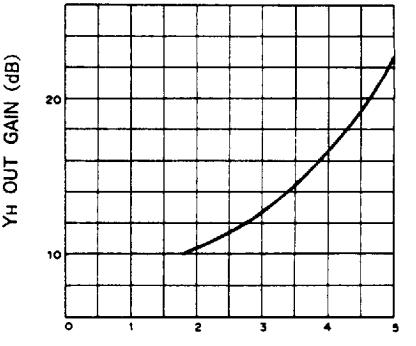
44 pin YIN input level (mV)

γ OFFSET control characteristics (γ = 1.8V)



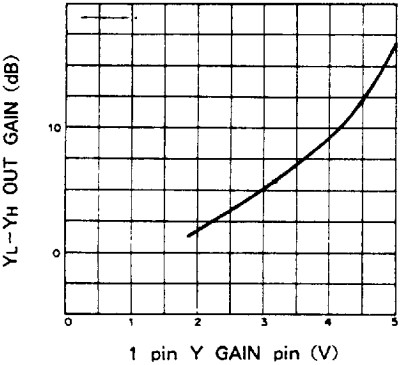
44 pin YIN input level (mV)

YH GAIN control characteristics



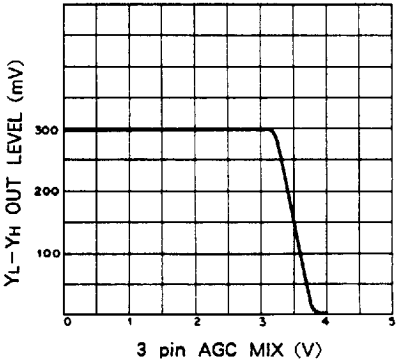
1 pin Y GAIN pin (V)

YM GAIN control characteristics



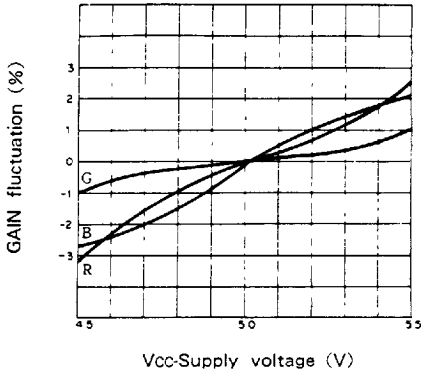
1 pin Y GAIN pin (V)

YL MIX control characteristics

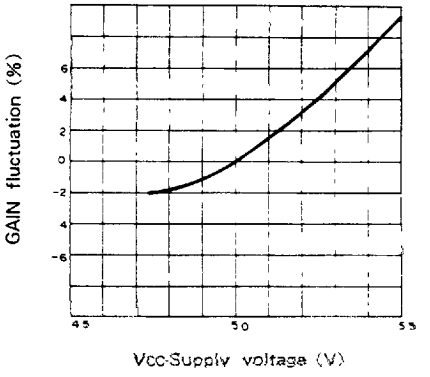


3 pin AGC MIX (V)

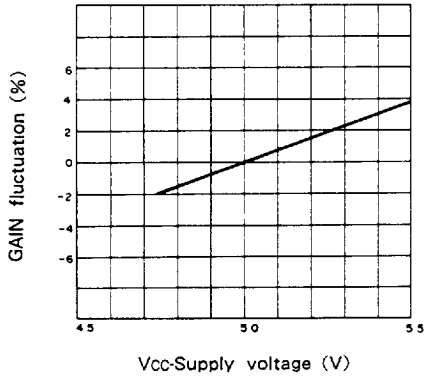
S1, S2, Y-R, G, B GAIN Vcc characteristics



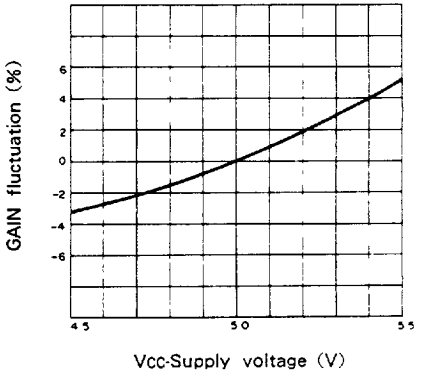
YIN–YH GAIN Vcc characteristics



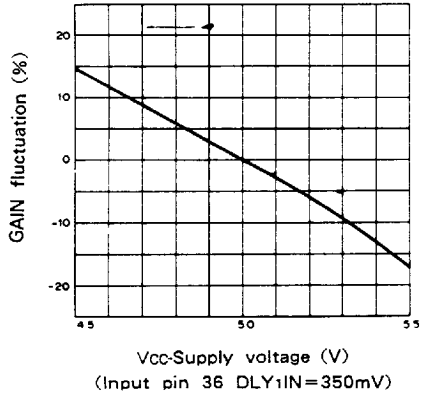
YIN–YL-YH GAIN Vcc characteristics



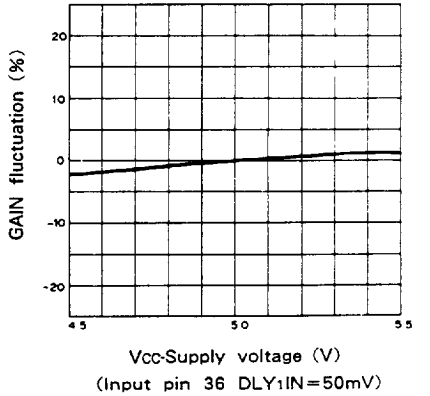
YIN–YL GAIN Vcc characteristics



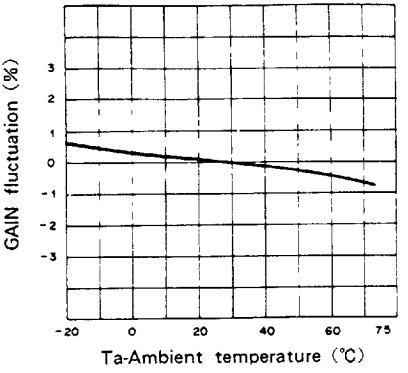
CSY GAIN Vcc characteristics



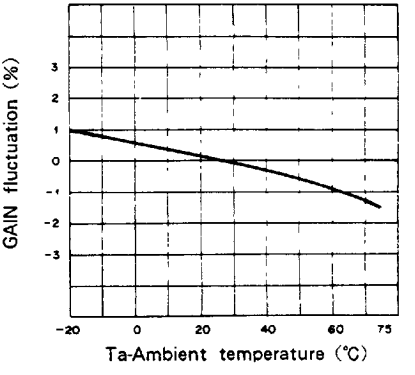
VCS GAIN Vcc characteristics



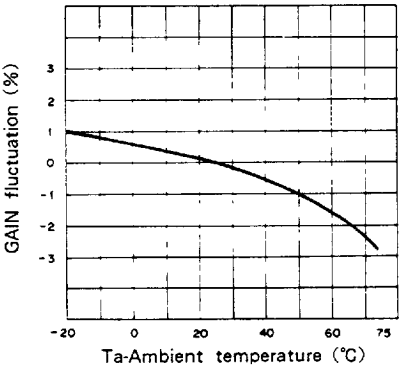
S_1, S_2 IN → C_0, Y_0 OUT Gain temperature characteristics



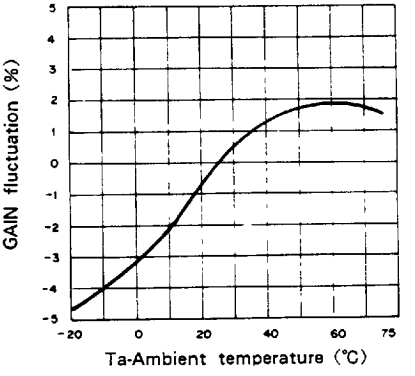
DLY_1, DLC_1 IN → Y_1, C_1 OUT gain temperature characteristics (0dB)



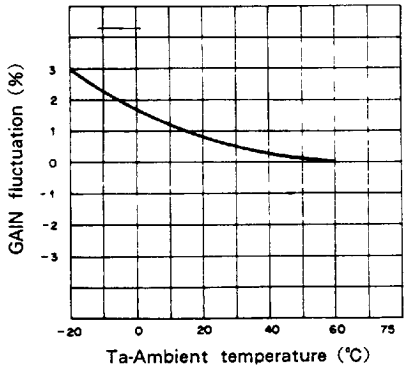
DLC_1 IN → R, B OUT gain temperature characteristics



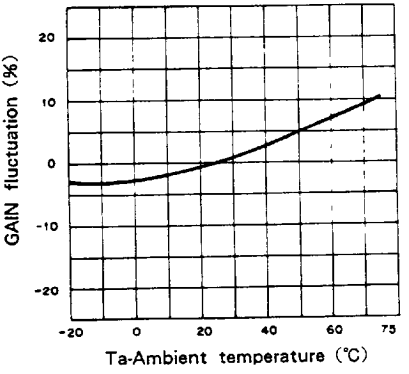
Y IN (220mV) → Y_Y OUT gain temperature characteristics



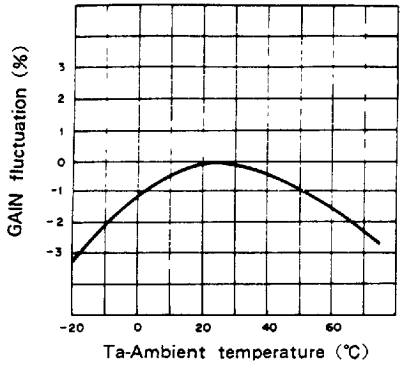
Y_{Y1} IN → Y_H OUT gain temperature characteristics



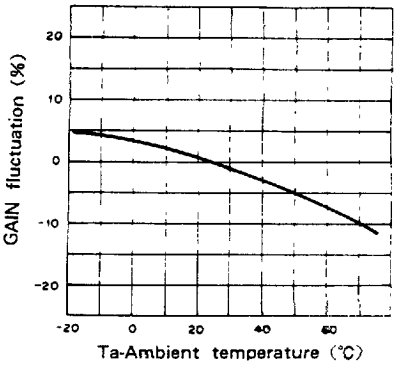
DLY_1 IN → Y_L - Y_H OUT aperture gain temperature characteristics



DLY1 IN (350mV) → YL - YH OUT CSY temperature characteristics.



DLY1 IN (50mV) → YL - YH OUT CSY VAP temperature characteristics.



Operation

CXA1151 is an IC that outputs RGB, YL - YH, YH, and CSY from the signal that sampled and held the complementary color checker coding imager.

1. S1 and S2 input → RGB OUT

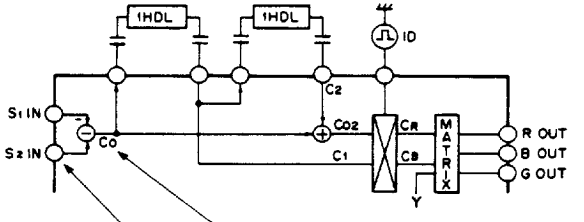


Table-1 Imager coding

Mg	G	Mg	G	0H
Ye	Cy	Ye	Cy	
G	Mg	G	Mg	1H
Ye	Cy	Ye	Cy	
Mg	G	Mg	G	2H
Ye	Cy	Ye	Cy	
S_2	S_1	S_2	S_1	

Table-2 Chroma signal

	0H(C_0)	1H(C_1)	2H(C_2)
C	2R−G	−(2B−G)	2R−G

Table-3 S1 and S2 signals

	0H	1H	2H
S_1	G+Cy	Mg+Cy	G+Cy
S_2	Mg+Ye	G+Ye	Mg+Ye

1) Imager
The coding imager shown in Table-1 is used.

2) S1 and S2 inputs
The signals that sampled and held the imager output are input. By using the imager shown in Table-1, field reading is performed to obtain signals shown in Table-3. G+Cy and G+Ye, or Mg+Ye and Mg+Cy are alternately input to S1 and S2 every hour.

3) Chroma signal
The chroma signal (C) is acquired from S_2 - S_1. As shown in Table-2, a signal that alternates 2R-G and 2B-G is obtained.

4) C_{02} and C_1 signals
To make the RGB signal in the matrix circuit, 2R-G and 2B-G are required at the same time. By using 1HDL, signal C_1 that 1 hour behind and signal C_2 that is 2 hours behind are created. By averaging C_0 and C_2 with the same period as 2B-G of C_1, 2R-G is created.

5) Multiplexing
2R-G and 2B-G are alternately sent every hour to C_1 and C_{02}, so 2R-G (C_R) and 2B-G (C_B) are separated by the ID pulse that inverts "L" to "H", or vice versa every 1 hour.

6) Matrix
RGB is made from C_R, C_B, and Y. The theoretical formulae shown below are applied.
$R = C_R + 0.12Y$
$B = -C_B + 0.20\ (Y - C_R)$
$G = Y - C_R + C_B$
Coefficients, 0.12 and 0.20, are adjustable. (RMTX and BMTX Pins)

7) RGB output
The RGB output is a clamped output. The clamped DC is output to the DC pin. From the R OUT, B OUT, and G OUT pins, the C_R, C_B, and Y signals to be fed to the matrix can be output.

2. Y IN, Y_L IN → Y_L - Y_H OUT
As Y_L that is output from Y_L - Y_H OUT, ② Y_L signal and ㊹ Y IN signal can be linearly switched with ③ AGC MIX pin of the MIX amplifier.

1) Y IN signal
$Y = Mg + G + Ye + Cy$ ((f_3) out of CXA1337), as the AGC output, is input.

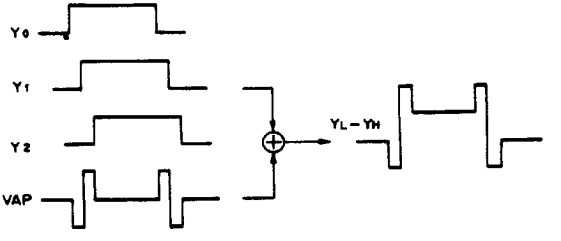
2) γ
The γ curve is adjustable, and presetting is available.

3) OFFSET
It is used in the negative mode. If GND is set, the output of the MIX amplifier comes out of Y_L - Y_H OUT. (For adjustment)

4) Y_L - Y_H OUT
By controlling the AGC MIX Pin, α (Y_L IN - Y IN) ($0 \leqq \alpha \leqq 1$) is output. The aperture signal is added and output.

3. V aperture signal
The V aperture signal is synthesized from $\frac{Y_0 + Y_2}{2} - Y_1$

The signal is made at a ratio of 1 : 1 between plus and minus.



After aperture signal VAP is synthesized, the signal whose level around noise is sliced and controlled by the aperture slicing circuit is added to the Y_L - Y_H signal.

The aperture signal is not output when the Y signal exceeds a reference level.

That reference level has been preset but it can be adjusted with ㉕ AP CUT Pin.

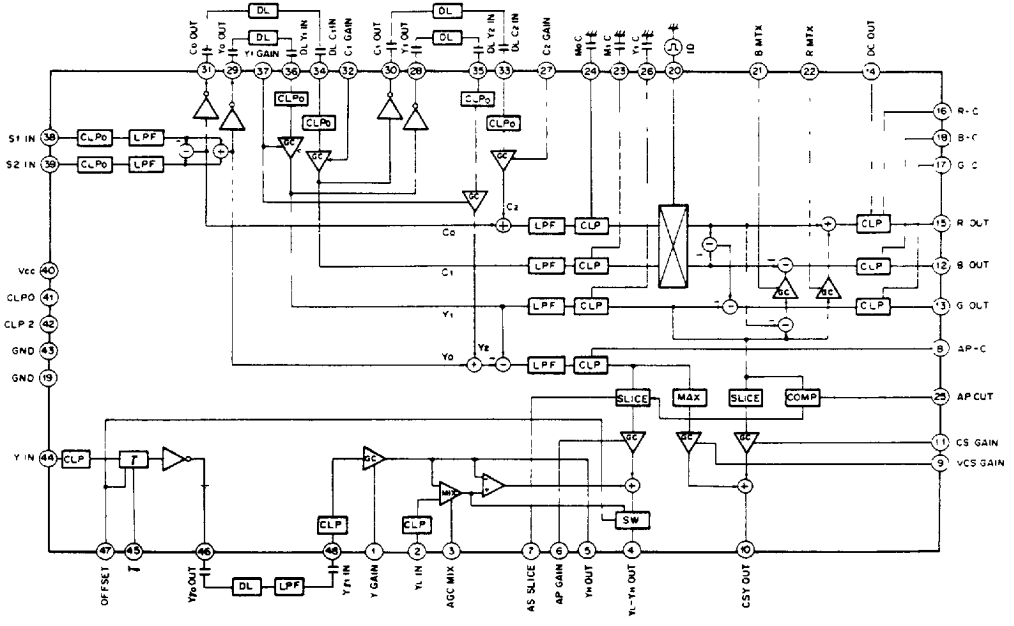
If ㉕ AP CUT is set to GND, the aperture signal is not output at all.

4. Chroma suppressing Y signal

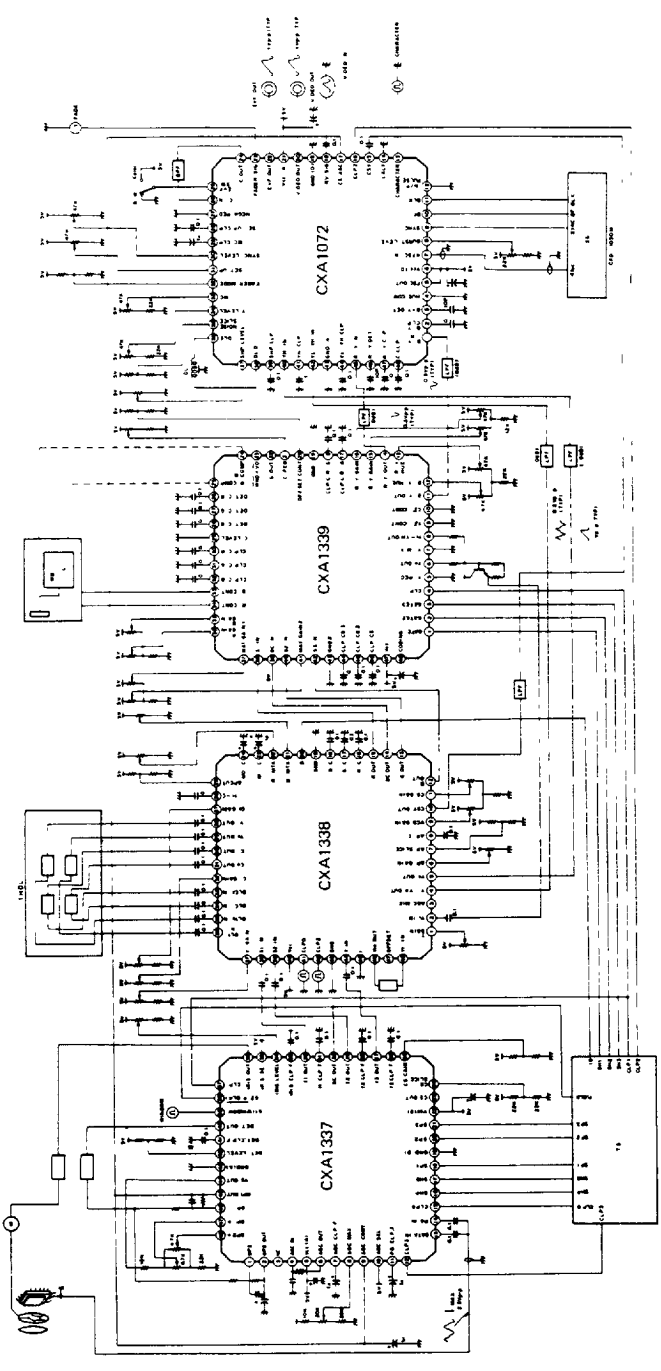
Depending on the Y signal level, a signal that suppresses the chroma signal is output.

The chroma suppressing Y (CSY) signal is made by mixing the following two signals.

1) The amount of the Y signal exceeding a reference level (1.2 times of the reference signal) is output.
   The sliced amount is fixed. After slicing, the signal is gain-controlled and output.
2) The absolute value of the aperture signal is output as the CSY signal.



Application Circuit



- It is recommended to set the resistance with no value indicated to 50k Ω and below between Vcc and GND.
- Unspecified capacity unit is μF