

SONY**CXA1496AQ****10-bit 20MSPS A/D Converter****Description**

The CXA1496AQ is a 10-bit 20MSPS 2-step parallel type A/D converter for video signal processing.

This A/D converter operates on a dual $\pm 5V$ power supply. The external addition of sample and hold, reference power supply and clock timing circuits permit the conversion of analog signals into digital signals.

Features

- Maximum operating frequency 20MHz (Min.)
- Integral linearity error 10-bit $\pm 1.5LSB$
- Differential linearity error 10-bit $\pm 1LSB$
- Low power consumption 310mW (Typ.)
- Wide band analog input 10MHz
- Low input capacity 150pF (Typ.)
- Built-in digital correction
(Compensation within a range of $\pm 16LSB$)
- TTL input (CLK only: ECL LIKE)
- TTL output (3-state control)
- Output code Binary/2S complement/
1S complement

48 pin QFP (Plastic)

**Function**

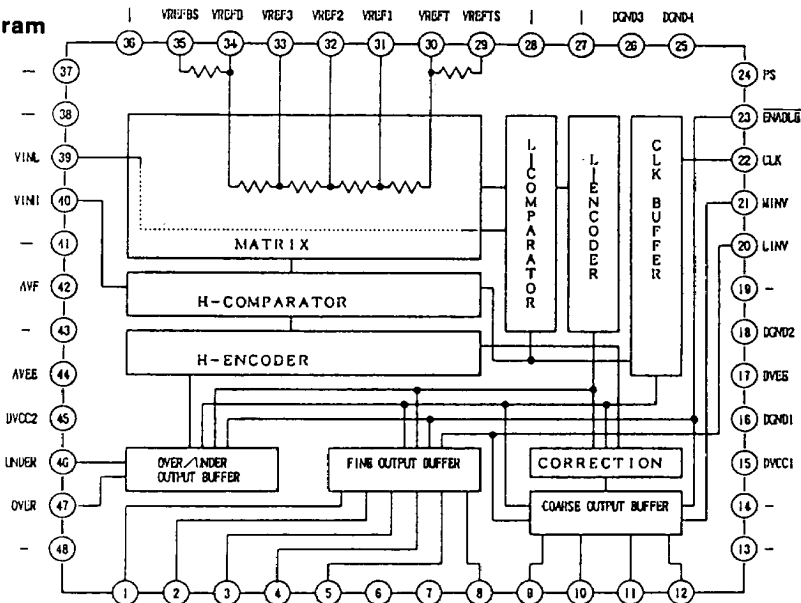
10-bit 20MSPS 2-step parallel type A/D converter

Structure

Bipolar silicon monolithic IC

Applications

High resolution video signal processing

3**Block Diagram**

Absolute Maximum Ratings (Ta=25°C)

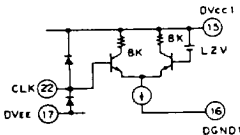
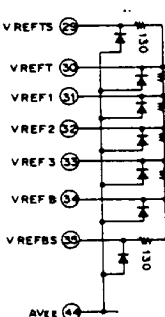
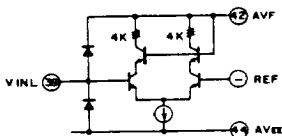
• Supply voltage	DVcc1	0 to +6	V
	DVcc2	0 to +6	V
	AVEE	0 to -6	V
	DVEE	0 to -6	V
• Analog input voltage	VINH	AVEE to AGND+0.3	V
	VINL	AVEE to AGND+0.3	V
• Reference voltage	VRT	AVEE to AGND+0.3	V
	VRB	AVEE to AGND+0.3	V
• Digital input voltage	CLK	DGND1-0.5 to DVcc1	V
	MINV	DGND1-0.5 to DVcc1	V
	LINV	DGND1-0.5 to DVcc1	V
	PS	DGND1-0.5 to DVcc1	V
	ENABLE	DGND1-0.5 to DVcc1	V
	Tstg	-65 to 150	°C

Operating Conditions

		Min.	Typ.	Max.	Unit
• Supply voltage	DVcc1	+4.75	+5	+5.25	V
	DVcc2	+4.75	+5	+5.25	V
	DGND1		0		V
	DGND2		0		V
	DGND3		0		V
	DGND4		0		V
	AVF	+0.5	+0.7	+0.9	V
	AVEE	-5.25	-5	-4.75	V
	DVEE	-5.25	-5	-4.75	V
	VINH	-2		0	V
• Analog input voltage	VINL	-2		0	V
	VRT	-0.1	0	+0.1	V
• Reference voltage	VRB	-2.1	-2.0	-1.9	V
• Digital input voltage (MINV, LINV, PS, ENABLE)	DIN (H)	+2			V
	DIN (L)			+0.5	V
	DIN(H)	DVcc1-1	DVcc1-0.8		V
• Digital input voltage (CLK)	DIN(L)		DVcc1-1.6	DVcc1-1.4	V
					V
• Clock width	t _{PWH}	25			ns
	t _{PWL}	25			ns
• Operating temperature	Topr	-20		+75	°C

Pin Description

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
1 to 5 8 to 12	D0 to D9	O	TTL		Digital output pins D0 (LSB) to D9 (MSB)
46	UNDER	O			Underflow output pin
47	OVER	O			Overflow output pin
15	DVcc1	—	+5V (Ratings)		Digital power supply
45	DVcc2	—			
16	DGND1	—	GND		Digital ground
18	DGND2	—			
26	DGND3	—			
25	DGND4	—			
17	DVEE	—	-5V		Digital negative power supply
44	AVEE	—			Analog negative power supply
20	LINV	I	TTL		This input pin can invert the form of the output from D0 (LSB) to D8. In open condition this pin turns to High level input. (For details, refer to the output formula chart.)
21	MINV	I	TTL		This input pin can invert the form of the output from D9 (MSB). In open condition this pin turns to High level input. (For details, refer to the output formula chart.)
23	ENABLE	I	TTL		3-state control pin. Turns to enable when low is input. In open condition this pin turns to High level input.
24	PS	I	TTL		Power save input pin. In open condition this pin turns to High level input.

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description	
22	CLK	I	ECL LIKE		Clock input pin	
29	VREFTS	—	GND		Reference voltage sense pin (Top)	
30	VREF	I			Reference voltage force pin (Top)	
31	VREF1	—	-0.5V			
32	VREF2	—	-1.0V			
33	VREF3	—	-1.5V			
34	VREFB	I	-2V		Reference voltage force pin (Bottom)	
35	VREFBS	—			Reference voltage sense pin (Bottom)	
39	VINL	I	-2V to 0V		Analog input pin (Lower comparator input pin)	

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
40	VINH	I	-2V to 0V		Analog input pin (Upper comparator input pin)
42	AVF	—	+0.7V		Analog power supply

Electrical Characteristics

(Ta=25 °C, DVcc1, 2=5V, DGND1 to 4=0V, AVF=0.7V, AVEE, DVEE=-5V, VRB=-2V, VRT=0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit		
Resolution	n		10	10	10	bit		
DC characteristics								
Integral linearity error	E _{IL}	F _C =20MSPS	1.5		1.5	LSB		
Differential linearity error	E _{DL}	V _{IN} =0 to -2V	-1		+1	LSB		
Analog input								
Analog input current	I _{IN}	V _{IN} =0	0	25	100	μA		
Analog input capacity	C _{IN}	V _{IN} =-1V+0.07V _{rms}		150		pF		
Analog input band width	BW	-1dB down		10		MHz		
Reference voltage input								
Reference current	I _{REF}		8	10	12	mA		
Reference resistance	R _{REF}		160	200	240	Ω		
Offset voltage	E _{OT}		3	13	23	mV		
	E _{OB}		2	12	22	mV		
Reference voltage 1	V _{REF1}		-0.55	-0.5	- 0.45	V		
Reference voltage 2	V _{REF2}		-1.05	-1.0	- 0.95	V		
Reference voltage 3	V _{REF3}		-1.55	-1.5	- 1.45	V		
Digital input								
Digital input voltage H	V _{IH}		2			V		
Digital input voltage L	V _{IL}				0.5	V		
Digital input current 1H	I _{IH1}	* 1	D _{VCC1} Max.	V _{IH} =D _{VCC1} -0.8V	-10	0.5	+10	μA
Digital input current 1L	I _{IL1}			V _{IL} =D _{VCC1} -1.6V	-1	0	+1	μA
Digital input current 2H	I _{IH2}	* 2		V _{IH} =2.7V	-10	0	+10	μA
Digital input current 2L	I _{IL2}			V _{IL} =0.5V	-20	-10	0	μA
Digital input capacity				5			pF	

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Switching characteristics						
Max. operating frequency	Fc		20			MSPS
Pulse width H	tpWH	* 3	25			ns
Pulse width L	tpWL		25			ns
Sampling delay TS1	tsH			4		ns
Sampling delay TS2	tsL			3		ns
Output rising delay time	tOLH	* 3 CL=20pF	16	24	43	ns
Output falling delay time	tOHL	* 5	24	32	52	ns
3-state output disable time H	tpHZ	* 4 * 6	40	100	500	ns
3-state output disable time L	tpLZ		40	100	500	ns
3-state output enable time H	tpZH		40	150	500	ns
3-state output enable time L	tpZL		40	150	500	ns
Digital output						
Digital output voltage H	VOH	IOH=-500 μA	2.7	3.4		V
Digital output voltage L	VOL	IOL=3mA			0.5	V
Leak current during output OFF	IOZ	* 6	-20		20	μA
Dynamic characteristics						
Differential gain error	DG	NTSC 40IRE mod ramp, Fc=14.3MSPS		0.5		%
Differential phase error	DP			0.3		deg
SNR	SNR	Fc=20MHz F _{IN} =1kHz		51		dB
		Fc=20MHz F _{IN} =1MHz		50		dB
		Fc=20MHz F _{IN} =5MHz		48		dB
		Fc=20MHz F _{IN} =10MHz		48		dB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply						
DVcc1 current	IDVCC1	DVcc1=5V	3	6	10	mA
		At power saving	3	5	11	mA
DVcc2 current	IDVCC2	DVcc2=5V	0	2	5	mA
		At power saving	0	2	4	mA
DGND3 current	IDGND3	DGND3=0V	2	3	5	mA
		At power saving	0	0	0.1	mA
DGND4 current	IDGND4	DGND4=0V	2	3	5	mA
		At power saving	0	0	0.1	mA
DVEE current	IDVEE	DVEE=-5V	-50	-33	-25	mA
		At power saving	-12	-3	-2	mA
AVEE current/AVF current	IAVEE IAVF	AVEE=-5V	-26	-16	-12	mA
		At power saving	-10	-5	0	mA
Power Consumption (IDVCC1+IDVCC2+ IDVEE + IAVEE)		DVcc1, DVcc2=5V DGND1, DGND2, DGND3, DGND4=0V AVF=0.7V DVEE, AVEE=-5V	40	57	80	mA
		At power saving	5	15	37	mA

*1 CLK input

*2 MINV, LINV, ENABLE, PS inputs

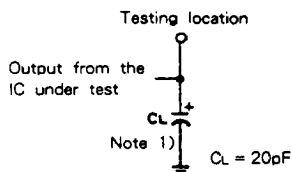
*3 See Timing Diagram (1)

*4 See Timing Diagram (2)

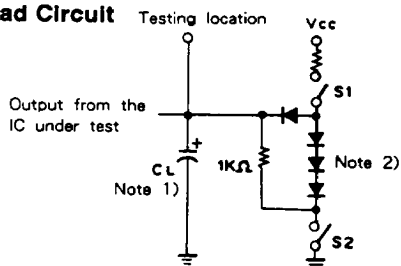
*5 Load is at the Bi-state Totem-Pole output delay time test load circuit

*6 Load is at the 3-state output test load circuit

Bi-state Totem-Pole Output Delay Time Test Load Circuit



3-state Output Test Load Circuit

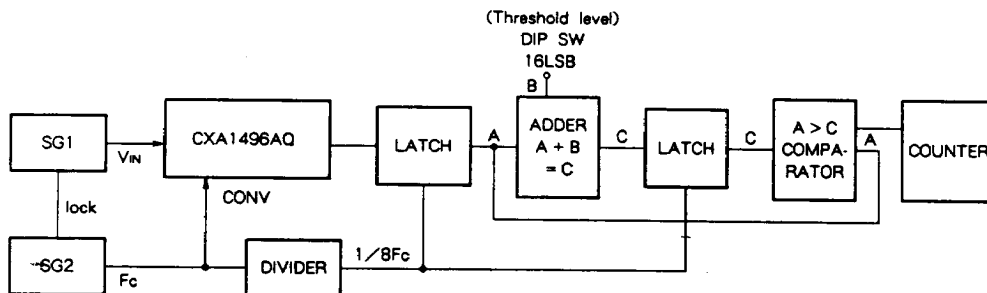


Test Conditions	S1	S2
t_{pZL}	Close	Open
t_{pZH}	Open	Close
t_{pLZ} t_{pHZ}	Close	Close

Note 1) C_L includes the probe capacitance and the floating capacitance of the test circuit.

Note 2) All diodes use 1S2076.

Error Rate Testing Circuit



Notes on Operation

1. Analog ground (Analog ground on PCB)
Keep analog ground surface on PCB as wide as possible with impedance and resistance as low as possible.
2. Digital ground (DGND1, DGND2, DGND3, DGND4)
Upon mounting to PCB keep ground surface as wide as possible with impedance and resistance as low as possible.
Moreover, a common analog and digital ground immediately near ADC will help obtain characteristics smoothly.
3. Digital positive power supply (DVcc1, DVcc2)
Connect to the digital ground with a ceramic capacitor over 0.1 μ F and as close to the pins as possible.
4. Analog positive power supply (AVF)
As the standard circuit example shown in p.16, make it about +0.7V by connecting to the analog ground with a diode and +5V with a pull-up resistor respectively.
Connect to the analog ground on PCB with a ceramic capacitor over 0.1 μ F as close to the pin as possible.
5. Analog negative power supply (AV $\bar{E}$)
Connect to the analog ground on PCB with a ceramic capacitor over 0.1 μ F as close to the pin as possible.
6. Digital negative power supply (DV $\bar{E}$)
Connect to the digital ground with a ceramic capacitor over 0.1 μ F as close to the pin as possible.
When V $\bar{E}$ is divided into digital and analog, there is continuity because of approx. 4 Ω resistance between the two inside the IC.
Accordingly, if an excessive potential difference (more than 100mV) is applied continuously, this may destroy the IC. To prevent the IC destruction, connect AV $\bar{E}$ and DV $\bar{E}$ with a inductance having good high frequency characteristics. Prevent noise mixing and the generation of potential difference between analog and digital.
7. Reference voltage (VREFTS, VREFT, VREF1, VREF2, VREF3, VREFB, VREFBS)
These pins provide reference voltage to upper and lower comparators. Voltage between Pins VREFT and VREFB corresponds to input dynamic range.
There is a 200 Ω resistance between VREFT and VREFB. By applying 2V to both pins a current of about 10mA flows. When the reference voltage is destabilized by the clock, ADC characteristics are adversely affected. Connect Pins VREFT and VREFB to the analog ground on PCB by means of a tantalum capacitor over 10 μ F and a ceramic capacitor over 0.1 μ F respectively. Also, connect each of VREF1, VREF2 and VREF3 pins to the analog ground on PCB using a ceramic capacitor over 0.1 μ F. This will provide stability to the characteristics of high frequency. Strictly speaking on reference voltage pins VREFT side and VREFB side there is a respective about 15mV offset. When there is no problem with the usage of those offset voltages, voltage is applied directly to VREFT, VREFB. In case the reference voltage is to be strictly applied, adjust to obtain an offset voltage of 0V, keeping Pins VREFTS and VREBS as sense pins and Pins VREFT and VREFB as force pins to form a feedback loop circuit.
For details, see Application Circuit.

8. Analog input (VINH, VINL)

VINH is the input pin for the upper comparator while VINL is the input pin for the lower comparator. Keep the input signal level within the level between VREFT and VREFB.

As this IC's analog input capacitance stands at about 150pF, it is necessary to drive with an buffer amplifier having sufficient driving capability. Also, when driving is done with the buffer amplifier of a low output impedance, as ADC input capacitance is large, ringing is generated and settling time grows longer. Here a small resistance of about 5 to 30Ω is connected in series between the buffer amplifier and each of ADC's VINH and VINL pins, as a dumping resistance. This eliminates ringing and shortens settling time. Also keep wiring between buffer amplifier and ADC as short as possible.

9. Clock input (CLK)

ECL LIKE input. Adds the signal of Vcc1 (5V) -0.8V at high level and Vcc1 (5V) -1.6V at low level.

Clock line wiring should be the shortest possible while distanced from other signal lines to avoid affecting them.

This IC is of the serial parallel type ADC. Accordingly an external sample and hold circuit (SH) is necessary. However the timing between this SH circuit output waveform (ADC analog input waveform) and the ADC clock timing requires attention. In the relation between ADC clock and the ADC analog input signal, with the timing T_H of the rising edge of ADC clock, the upper comparator compares the input signal and the reference voltage to latch the results. After that, with the timing T_L of the falling edge of ADC clock, the lower comparator compares the input signal and reference signal to latch the results. (Strictly speaking, the sampling delay t_{SH} is in T_H and the sampling delay t_{SL} is in T_L .)

In this ADC, the lower comparator features a length of $\pm 32mV$ ($\pm 16LSB$) redundancy in relation to the upper comparator. At the timing when the lower comparator compares input signal and reference signal to latch at the timing T_L , it is necessary to have the SH output settling performed. But at the timing when the upper comparator compares input signal and reference voltage to latch at the timing T_H , as long as the SH output is within the $\pm 32mV$ range to the final settling value, digital correction applies, A/D conversion precisely occurs. As seen from the above, ADC clock rise and fall timing versus SH output waveform should be duly considered. For the clock High level time t_{WH} and Low level time t_{WL} , set to a value in excess of the time indicated for the respective operating conditions.

Output data is output synchronously with the clock rising edge. For details on timing, refer to Timing Diagram.

10. MINV input (MINV)

Digital output polarity inversion control pin of D9 (MSB).

TTL input. At open, turns to High level input.

For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.

11. LINV input (LINV)

Digital output polarity inversion control pin of D8 to D0 (LSB).

TTL input. At open, turns to High level input.

For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.

12. 3-state (ENABLE)

3-state control pin of digital output (D0 to D9, UNDER, OVER).

TTL input. At open, turns to High level input. At that time digital output turns all to high impedance.

13. Power save input (PS)

Power save control pin of internal circuit.

TTL input. At open, turns to High level input. To set to power save mode, turn both Pins PS and ENABLE to High level input.

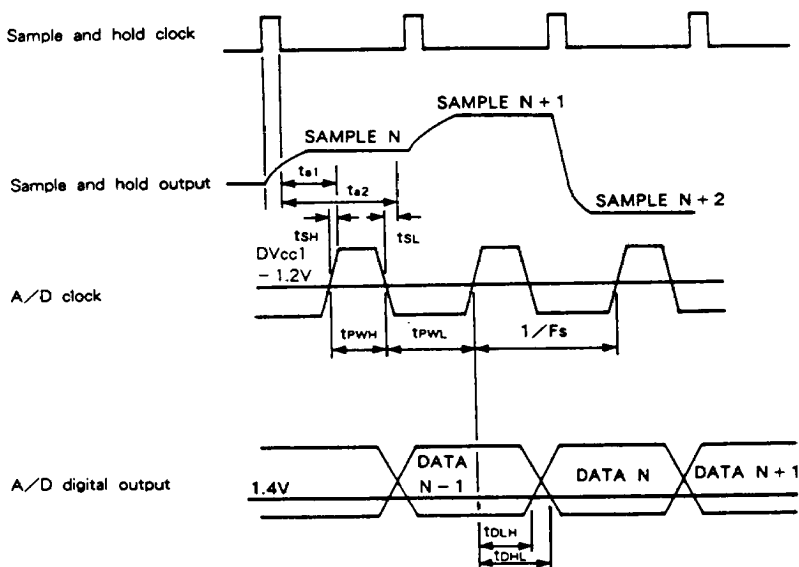
14. Digital output (D0 to D9)
Output pin of D9 (MSB) to D0 (LSB).
TTL output.
Output data polarity inversion is executed by means of MINV and LINV signals. Can output in binary, 1S complement and 2S complement.
Also, by turning ENABLE signal to High level, the output can be turned into high impedance output.
For correspondence with analog input voltage and output data code, refer to Output Formula Chart.
For the timing, refer to Timing Chart.
15. Overflow output (OVER)
When the input signal exceeds VREFT, overflow signal is output.
MINV and LINV have no effect on this pin.
Also by turning ENABLE signal to High level, the output can be turned into high impedance output.
For correspondence with analog input voltage and output data code, refer to Output Formula Chart.
For the timing, refer to Timing Chart.
16. Underflow chart (UNDER)
When the input signal turns below VREFB, underflow signal is output.
MINV and LINV have no effect on this pin.
Also by turning ENABLE signal to High level, the output can be turned into high impedance output.
For correspondence with analog input voltage and output data code, refer to Output Formula Chart.
For the timing, refer to Timing Chart.

Output Formula Chart

ENABLE		0	0	0	0	1 (OPEN)	1 (OPEN)	1 (OPEN)	1 (OPEN)	1 (OPEN)	1 (OPEN)
MINV			1 (OPEN)		1 (OPEN)		1 (OPEN)		1 (OPEN)		1 (OPEN)
LINV			1 (OPEN)		0		0		1 (OPEN)		0
OUTPUT			OF 9876543210UF (MSB)		OF 9876543210UF (LSB)		OF 9876543210UF (MSB)		OF 9876543210UF (LSB)		OF 9876543210UF (MSB)
0V		0	100000000000	101111111110	101111111110	110000000000	110000000000	111111111110	111111111110	111111111110	Z
:		1	000000000010	001111111100	001111111100	010000000010	010000000010	011111111100	011111111100	011111111100	Z
:		2	0000000000100	001111111010	001111111010	0100000000100	0100000000100	011111111010	011111111010	011111111010	Z
:		3	0000000000110	001111111000	001111111000	0100000000110	0100000000110	011111111000	011111111000	011111111000	Z
:		:	:	:	:	:	:	:	:	:	:
:		512	0100000000000	011111111110	011111111110	0000000000000	0000000000000	001111111110	001111111110	001111111110	Z
:		:	:	:	:	:	:	:	:	:	:
:		1019	011111110110	010000001000	010000001000	001111110110	001111110110	000000001000	000000001000	000000001000	Z
:		1020	011111111000	010000000110	010000000110	001111111000	001111111000	000000000110	000000000110	000000000110	Z
:		1021	011111111010	010000000100	010000000100	001111111010	001111111010	000000000100	000000000100	000000000100	Z
:		1022	011111111100	010000000010	010000000010	001111111100	001111111100	000000000010	000000000010	000000000010	Z
-2V		1023	011111111111	010000000001	010000000001	001111111111	001111111111	000000000001	000000000001	000000000001	Z

0: VOLTAGE LEVEL-LOW OF: OVER FLOW
 1: VOLTAGE LEVEL-HIGH UF: UNDER FLOW
 Z: HIGH IMPEDANCE

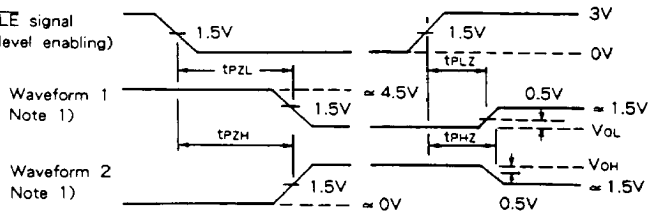
Timing Diagram (1)



T_H is the timing of latching result for the comparison of V_{IN} and V_{REF} the upper comparators.

T_L is the timing of latching result for the comparison of V_{IN} and V_{REF} in the lower comparators.

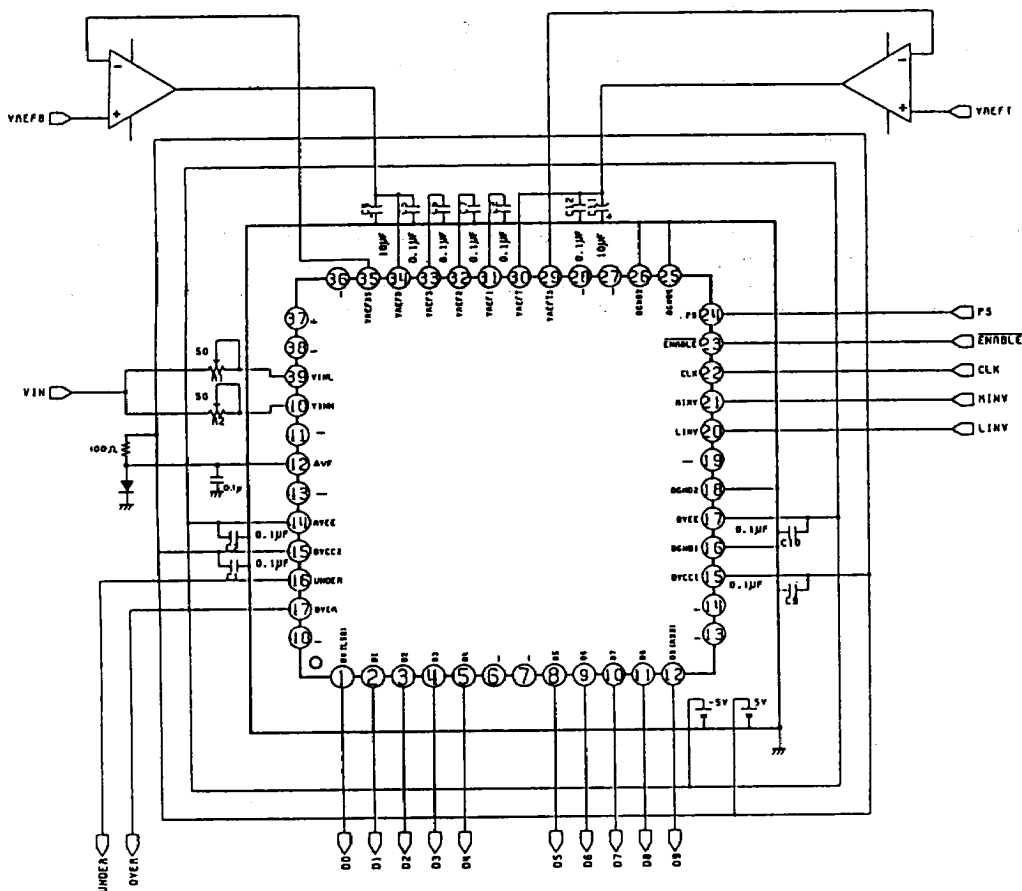
ENABLE signal
(Low-level enabling)



Voltage waveform of 3-state enable and disable *
 (* Enable time= t_{PZL}/t_{PZH}
 Disable time= t_{PLZ}/t_{PHZ})

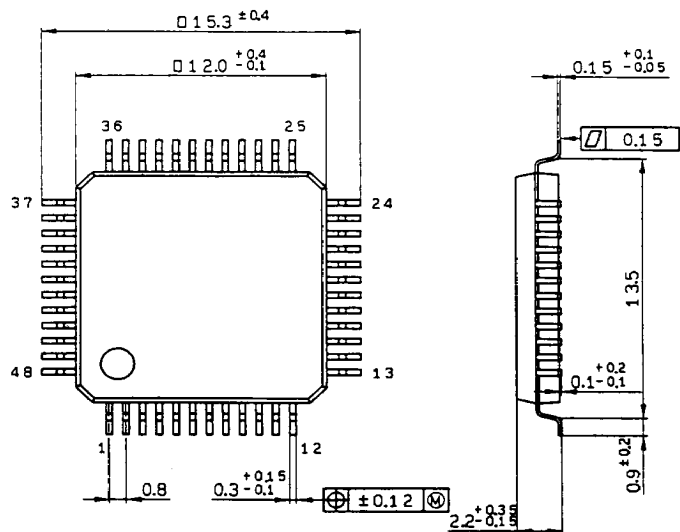
Note) Waveform 1 indicates the output waveform when internal conditions are set to obtain a low level output, with the exception of when output is disabled by means of the ENABLE signal.
Waveform 2 indicates the output waveform when internal conditions are set to obtain a high level output, with the exception of when output is disabled by means of the ENABLE signal.

Standard Circuit



Package Outline Unit : mm

48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	