SONY

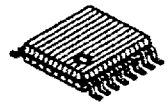
CXA1850N

Low Current Consumption FM IF Amplifier for Pagers

Description

The CXA1850N is a low current consumption FM IF amplifier which employs the newest bipolar process. It is suitable for such sets as Japan single conversion pagers which require low current consumption.

16 pin VSOP (Plastic)



Features

- Low current consumption 720 μA (typ. at Vcc=1.5V)
- Low voltage operation Vcc=1.0 to 4.0V
- Few external parts for needless of IF decoupling capacitor
- Built-in reference power supply for operational amplifier and comparator
- Small package 16-pin VSOP
- IF input GND standard

Functions

- Second IF and limiter amplifiers
- FM detector
- Quaternary LPF operational amplifier
- FSK comparator
- Regulator output for RF amplifier and first mixer
- Power-save function
- Reduced voltage detection circuit

Applications

Single super pagers for Japan and overseas

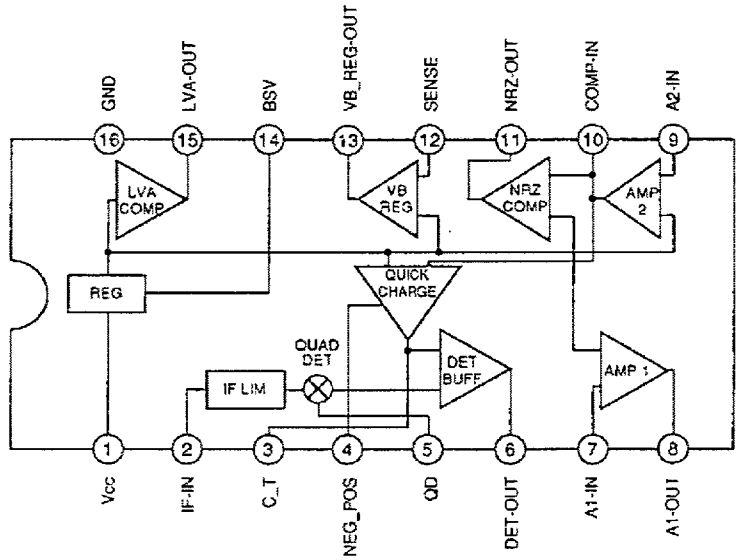
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	7.0	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C

Operating Condition

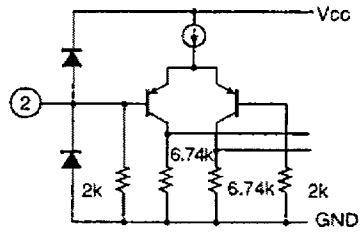
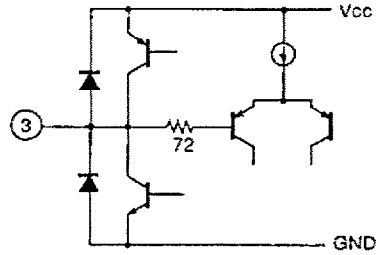
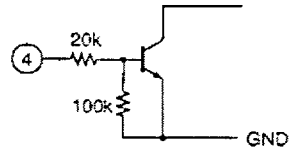
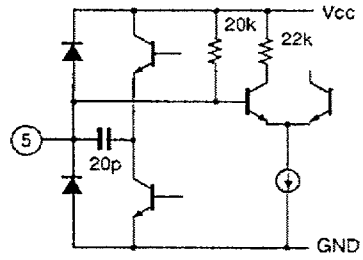
Supply voltage	Vcc	1.0 to 4.0	V

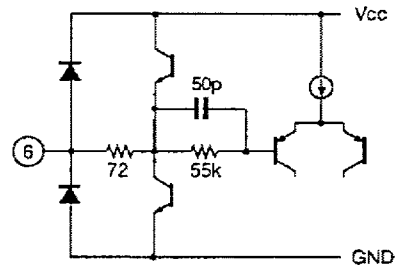
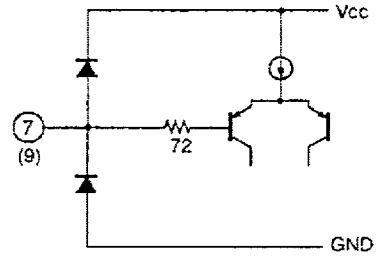
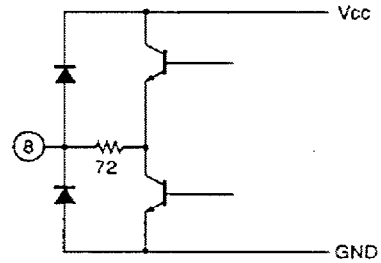
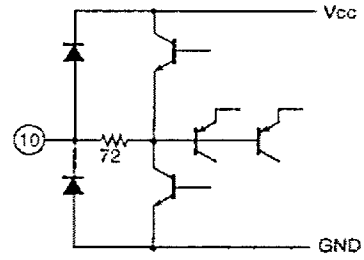
Block Diagram

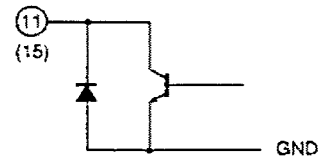
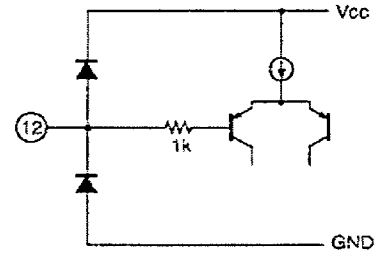
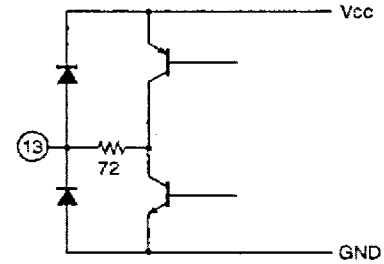
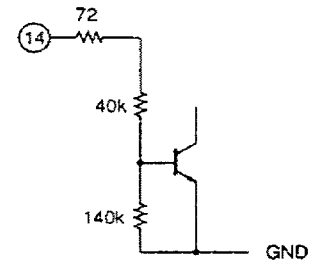


E93510—ST

Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	Vcc			Power supply.
2	IF-IN	0V		IF limiter amplifier input.
3	C_T	0.2V		Connects a capacitor that determines the low cut-off frequency for the entire system.
4	NEG_POS	0V		Controls the ON/OFF operation of the quick-charge circuit. (Applied voltage range: –0.5 to +7.0V)
5	QD	1.5V		Connects the phase shifter of FM detector circuit.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	DET-OUT	0.2V		FM detector output.
7 9	A1-IN A2-IN	0.2V 0.2V		Input for operational amplifiers 1 and 2 (AMP1, AMP2).
8	A1-OUT	0.2V		Output for operational amplifier 1 (AMP1).
10	COMP-IN	0.2V		NRZ comparator input. Output for operational amplifier 2 (AMP2) is connected.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11 15	NRZ-OUT LVA-OUT	— —		NRZ and LVA comparator outputs and they are open collectors. (Applied voltage range −0.5 to +7.0V)
12	SENSE	0.2V		Input pin for internal constant-voltage source amplifier. This pin is controlled to maintain 200mV.
13	VB_REG-OUT	—		Output pin for internal constant-voltage source amplifier. Connect the base of PNP transistor. (Current capacity: 100μA)
14	BSV	—		Controls the battery saving. Setting this pin low suspends the operation of IC. (Applied voltage range: −0.5 to +7.0V)
16	GND	—		Ground

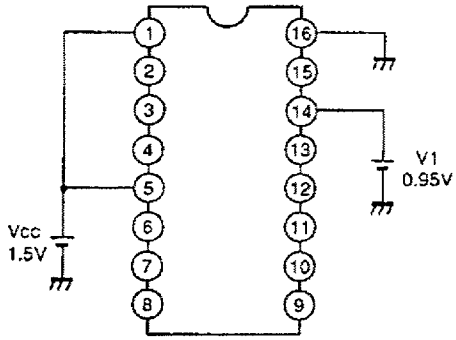
Electrical Characteristics (VCC=1.5V, Ta=25°C, Fs=455kHz, FMOD=256Hz, FDEV=2.3kHz, AMMOD=30%)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	ICC	Measurement circuit 1	500	720	930	µA
Current consumption	ICCS	Measurement circuit 1, V1=0.3V			20	µA
AM rejection ratio	AMRR	Measurement circuit 3, VIN=60dBµ	25			dB
Op amp. input bias current	IBIAS	Measurement circuit 2		40	100	nA
Op amp. open loop gain	AV	Measurement circuit 4	45			dB
Op amp. output voltage amplitude	VO	Measurement circuit 5	0.65			Vp-p
NRZ output saturation voltage	VSATNRZ	Measurement circuit 8			0.4	V
NRZ output leak current	ILNRZ	Measurement circuit 7			5.0	µA
NRZ hysteresis width	VTWNRZ	Measurement circuit 6	5	10	15	mV
VB output current	IOUT	—	100			µA
VB output saturation voltage	VSATVB	Measurement circuit 9			0.4	V
VB SENSE voltage	VSENVB	—	205	215	225	mV
LVA operating voltage	VLVA	Measurement circuit 10, NRZ_COMP operation	1.05	1.10	1.15	V
LVA output leak current	ILLVA	Measurement circuit 10			5.0	µA
LVA output saturation voltage	VSATLVA	Measurement circuit 8			0.4	V
Detector output voltage	VODET	Measurement circuit 3	21	28	38	mV
Logic input voltage high level	VTHBSV		0.9			V
Logic input voltage low level	VTLBSV				0.35	V
Limiting sensitivity	VIN (LIM)	Measurement circuit 3		17	24	dBµ

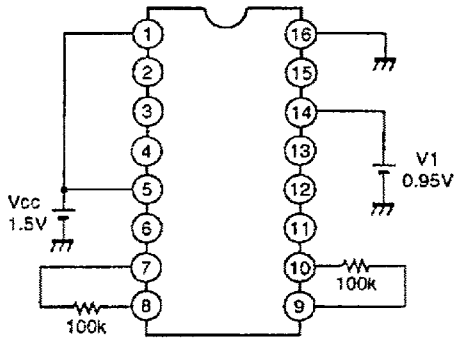
Design Data

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
IF limiter input resistance	RINLIM		1.6	2.0	2.4	kΩ
Op amp. minimum input voltage					0.05	V
Comparator minimum input voltage					0.05	V
LVA hysteresis	VTHLVA	Measurement circuit 10, NRZ_COMP operation		10		mV

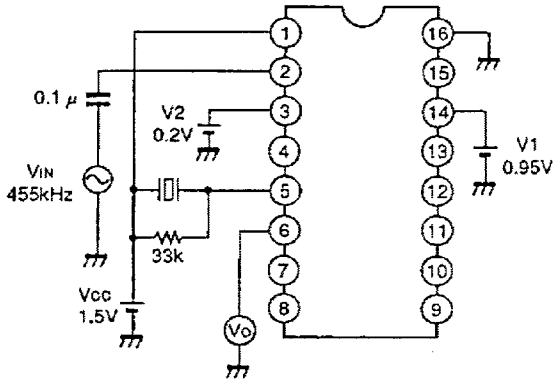
Measurement Circuit



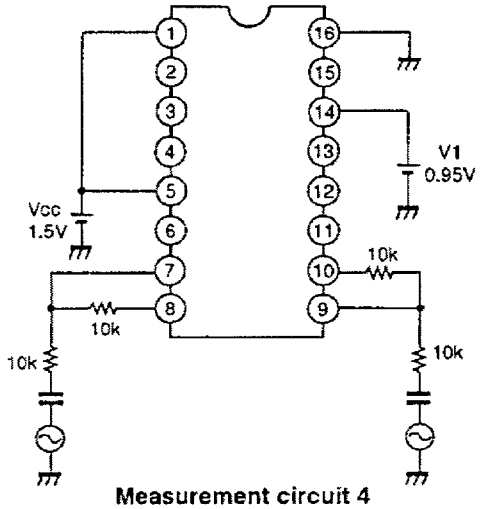
Measurement circuit 1



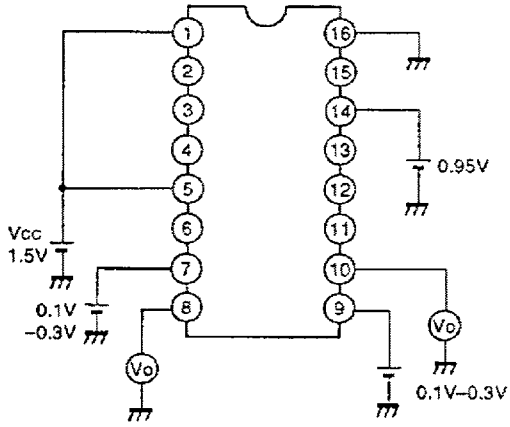
Measurement circuit 2



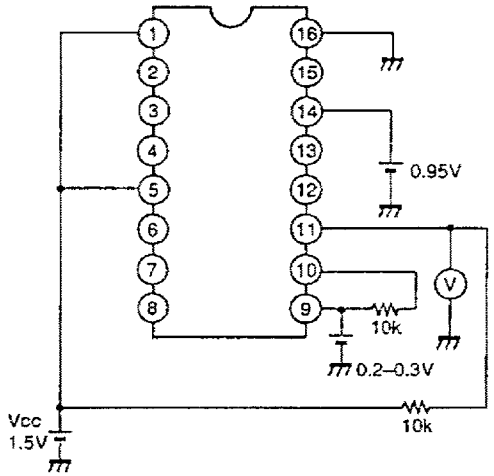
Measurement circuit 3



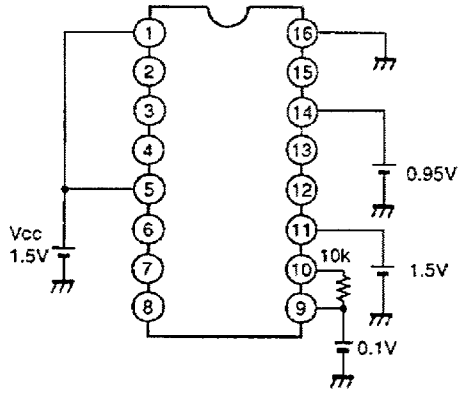
Measurement circuit 4



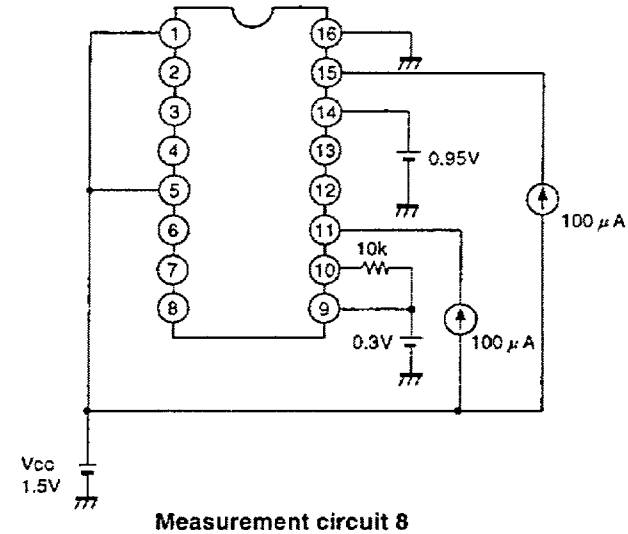
Measurement circuit 5



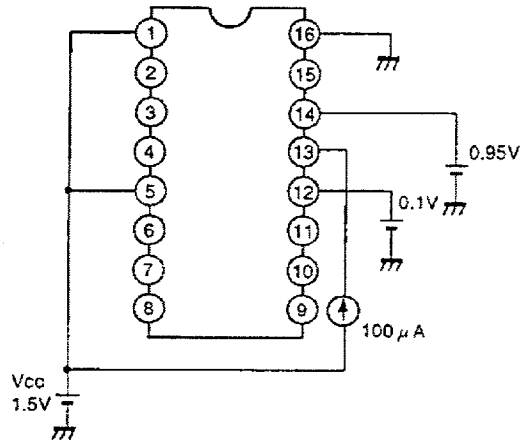
Measurement circuit 6



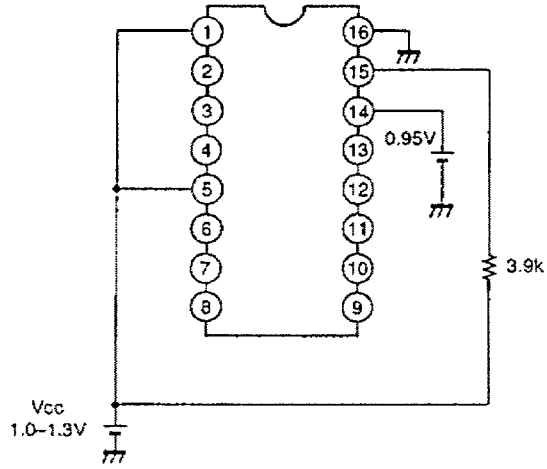
Measurement circuit 7



Measurement circuit 8



Measurement circuit 9



Measurement circuit 10

1) Power Supply

The CXA1850N, with built-in regulator, is designed to permit stable operation at wide range of supply voltage from 1.0 to 4.0V. Decouple the wiring to Vcc (Pin 1) as close to the pin as possible.

2) IF Filter

The filter to be connected between IF limiters should have the following specifications.
Output impedance : 2.0kΩ±10%
Band width : Changes according to applications

3) IF Limiter Amplifier

The gain of this IF limiter amplifier is approximately 100dB. Take notice of the following points in making connection to the IF limiter amplifier input pin (Pin 2).

a) Be sure the wire to the IF limiter amplifier input (Pin 2) is as short as possible.

b) As the IF limiter amplifier output appears at QD (Pin 5), be sure the wire to the RLC and ceramic discriminator connected to QD is as short as possible and reduce the interference with the IF limiter amplifier input.

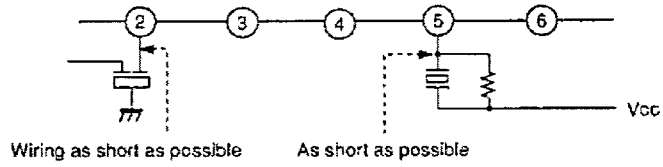
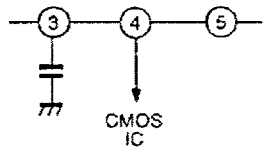


Fig. 1

4) Quick Charge

In order to hasten the rising time from when power is turned on or when reception standby, the CXA1850N features a quick charge circuit.
Therefore, the quick charge circuit eliminates the need to insert a capacitor between the detector output and the LPF as is the case with conventional ICs, but connects a capacitor to Pin 3 to determine the average signal level during steady-state reception. The capacitance of the capacitor connected to Pin 3 should be chosen such that the voltage does not vary much due to discharge during battery saving.
Connect a signal for controlling the quick charge circuit to Pin 4. Setting this pin high enables the quick charge mode, setting this pin low enables the steady-state reception mode. Quick charge is used when the power supply is turned on. The battery saving must be set high at the time. Quick charge is also used according to need during battery saving.
Connect Pin 4 to GND when quick charge is not being used.



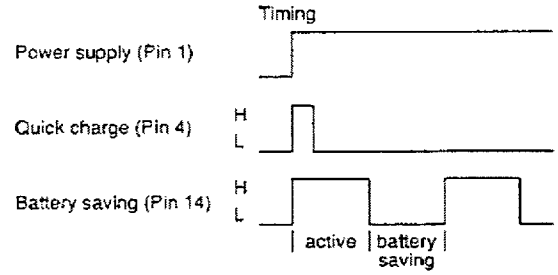
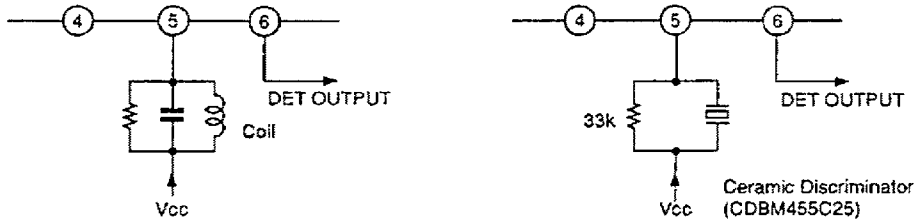


Fig. 2

5) Detector

The detector is of quadrature type. To perform phase shift, connect RLC resonator circuit or ceramic discriminator to Pin 5.
The phase shifting capacitor for the quadrature detector is built in.
The demodulated FM (FSK) signal from the detector will have its high-frequency component eliminated through the LPF of the DET-BUFF and then fed to DET-OUT (Pin 6).
DET-OUT output impedance is 200 Ω or less.

The CDBM455C25 (MURATA MFG. CO., LTD.) ceramic discriminator for the CXA1850N is recommended.



a) Coil b) Ceramic Discriminator

Fig. 3

6) AMP, NRZ-OUT

Two operational amplifiers are built in this IC.
One of them is connected internally to an NRZ comparator.

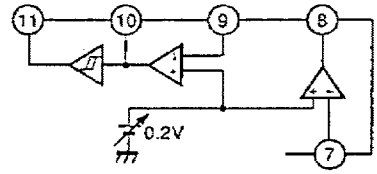


Fig. 4

Using these two operational amplifiers to construct an LPF, remove noise from the demodulated signal and input to the NRZ comparator, which is the next stage.
The NRZ comparator molds waveform of this input signal and outputs it as a square wave. The NRZ comparator output stage is for open collector.
Thus, if the CPU is of CMOS-type and the supply voltage is different, a direct interface as illustrated in the figure below can be implemented.

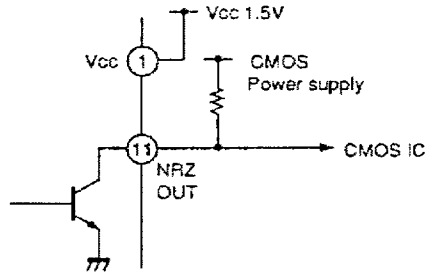


Fig. 5

7) SENSE, VB_REG-OUT

Controls the base bias of the external transistors.

8) LVA-OUT

This pin goes high (open) when the supply voltage becomes low. Since the output is an open collector, it can be used to directly drive CMOS device as can NRZ-OUT. The setting voltage of the LVA is 1.10V (typ.), and it possesses a hysteresis with respect to the supply voltage. The hysteresis width is 10mV (typ.).

9) BSV

Operation of the CXA1850N can be halted by setting this pin low. This pin can be connected directly to CMOS device. The current consumption for BSV is 20 μA or less (at 1.5V).

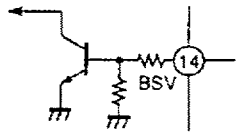


Fig. 6

Principle of Quick Charge Operation

BUF in Fig. 7 is the detector buffer amplifier, and AMP1 and AMP2 are operational amplifiers to construct an LPF. COMP is the NRZ comparator. Coupling on conventional system is performed by placing a capacitor between the detector buffer and the LPF operational amplifier, matching of DC is not performed . Thus, this matching capacitor must be charged when restoring the system from reception standby mode to reception mode, within which time signals from the comparator appear at the NRZ output.
To shorten this rise time, as shown in Fig. 7 the CXA1850N adds feedback loop from the comparator input to the input circuit of output. This equalizes the average value of the comparator input voltage to the reference voltage, with the quick charge circuit of CHG being set inside the feedback loop. Switching the current of quick change circuit enables reduction of the rise time.
In this block, CHG is a comparator which compares the input voltage and outputs the current based on this comparison. The current on CHG is switched between high and low at Pin 4. To shorten the time constant when switching from reception standby mode to reception mode, switch the current to high and increase the charge current at C in Fig. 7. During steady-state reception mode, switch the current to low, lengthening the charge time constant, and allowing for stable data retrieval.

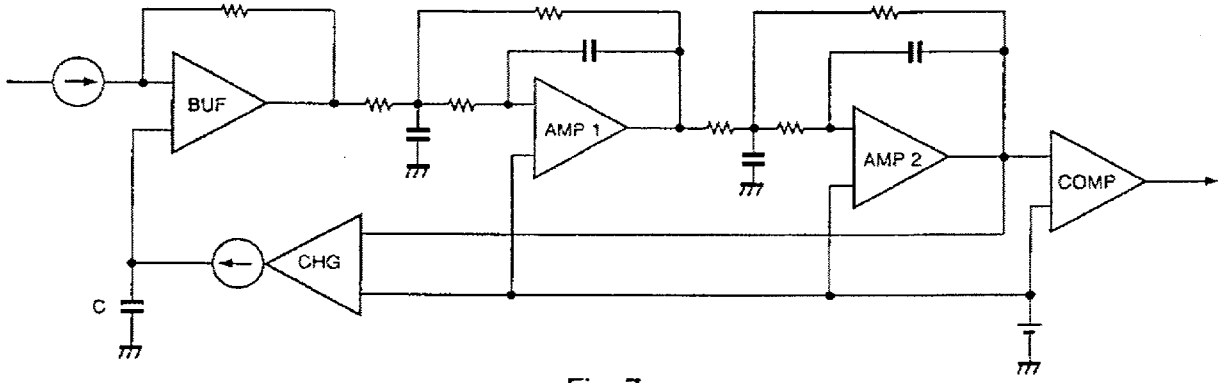


Fig. 7

[CXA1850N data filter constant settings]

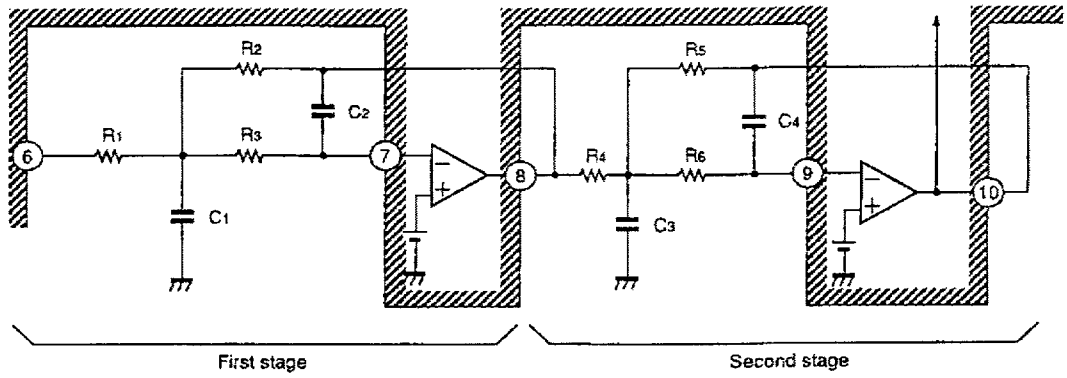


Fig. 8

<Method for determining the circuit constants>

The data filter cut-off frequency fc (Hz) is determined according to the data speed. By first determining the value of the capacitor C_1 (=C_3), the parameter K is determined.

$$K = \frac{100}{fcC'}$$ where C' is the value of C_1 expressed in μF.

If the value of K calculated in this way is multiplied by the appropriate value from the following table, the required characteristics are obtained.

Circuit Constant Values

Part symbol \ Gain of each stage (dB)	0	6
R_1, R_4	3.374	2.530
R_2, R_5	3.374	5.060
R_3, R_6	3.301	3.301
C_2, C_4	0.15C_1	0.1C_1

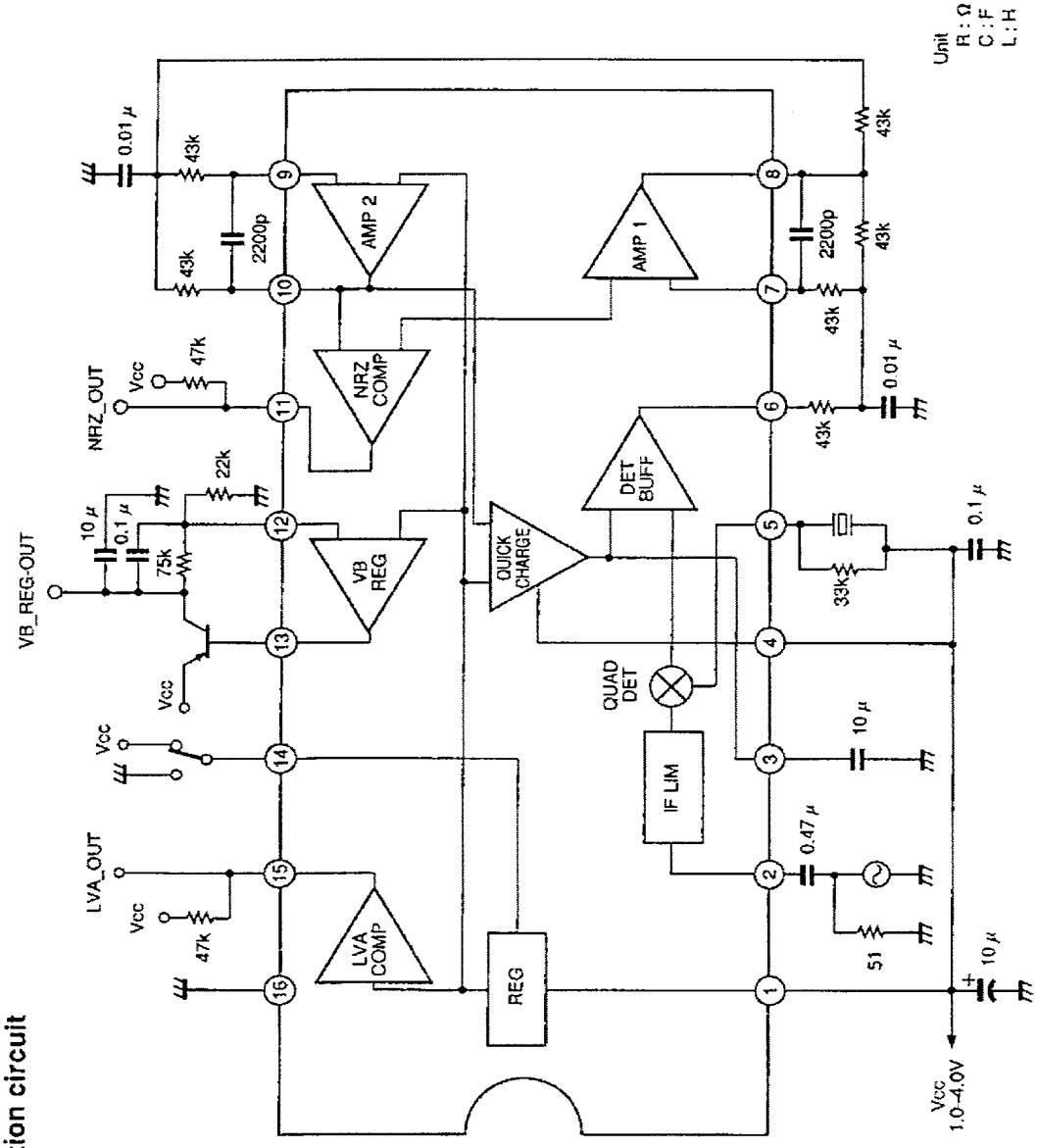
Resistance when parameter K=1 (Unit : kΩ)

Ex.) Assuming fc=768Hz (256Hz x 3) and C_1 (=C_3) =0.01μF.

$$K = \frac{100}{768 \times 0.01} \fallingdotseq 13.0$$

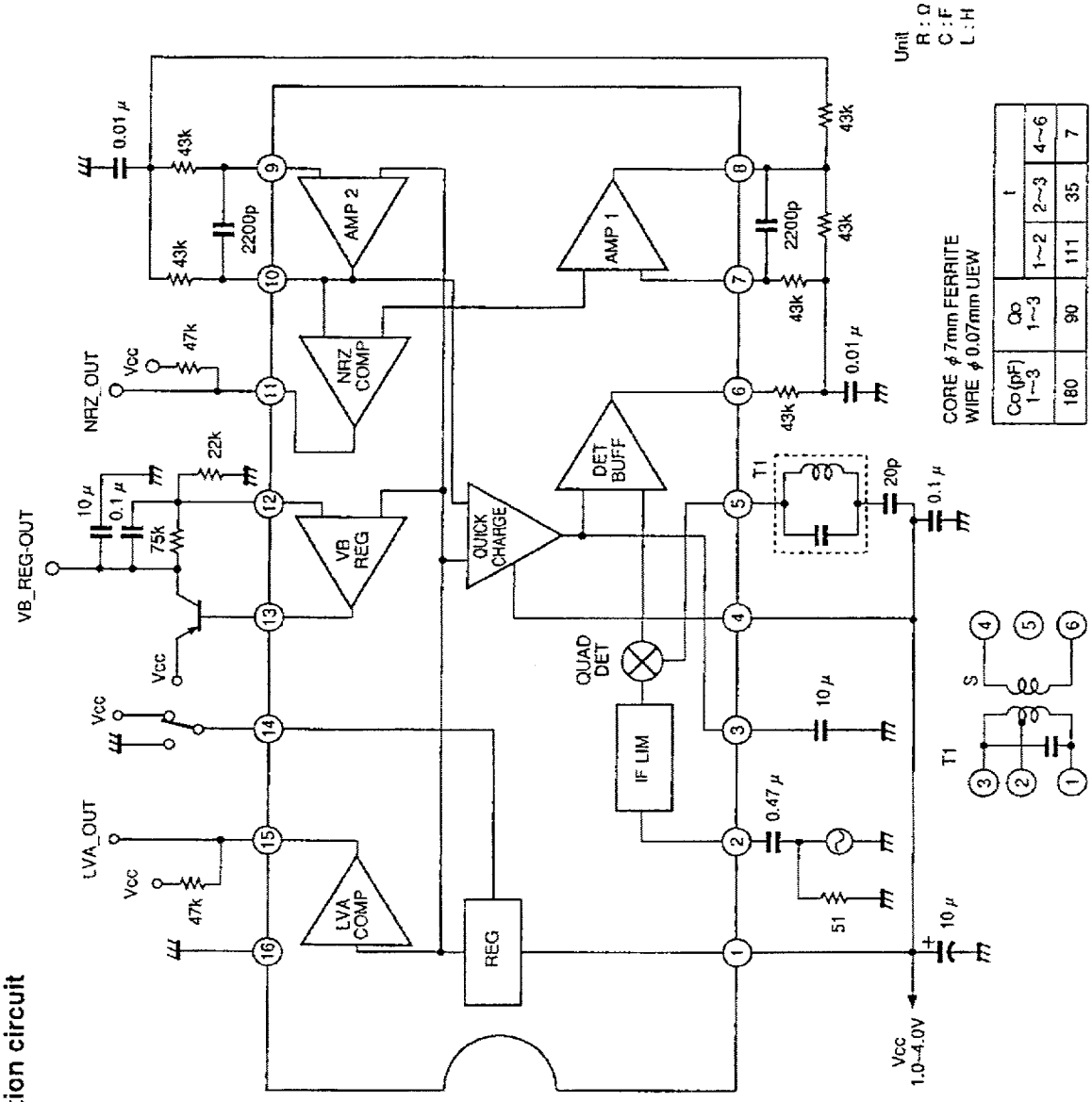
The usable resistances and capacitances derived from this K value and above table are indicated in the following Application Circuit.

Application circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application circuit



Co (pF) 1~3	Qo 1~3	t 1~2	t 2~3	t 4~6
180	90	111	35	7

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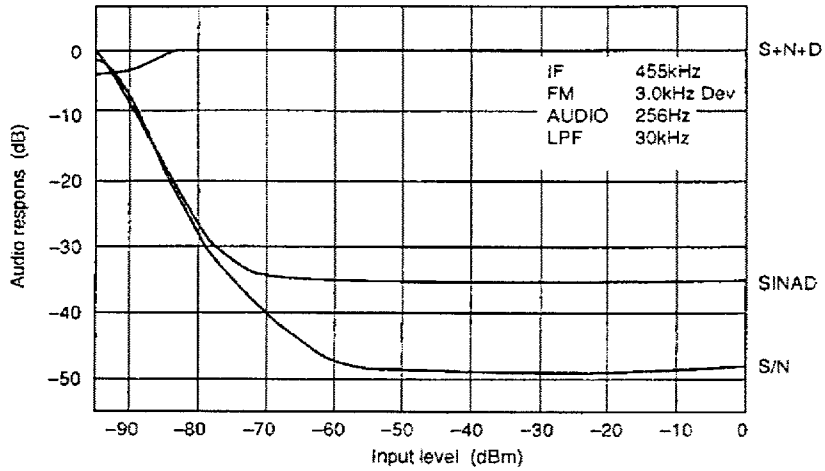
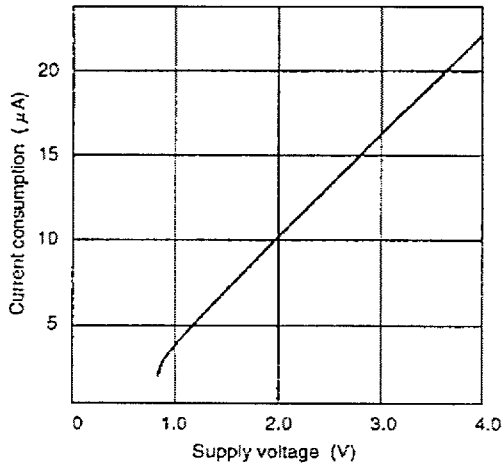
Example of Representative Characteristics

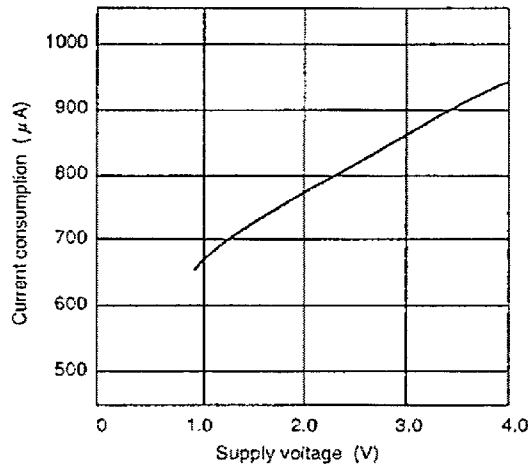
Input/output characteristics (at Pin 10)



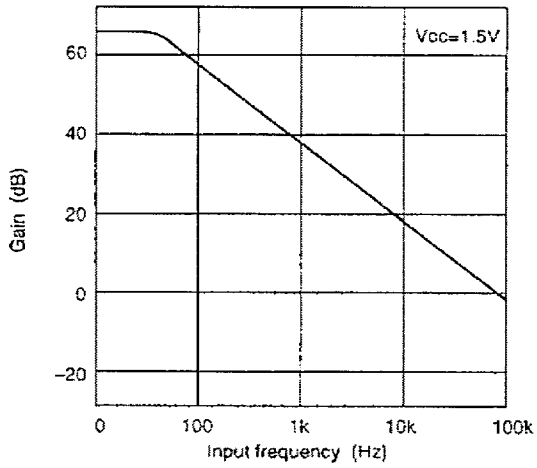
Supply voltage vs. Current consumption (battery saving mode)



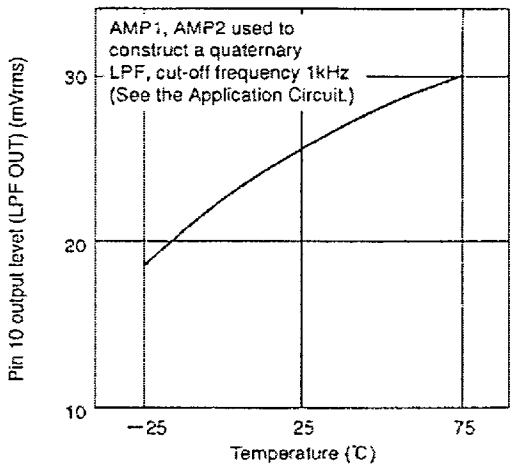
Supply voltage vs. Current consumption



Operational amplifier input frequency vs. Gain



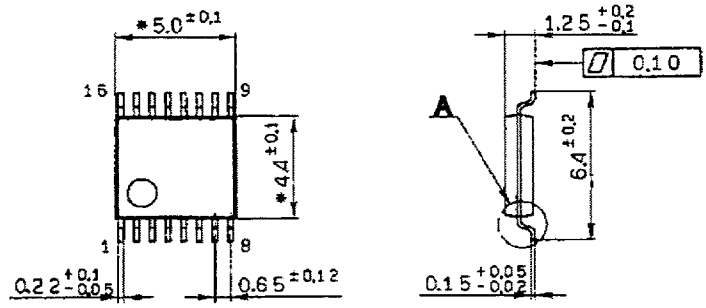
Pin 10 output level vs. Temperature

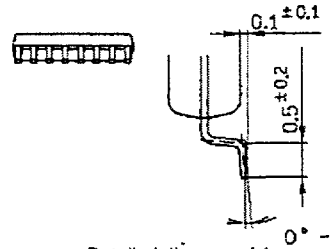


Package Outline

Unit : mm

16pin VSOP (Plastic) 225mil





Detailed diagram of A

SONY NAME	VSOP-16P-L01
EIAJ NAME	SSOP016-P-0225-Similar A
JEDEC CODE	———

Note) Dimensions marked with * do not include resin residue.