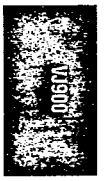
3 VJ900
ANALOG MASTER CHIP FAMILY

T-42-21

USER'S GUIDE

Release 2.0

CONTENTS



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I. INTRODUCTION

1.1 Preface

The VJ900 User's Guide gives a design engineer the information and data needed to begin designing integrated circuitry. The engineer who has done successful designs with discrete components can do equally well with IC design because the basic elements are the same, but are used under somewhat different constraints. The purpose of this user's guide is to set forth some of those constraints and explain how they arise.

A careful reading of the VJ900 User's Guide will help the beginning IC designer avoid elementary mistakes. The text contains several explicit Do's and Don't's along with discussions of the physical reasons for each rule. It covers basic integrated circuit design concepts, and methods and data for circuit simulation. However, because the user's guide does not cover all the detailed aspects of IC design, it is recommended that the designer use the book *Analysis and Design of Analog Integrated Circuits* (2nd Ed.) by P.R. Gray and R.G. Meyer, J. Wiley (1984). This is an excellent book on basic linear IC design techniques.

The VJ900 User's Guide is organized on a component basis, with separate chapters describing each type of component used in the VJ900 series master chips.

1.2 Bipolar-CMOS Comparison

Today, CMOS is the dominant technology for logic ICs, and is being used increasingly for analog ICs as well. This section summarizes some of the differences between bipolar and CMOS devices, so an informed decision can be made for a particular design.

Power

CMOS offers great advantages in power dissipation for logic circuitry. The same considerations do not apply to analog circuits, however, because in both CMOS and bipolar ICs such circuits usually must draw current at all times.

Transconductance

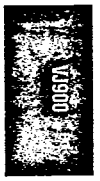
The bipolar device has a fundamental advantage arising from basic device physics. The bipolar transistor can be turned ON with only about 150 mV change in V_{be}, while to turn a MOSFET fully ON requires several V change in the gate voltage. The transconductance is 10 to 50 times higher for the bipolar transistor in typical circuit applications.

Gain-bandwidth product

One consequence of the higher transconductance of the bipolar device is a generally higher gain-bandwidth product. Voltage gains of 500 to 1000 are readily achievable in a single actively-loaded stage. A higher gain also translates to superior performance in feedback loops, easier frequency compensation, etc.

Transistor matching and input offsets

The bipolar device gives offsets around 1 mV, while the MOSFET is reported to have offsets of typically 5 to 15 mV. The higher bipolar transconductance also means that offsets due to mismatch in the load elements have less influence on input offset.



Repeatability

An interesting question is how well the parameters of a process repeat from run-to-run and wafer-to-wafer. The turn-on voltage of a bipolar transistor is only logarithmically dependent on the doping levels and device dimensions, while that for a MOSFET has a much stronger dependence. The better inherent repeatability of bipolar processes is perhaps best seen in memory circuits, where FET chips will have a 3:1 ratio between the fastest and slowest product from a given chip design (the so-called "dash numbers" in a product catalog). For bipolar, the speed distribution is more typically ±15%.

Modeling accuracy

The MOSFET has a number of effects—the body effect, the short-channel effect and the second gate effect—which are hard to model and have no analogy in a bipolar transistor. The model parameters for the FET are also much more dependent on the device dimensions. Consequently, SPICE modeling accuracy is substantially worse for FETs.

Noise

The bipolar device is less resistive than the MOSFET, resulting in low Johnson/Nyquist noise. MOSFETs have been observed to have large amounts of 1/f noise at low frequency (up to 10 kHz), while bipolar transistors have very little 1/f noise (typical noise corners 10 to 50 Hz). The pickup of electrical noise from neighboring circuitry due to the current spikes which occur during switching of typical logic structures is often troublesome for CMOS. Bipolar offers very quiet logic switching (with CML and ECL logic forms) at the expense of higher power and a lower packing density.

Linearity

The MOSFET is a more nonlinear device than the bipolar transistor (especially short-channel types). This means that CMOS amplifiers must almost always use negative feedback to stabilize the gain and reduce distortion. In many cases this is unnecessary for bipolar. Bipolar has a linearity advantage in the use of linear resistors as loads, as compared to the nonlinear FET loads used with CMOS.

Logic-with-analog capability

This is generally superior with CMOS if large amounts of logic are desired. The amount of logic which can be placed on a bipolar chip is less due to the lower packing density.

Temperature compensation

It is often necessary to keep some properties (i.e., gain, DC voltage) stabilized with respect to temperature. Bipolar has a large body of techniques (bandgap references) for achieving this which are largely absent from CMOS.

Dynamic techniques

There are situations where it is desirable to use charge stored on a node as an analog variable. This is difficult with bipolar circuits because the device draws a DC base current.

Analog gating

CMOS provides a transmission gate which can be used as an analog switch. This feature is usually lacking in bipolar.

Complementary design methods

The use of complementary-symmetry design is desirable for many kinds of circuitry. CMOS provides high performance in both the PMOS and NMOS FETs, while most bipolar processes team a fast NPN with a slow lateral PNP in such circuits. The CBP process used in the VJ900 overcomes this limitation by offering high-performance NPN and PNP transistors. Bipolar generally offers higher precision than CMOS, at the expense of lower packing density.

1.3 The CBP Process

The VJ900 series master chips are all fabricated with VTC's complementary bipolar process (CBP). This process is a unique oxide-isolated bipolar/linear process intended for making high-performance linear integrated circuits. A high packing density is achieved by the use of shallow structures, which also provide good frequency response in the NPN transistors but have limited breakdown voltages. The NPN transistors have unity-gain bandwidths of about 6 GHz. Additional process steps allow the fabrication of high-speed (about 1 GHz F_T) high-current true vertical PNP transistors. The process is intended to operate with no more than 12 V between the most positive and most negative DC supply voltages. Designs with more than 5 V supplies require careful design in some types of circuitry to avoid breakdown problems. The nominal supply schemes shown in Table 1 are acceptable with reasonable voltage tolerances.

Table 1: Typical Power Supply Schemes

+5, 0, -5 V	Linear
0, +5 V	TTL
0, -5.2 V	ECL
0, +5, +12 V	Disk Drive Standard

Because of the relatively high packing densities achieved, this process also allows the designer to include substantial amounts of logic circuitry (up to a few hundred gates) along with linear circuits. The most favorable logic forms for logic/linear combinations are CML and ECL (see VTC's *Design Note DN-4*).

It is possible to buffer these to TTL levels at inputs and outputs. The CBP process provides two layers of metal interconnections. This is desirable for large, complex chips.

VJ900 series master chips support the following components:

- Vertical NPN transistors
- Vertical PNP transistors
- Schottky diodes
- Base (P–) resistors (nominal 900Ω / square)
- Enhancement resistors (nominal 150Ω / square)
- Zener diodes (nominal Zener voltage about 5 V)
- Oxide (linear) capacitors.

The data sheet for each master chip must be consulted to determine how many of each component are provided.

The CBP process comes closer than other linear processes toward making the PNP an equal partner in the circuit. The vertical PNPs do not have the same speed as the NPNs, but their performance relative to the NPNs is much better than in other bipolar/linear processes. This makes all kinds of complementary circuits feasible with CBP, and allows the use of PNPs in fast signal paths.

There are certain forbidden design practices which must be pointed out:

- NPN and PNP transistors may not be operated in the inverted mode, and
- Operation of transistors in saturation is not allowed unless they are Schottky-clamped.

1.4 Constraints of IC Design

Integrated components differ substantially from discretes. Some of the larger differences are:

- Integrated components are diode-isolated in these processes, while discretes are isolated by air or solid insulators. A suitable DC reverse-bias must be maintained across the isolation junctions at all times if they are to be insulators (i.e., pass negligible current).
- The general power and current levels used inside an IC are much lower than those typical of discrete designs. This can be done because of the very low parasitic capacitances of on-chip elements. A typical node capacitance on-chip is .05 to .1 pF.
- DC coupling is generally used. Large bypass and coupling capacitors take up a prohibitive amount of area (or else take up expensive pins if they are off-chip). In general, capacitances of a few pF are the largest used on-chip. This amount of capacitance often dominates other on-chip stray capacitances.
- The total transistor and resistor count is less important than with discretes. The incremental cost of another transistor is quite low. Transistors are often used in great profusion as loads, etc., where passive elements would be used in a discrete design.
- On a single chip the matching and tracking of elements is much better than matching of discrete components. Two identical resistors, for example, will match within a few tenths of a percent over all temperature and processing variations. However, their absolute values are much less well-controlled than their matching.
- Silicon is a very good thermal conductor—better than some metals. Thus, temperature variations across a single chip are usually small and the effect of temperature can be assumed to be identical for all components on a chip. An exception can be found in certain kinds of analog circuits (e.g., high-gain amplifiers) where the temperature gradients on the chip can affect matching of the resistors and transistors.
- The packaging of IC chips imposes sharp constraints on the allowable power dissipation. In general, most common packages (such as DIPs) will not safely dissipate more than .5 to 1 W. Thus, the use of low operating currents inside the chip is not only an opportunity of IC design, but often a necessity as well.

1.5 Modeling and Breadboards

Many discrete-component designers are accustomed to building breadboards of their circuit and testing them out before committing them to production. The designer could consider doing this for integrated designs by building up the circuit either with commercial metal can transistors or with the actual integrated transistors bonded out in a suitable package. Unfortunately, this does not work very well, since the typical on-chip parasitic capacitances are more than an order of magnitude smaller than the "stray C" introduced by scope probes, package capacitance, wires, etc. This will cause gross errors in measurements of time delay and frequency response, although DC level measurements can sometimes be usefully done with breadboards. For some high-performance ICs the package parasitics have a dominant influence on performance. In such cases, the package properties must also be modeled as part of the design effort (see Section 6.6). The near-universal practice in IC design is to use simulation programs—electronic breadboards. These programs actually solve the full nonlinear differential equations for the circuit exactly. Familiarity with these programs is the one inescapable new discipline which the IC design engineer must acquire.

Simulation programs, of which SPICE and ASPEC are the best-known examples, are only as good as the data put into them. In particular, stray capacitance occurs everywhere in a chip, and it must be modeled accurately if good results are to be obtained (i.e., if the electronic breadboard is to agree with reality). This often requires that extra parasitic components (usually reverse-biased diodes) be inserted into the schematic. This may seem like extra effort, but if accurate results are to be obtained the designer should adhere to this discipline. The parasitic capacitance of a resistor to its surrounding body region is a particular case of great importance. Another common source of stray C is the metal interconnection lines on a chip, especially the longer ones. The importance of accurate simulation cannot be overly stressed, since a new iteration of the design can take months and cost thousands of dollars. A quick resort to the soldering iron is no longer possible in the IC age, and the "cut and try" should be done at

the simulation stage. It is often found that when parasitic Cs of resistors, metal, etc. are completely ignored, the simulation will indicate delays and frequencies up to twofold better than reality. This can cause great dissatisfaction when the simulation results are compared to measurements on the finished chip. Such disasters are only a further example of the "garbage in, garbage out" principle in computer work—the output is no better than the initial data.

VTC takes no responsibility for the observed time-domain or frequency-domain behavior versus simulation unless *all* of the parasitic capacitances described here are included in the simulation.

1.6 Design Tolerances

One of the tasks of the circuit designer is to make sure the circuit has adequate tolerances—that it will operate satisfactorily under any required conditions of temperature and supply voltage, and that the manufacturing yield will not be low due to the normal statistical variations in the fabrication process. The circumstances for an integrated design are different than those for a discrete design, and the designer should be familiar with the differences in order to make best use of the IC process. Integrated circuit technology deals with very large numbers of elements. A typical IC today will have several thousand resistors, transistors, etc. Moreover, in most ICs it is not possible to measure the properties of these components individually since they are buried in the internal circuitry of the die and have no terminals where measuring equipment can be attached. Consequently, it is impossible to deal with them all as elements whose properties are exactly known. Instead, the designer must make careful measurements of the properties of individual sample components and finding the statistical distributions of the parameters of interest. The designer must then carry through the design using these statistical numbers as a guide for the expected circuit behavior. The parameters of IC elements are affected by many influences. Consider, for example, the things that can affect a resistor value (or ratio):

- The resistor effective size varies due to: a) variations in the mask feature size, b) variations in the photoresist expose and develop operations, and c) variations in the etching process.
- The sheet resistance of the resistor will vary due to fluctuations in gas flow rates, temperatures, etc., in the diffusion furnace.
- The resistor value can be moderately influenced by the dopant concentration in adjacent regions, and by the voltage across its isolating junction.
- Resistor ratios can be influenced by temperature gradients across the chip, since the resistors have a finite temperature coefficient.

The point is that resistor value is affected by many independent influences. This is relevant to whether one should do worst-case or statistical design. In a worst-case design one would add up the percentage worst-case influences from all sources and call this the allowable tolerance. However, such an approach ignores the fact that various influences are statistically independent and are as likely to give positive as negative contributions, so the different influences may cancel each other to some extent.

As an illustration of the difference between worst-case and statistical design, consider coin flipping. Suppose one flips a coin 50 times for one dollar each time. Using the *worst-case* situation the loss would be fifty dollars—which would be extremely unlikely. Using the *statistical* approach would allow for a break-even situation. And using the *standard deviation* would allow for a loss or gain of seven dollars.

In statistical design one attempts to find the distribution of some parameters (such as bandwidth, propagation delay, DC voltage) and to let the worst-case be, for example, three standard deviations. If product within three standard deviations of the nominal value all meets the product requirements, the design is judged acceptable. In practice, this may mean that a small percentage of unacceptable product occasionally arises and must be rejected at various tests during manufacturing.

Consider this example: Suppose measurements indicate that a resistor varies ±2% due to variations in mask size, ±2% due to development variations, ±2% due to etch tolerances, and ±2% due to variations in doping level. All of these are independent processes. Worst-case design would say that the error in resistor value is 2 + 2 + 2 + 2 = ±8%. If the statistical approach is used, then the formula is the square root of the sum of squares (i.e., the tolerance) is

$$\sqrt{(2^2 + 2^2 + 2^2 + 2^2)} = \pm 4\%$$

The difference is substantial and arises due to the partial cancellation from different sources of resistor variation. In general, with variations of parameters arising from many independent causes, the worst-case approach gives far too pessimistic a result. Many existing successful IC designs could be proven unworkable by such worst-case methods. Therefore, it is highly recommended that the IC designer become acquainted with basic statistics.

The standard deviations of many important device parameters are given later in this user's guide. In finding the statistical distribution of combinations of components (such as resistors in series or parallel) the following statistical formulas are often needed. Suppose we have two normally distributed random variables x1 and x2, with means m1 and m2 and standard deviations s1 and s2.

Sum or Difference

If we denote the mean and standard deviation of the sum by M and S, then:

$M = m1 + m2$ or $m1 - m2$ (as appropriate)

$S = \sqrt{S1^2 + S2^2}$ (both cases)

Product or Quotient

Denoting the resulting mean and standard deviation by M and S:

$M = m1m2$ or $\frac{m1}{m2}$ (as appropriate)

$S/M = \sqrt{\left(\frac{S1}{M1}\right)^2 + \left(\frac{S2}{M2}\right)^2}$ (both cases)

It is interesting that for the sum and difference case it is possible for the resulting percentage standard deviation to be less than that of either variable. For the product/quotient case the relative standard deviation always is greater than that of either variable.

1.7 Bibliography

Linear IC Design

Analysis and Design of Analog Integrated Circuits (2nd Ed.). Paul R. Gray and R.G. Meyer. J. Wiley & Sons (1984).This is a college-level text devoted to analog IC design. It is highly recommended as the best single book currently available. It covers the various kinds of current sources, methods of temperature compensation, basic gain stages. There is a useful introductory section on the device physics, parameters, and structures of NPN and PNP transistors. The second edition differs from the first primarily in the inclusion of material on MOS analog design.

Bipolar and MOS Analog Integrated Circuit Design. Alan B. Grebene. J. Wiley & Sons (1984). The emphasis of this book is more on the coverage of a wide variety of circuit types rather than on teaching the fundamentals of circuit analysis. It is highly recommended as a reference and source book.

Integration of Analogue Integrated Circuits. J. Davidse. Academic Press (1979). This is not so much a text as a monograph surveying the basic techniques. There is good material on bandgap references and it contains a section on translinear methods for synthesizing complex analog functions.

Feedback. F.D. Waldhauer. J. Wiley & Sons (1982). This book is an excellent source on the general principles of feedback and stability analysis and the design of high-frequency integrated circuits. It also contains worthwhile material on device physics as applied to high-frequency transistor models, and some design examples.

Basic Integrated Circuit Engineering. D.J. Hamilton and W. G. Howard. McGraw-Hill (1975). A general college-level text.

Circuit Design for Integrated Electronics. H.R. Camenzind. Addison-Wesley (1968). This very early IC design text is still useful today, especially for linear ICs.

Device Physics

Physics and Technology of Semiconductor Devices. Andrew S. Grove. J. Wiley & Sons (1967). This is a very early text on device physics, and is still one of the better ones. It was developed for an in-house course given to engineers and technicians at a time when colleges did not teach semiconductor courses. Chapter 5 on the PN junction is particularly outstanding and is highly recommended.

Device Electronics for Integrated Circuits. Richard S. Muller and T.I. Kamins. J. Wiley & Sons (1977). This is a very thorough graduate-level book on device physics. Modeling of the bipolar transistor is covered in great detail, and the Gummel-Poon model is developed in section 6.6. A useful section on Schottky diodes is also included.

Physics of Semiconductor Devices (2nd Ed.). S.M. Sze. J. Wiley & Sons (1981). This is a standard reference work on semiconductor devices of all kinds, and has coverage going well beyond the bipolar transistor. It is not an elementary book and requires a good background in semiconductor physics.

Transistors—Fundamentals for the Integrated-Circuit Engineer. R.M. Warner and B.L. Grung. J. Wiley & Sons (1983). This is a monograph on the basic device physics of both bipolar and MOS transistors, and covers the subject in great detail.

Modeling the Bipolar Transistor. I. Getreu. Tektronix Inc., Portland OR (1976). This short work goes into the basic modeling parameters and discusses the procedures needed to get the required model parameters from electrical measurements. It is not sold through book dealers but can be ordered from Tektronix (Part No. 062-2841-000).

Collections of Papers

Analog Integrated Circuits. IEEE Press (1978). Ed. by Alan B. Grebene. A collection of papers on predominantly bipolar designs, including work on op amps, data converters, phase-locked loops, and more. This book is highly recommended to get the flavor of how analog chips are designed.

Integrated-Circuit Operational Amplifiers. IEEE Press (1978). Ed. by R.G. Meyer. Collected papers on op amp design.

Analog MOS Integrated Circuits. IEEE Press (1980). Ed. by P.R. Gray, D.A. Hodges, and R.W. Brodersen. Papers on the developing field of FET analog design.

Modern Active Filter Design. IEEE Press (1981). Ed. by R. Schaumann, M. Soderstrand, and K. Laker. A collection of papers on the special subject of filters.

Data Conversion Integrated Circuits. IEEE Press (1980). Collected papers on ADCs and DACs.

2. NPN TRANSISTORS

2.1 NPN Transistor Properties and Usage

The transistor types described here differ very little in most of their properties—their main difference being current-handling ability. All of the NPN transistors have about the same frequency response, breakdown voltage, β, etc. Because the transistors are of different sizes, there are also significant differences in parasitic capacitance.

The transistor SPICE model parameters such as capacitance and resistance are given in the SPICE Models section. Matters relating to transistor usage are also covered. The usage conventions extend beyond the basic model parameters, but are nevertheless part of the overall set of design conventions. The usages (such as those relating to transistor matching) have grown up with experience in bipolar analog design, and should be followed carefully.

Each transistor has a maximum collector current. This is given in the SPICE Models section but is not a SPICE modeling parameter. The values are based on the boundary between low-level and high-level injection effects, saturation due to the internal collector resistance, etc. The unity-gain frequency f_T of a transistor varies with collector current, and in most cases, the highest unity-gain frequency occurs at about the rated maximum collector current. The onset of high-level injection is not sudden; the SPICE models show no unusual behavior at this current. The maximum Ic is the instantaneous collector current/bias current plus signal current.

The various transistors also differ in purpose. Many of them are optimized for specific uses (low noise, tight matching).

The SPICE models become progressively less accurate for high currents due to high-level injection effects. Predictions can be rather far off. A more detailed discussion of frequency response versus bias current can be found in Gray and Meyer (Sec. 1.4.8).

It is up to the designer to keep the current below the stated maximum by suitable design (i.e., by appropriate choice of the resistor values). VTC takes no responsibility for the accuracy of the device models above the stated maximum collector current.

Because of the limits on Ic, several transistor sizes are provided with different current-handling capacities. Multiple parallel transistors can also be used to increase current handling capabilities. It is desirable to use the smallest device which meets your needs. In typical designs, 90% of the transistors will be the minimum geometry (i.e., the smallest transistor which can be built under the given design rules).

The maximum Ic given in the SPICE Models section may be too much for certain applications. As the maximum Ic is approached, the temperature and voltage dependences of the transistor currents begin to change due to high-level injection. In particular, the collector current is no longer proportional to $EXP(V_{be} / kT)$, but gradually goes over to $EXP(V_{be} / 2kT)$, and has an intermediate behavior in the transition region. For most circuit types this is not very important, but for temperature-compensation circuits it is. An example of a circuit where this makes a difference is a bandgap reference. It is strongly suggested that such a circuit be designed with a maximum Ic at most only one-third the given maximum for the transistors used in the temperature-compensation part of the circuitry. High temperature is the worst-case for high-level injection effects.

The use of NPN transistors in the inverted mode is a forbidden practice. This is done because 1) the inverted β is inherently low for these processes (about 2); 2) there are no manufacturing procedures in place to monitor and guarantee the parameters in the inverted mode; 3) no detailed characterization of inverted-mode operation has been done; and 4) inverted-mode operation inescapably produces a very substantial substrate current because of a lateral PNP parasitic.

2.2 Choosing the Collector Current

It is stated above that there is a maximum collector current, and the reasons for this were discussed. Apart from this, the designer is free to choose the operating current at will. It should be pointed out, however, that experience with metal-can discrete transistors is not a good guide in choosing the current. Because the parasitic capacitances are so low on a chip, the typical operating currents are much lower than for discrete designs.

A minimum-geometry NPN has only a few tens of fF CB or EB capacitance at zero bias. At higher reverse-biases (the normal condition) it will be even less. A typical resistor parasitic capacitance may be only .05 pF to .1 pF. Thus, 1 mA of charging or discharging current is sufficient to produce slew rates of more than 1 V/ns for these capacitances.

The designer accustomed to discrete components should rethink the situation when working on a chip. In general, 1 mA is a large current on-chip and will often produce a response much faster than needed. If the response is substantially faster than needed, the current should be cut. In the first place, if the speed is not needed, why pay for the power?

In the second place, a high-speed stage is much more likely to oscillate. The frequency response of a transistor can be adjusted by varying the collector current. If only a small bandwidth is needed, the transistor can operate at low current. Circuitry which operates at audio frequencies, for example, can probably operate with a few mA of collector current. A graph of the unity-gain frequency versus collector current, which illustrates the basic behavior, can be found in Gray and Meyer, Fig. 1.25.

It can be seen from this discussion that it is quite important to estimate the load capacitances correctly. Only if the load capacitance is known reasonably well can the designer confidently choose the operating current. That is why much care and time has been taken here to describe and specify *all* of the parasitic capacitance sources.

How far can the designer go in cutting the collector current? Clearly, if the circuit only needs a response of 5 kHz, then in principle the current can be quite small. Operating currents in the 10 to 100 μA range are common in analog IC design. It is recommended that the ON collector current be kept above 1 μA. If there is a good reason for using an even lower current, consult VTC to discuss the application and its requirements.

2.3 NPN Transistor V_{be} Matching

V_{be} matching is important in a number of kinds of circuits; for example:

- Differential amplifiers and op amps
- Current mirrors
- Active current splitters (emitter weighting).

Here it is desirable to have V_{be} versus Ic curves which are identical for the two transistors. Real bipolar transistors provide this to a good degree, but matching is not perfect. In fact, it has been found that the matching is dependent to some extent on the layout geometry. Table 2.1 gives measured NPN matching data.

Table 2.1: CBP NPN Transistor Matching

Name	Standard Deviation of Offset Voltage
T6NW	1.2 mV
T40NW	0.5 mV
TLN1	0.4 mV

The offset voltage is defined here as the voltage difference which must be applied between the inputs of an emitter-coupled pair to produce exactly equal collector currents. VTC's data shows that the offset voltage is independent of collector current.

Additional contributions to offset in finished (packaged) chips come from a) temperature gradients on the chip (Section 7.12), and b) stress gradients arising from packaging operations (Section 7.13).

Detailed measurements have shown that the mismatch between two identical transistors can be modeled quite accurately as a difference in effective junction area. Detailed measurements show that this model accounts for both the current and temperature dependences of the offset voltage.

A consequence of this model for offset voltage is that the offset voltage is proportional to the absolute temperature. This is important for offset-trimming schemes in which the designer wishes to perform a trim operation at room temperature and achieve a situation where the offset voltage is effectively trimmed for all temperatures.

There is sometimes a need for computer (SPICE) modeling of the V_{be} mismatch. This is done by changing the saturation current (I_S)* of one of a pair of matched transistors (this is equivalent to altering the effective EB junction area). An alternative way to do this in SPICE is to change the transistor area factor (i.e., use an area factor of 1.08 to generate a 2 mV offset).

While the V_{be} matching quoted above is quite good, in many cases the designer will want to have an even lower offset voltage. A common method for lowering the offset still further is with the use of centroid-weighted quads of transistors. In this arrangement an emitter-coupled pair is made up of four identical transistors. These are spatially arranged such that one of each pair is on the left and right, and one of each pair on the top and bottom. Thus, gradients in the process parameters and chip temperature tend to cancel out. Improvements of 3:1 in offset have been reported using this method. An illustration of a centroid-weighted quad can be found in Gray and Meyer (Fig. 6.30).

In working with centroid-weighted quads, great care should be taken in the metal routing and length. When an offset voltage below 1 mV is needed and

**The standard deviation of I_S, denoted $\langle I_S \rangle$, is related to the standard deviation of the input offset voltage $\langle V_{OS} \rangle$ by the equation:*

$$\langle I_S \rangle / I_S = \langle V_{OS} \rangle / (kT/q)$$

(See Gray and Meyer, secs. 3.6.1 and 3.6.2).

the current is substantial, the IR drops in the metal can be an important design consideration. In general, an arrangement with the greatest degree of symmetry is best.

Emitter area ratios are not accurately maintained between different transistor geometries. If emitter area ratioing is to be used, it must always be done using multiple identical transistors in parallel.

Many analog circuits operate with current supplied by an active current source. This consists of a transistor with its base tied to some DC voltage and its emitter connected to a DC supply voltage either through a resistor or directly. Unless there is some truly compelling reason to the contrary, all active current sources should have a ballast resistor between the transistor emitter and the supply line, typically dropping 100 to 500 mV across this resistor. Occasionally, schematics can be seen where this is not done (e.g., in current mirrors), but this is a hazardous practice. The reason for this is that metal supply lines on a chip are not all at the same potential. The aluminum metal is not a perfect conductor, and it is common to see up to 20 to 30 mV potential differences between different points on the supply metal for a large chip. If no ballast resistors were used, supposedly identical current sources at different places on the chip would have substantially different output current. The occurrence of large currents for certain transistors in favorable locations is often described as current hogging, and is always a hazard for common-emitter stages. Of course, immediately adjacent points of a metal supply line will not have nearly this much difference in supply potential.

Another reason for the ballast resistor is that it cuts down the voltage gain of the current source transistor. This is desirable in order to reduce the likelihood that the current source will oscillate.

2.4 NPN Transistor β Matching

In several types of circuits (such as base current cancellation circuits) close matching between β of different transistors is important. In constructing a statistical model for β, the designer should assume a normal distribution with the following parameters:

MEAN: Bo (see Section 2.7 and App. A)
STD. DEV.: .012 Bo

Bo will differ substantially for different transistor geometries, so matched β devices should have the same geometry.

2.5 Low-Noise Amplifiers

The dominant factor in broadband input noise is often the base resistance. In order to achieve very low noise, special transistor geometries are used which have many long, narrow emitter stripes such as the TLN1. Low noise is also favored by the use of high collector currents, which reduces shot noise. A good treatment of the basic principles governing electrical noise in analog ICs can be found in Gray and Meyer, Chapter 11.

Because low-noise input transistors are designed with very low inherent base resistances, it is often important to estimate the amount of noise arising from the resistance of the metal interconnection lines. This may not be negligible, and wider-than-minimum lines may be required, or placements such that metal runs are quite short. Data on metal line resistances is found in Part 6.

2.6 NPN Transistor Saturation

It is strongly urged that the designer does not operate any transistor in saturation, even momentarily. There are several reasons for this (discussed in more detail in Part 7):

- The models are a lot less accurate under these conditions. In particular, ON-OFF delay may be poorly predicted, so that the designer is reduced to guesswork about the circuit performance.
- There is a parasitic substrate PNP in every normal NPN transistor, and this device gets turned ON in saturation. This results in significant amounts of substrate current, which can have unpredictable effects on circuit operation.
- The parasitic substrate PNP does not appear in most schematics, and is not modeled in the usual modeling programs (unless the designer deliberately adds a transistor to represent it). The parasitic PNP usually has a β substantially more than 1, so that it can contribute to thyristor latchup.
- If there is significant substrate current it can alter the substrate potential and cause collector-substrate junctions to become forward-biased. The resulting injected minority carriers can cause many kinds of circuit mischief.

It is usually possible to avoid saturated operation. An emitter-coupled pair, for example, can usually be designed so that no transistor saturates by choosing appropriate resistor values and ratios. While undesirable things can happen when the parasitic PNPs are turned ON, bipolar ICs are biased in such a way that

they usually never get turned ON, and they can be ignored. Saturation of an NPN is one of the few ways this lurking parasitic transistor can be turned ON.

If it is unavoidably necessary to use saturating operation, Schottky-clamp the transistor (Schottky-clamped transistors are discussed below). The effect of the Schottky diode is to divert the normal base-collector forward current which flows in saturation through the Schottky diode, which is a noninjecting diode. The parasitic lateral PNP never turns ON, and need not be modeled.

The properties of the parasitic substrate PNP are discussed in more detail in Part 7.

2.7 NPN Breakdown Voltages and β

The reverse (avalanche) breakdown voltages are not model parameters in SPICE. The designer must keep them in mind and recognize when they are exceeded. As long as the rated supply voltage for this process (12 V maximum between nominal supply voltages) is not exceeded, problems related to avalanche breakdown occur in only a few circuit configurations.

In general, there are no breakdown voltage problems for 5 V circuits, since no breakdown voltage is exceeded in this case.

For 10 and 12 V circuits the supply voltage can exceed the EB breakdown voltage, and it can also exceed BV_{ceo}. These problems must be overcome by suitable design. The EB junctions must never be subjected to more than about 4.5 V of reverse-bias. If the emitter-base junction of a transistor undergoes reverse breakdown even briefly, damage is done to the transistor and its β is irreversibly degraded. BV_{ceo} breakdown only occurs if the base potential is floating (i.e., if the base is driven at a low (<1 kΩ) impedance level, the much higher BV_{cbo} figure applies). In most cases an NPN will be held OFF through a resistor or transistor (i.e., a low-resistance path).

In practice, there are occasionally problems with breakdown voltages due to inductive loads. When one attempts to switch the current through an inductance rapidly, a large voltage L(dI/dt) is developed. Table 2.2 gives the worst-case and typical values of the breakdown voltages and β.

Table 2.2: CBP NPN Breakdown Voltage and β

Parameter	Min	Typ	Max
BV_{ces}	1.5	20	25
BV_{ebo}	4.6	4.9	5.2
BV_{ceo}	6.0	—	—
β*	70	100	150

**For integrated transistors there is some problem of definition for β because β is different for different geometries. This is fundamentally related to the perimeter-to-area ratio of the transistor. In general, transistors with larger emitters will have higher β. The specification given above is to be taken as worst-case in that it covers all NPN transistor geometries. The different β for different geometries is sometimes important in base current compensation schemes, which generally assume identical β for all NPN transistors.*

The value of BV_{ceo} depends strongly on β, and the minimum value would correspond to maximum β. For the typical β, BV_{ceo} will be higher than given here.

2.8 NPN Output Impedance

The usual conceptual model of a bipolar transistor is one in which the collector current is independent of the collector voltage (i.e., an ideal current source). In reality, the collector impedance is high but finite.

The variation of the collector current with collector voltage is called the Early effect, and is modeled by a SPICE parameter called the Early voltage (VAF). A high Early voltage corresponds to a high output impedance and vice versa. The value of the Early voltage is often of importance in modeling active-load amplifiers, current mirrors, etc.

Both theory and measurement show that the Early voltage VAF is strongly correlated with β, and that

$$VAF \cdot \beta = \text{const.}$$

For the NPN transistors the measurements give:

$$VAF \cdot BF = 5200$$

Where:

BF is the SPICE parameter for β.

This relation only holds for NPN transistors. Similar relations (but with different constants) hold for PNPs (see Part 3).

Since β varies from run to run, VAF will also vary. However, in a number of cases (such as the Wilson current mirror) the output impedance is proportional to the product VAF • BF and is thus largely process-independent.

2.9 NPN Transistors with Schottky Clamp Diodes

Schottky diodes are widely used in bipolar IC technology, primarily in digital ICs. They also have a place in analog ICs (which today often include digital circuitry as well). The important facts about Schottky diodes are given in Sections 4.2 and 4.3.

The main reason for using Schottky-clamped transistors is that they get around some of the consequences of saturation. Such a transistor has a Schottky diode in parallel with its CB junction. When the transistor is driven into saturation, instead of the CB junction becoming forward-biased, the excess base current is bypassed by the Schottky diode and shows up as normal collector current. This has favorable consequences for switching speed. When we speak of saturation of a Schottky transistor, we do not mean real saturation but this kind of quasi-saturation in which the collector-emitter potential is forced to a low value.

In many respects the Schottky-clamped NPN can be used like a saturating NPN transistor is normally used. There is, however, one significant difference in the DC behavior. The saturation voltage V_{ce}(sat) is substantially higher than for a non-Schottky-clamped transistor. A typical V_{ce}(sat) without Schottky clamping is <50 mV, while for a Schottky NPN V_{ce}(sat) = 200 to 250 mV typically.

A Schottky transistor is easily created by adding a Schottky diode. The VJ900 series master chips provide a substantial number of Schottky diodes for this purpose. The Schottky diode requires a separate model element, and because such a transistor operates in saturation, the parasitic (base, collector, emitter) resistances are more important.

In the design of common-emitter stages with Schottky NPNs, the base current substantially exceeds Ic/β. The ratio of total Ic to total Ib is called forced β. For switching applications (TTL outputs for example) forced β should be between 5 and 10.

3. PNP TRANSISTORS

3.1 Vertical PNP Transistors

The VJ900 series master chips provide fast vertical PNP transistors. The electrical performance of these transistors is greatly superior to the commonly-used lateral PNP transistors found in most bipolar linear processes. This is reflected in wider bandwidths, faster switching, and greater current-handling capability. The PNP transistors in the VJ900 series master chips are the fastest PNPs currently available in master chip form. This does not mean, however, that a given circuit block can be freely chosen to use PNP or NPN transistors. The PNP transistors remain about 10X slower than the NPNs, and their use in the signal path should be carefully considered in light of the speed and bandwidth requirements. In some cases, the PNP transistor may be preferable because of its higher emitter-base breakdown voltage—in amplifier inputs, for example. The slightly better V_{be} matching of PNP transistors is also advantageous in some situations.

3.2 PNP Current Mirrors and Active Loads

Current mirrors are a common use for PNP transistors. The following summarizes some of the important points in the application of such current mirrors:

- In many cases the accuracy of the mirror ratio can be improved by using emitter resistors (similar to the ballast resistors used for current sources). This is discussed further in VTC *Design Note DN-1*.
- The Early voltage VAF is an important parameter for current sources and active loads. The output impedance of a Wilson mirror, for example, is given by (Gray and Meyer, sec. 4.2.3):

$$R_o = \frac{\beta \cdot VAF}{2\, I_C}$$

Where:

R_o is the output impedance.
VAF is the Early voltage.
β is I_C / Ib for I_C << IKF.
I_C is the collector current.

Device theory predicts that VAF correlates with β in such a way that

$$VAF \cdot \beta = C$$

to a good degree of approximation. VTC's measurements directly confirm this. We find for the SPICE parameter BF which controls β:

$$VAF \cdot BF = 1500.$$

The SPICE parameter BF is approximately equal to the low-current β (I_C << IKF). The analogous relation for β at higher currents has a different constant. This correlation between β and VAF gives the pleasing conclusion that output impedance is roughly independent of processing variations for a Wilson mirror.

3.3 PNP Breakdown Voltages and β

The CBP process has the PNP breakdown voltages and β as shown in the following table:

Table 3.1: Vertical PNP Breakdown Voltage and β

Parameter	Min	Typ	Max	Condition
BV_{ces}	—	—	—	Ic = 5 µA
BV_{ebo}	12	>10	—	
BV_{ceo}	12	—	—	Ic = 5 mA
β	50	75	180	Ib = 2 µA Vce = 2.5V

3.4 PNP Transistor Matching

The conditions and definitions for transistor matching for NPNs are described in Section 2.3 , and the same remarks apply here. The matching standard deviations for the PNP transistors are shown in the following table:

Table 3.2: CBP PNP Transistor Matching

Name	Standard Deviation of Offset Voltage
TVPA8	0.5 mV
PVPA35	0.3 mV

3.5 Modeling the Vertical PNP Transistor

The SPICE model for the vertical PNP is the same as for the usual vertical NPN. There are no extra elements to contend with as with lateral PNPs. However, the collector of the vertical PNP is a P region surrounded by an N region at V_{CC}, so the substrate node for the vertical PNP in SPICE simulations is V_{CC}—the most POSITIVE supply voltage. Detailed listings of the SPICE model parameters for the PNP transistors are given in the SPICE Models section.

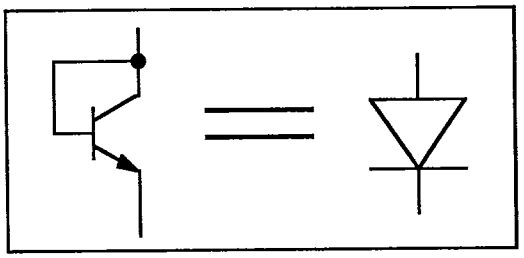
T-42-21

4. DIODES AND CAPACITORS

This part of the VJ900 User's Guide covers diodes—both those used as active circuit elements and those occurring as isolating elements in the structure. The latter are mainly of interest because of the need for accurate modeling of their capacitance. In addition to active and parasitic diodes, capacitors are also covered.

4.1 The Diode-Connected NPN Transistor

Schematic diagrams of analog circuits frequently show diodes using the usual arrow symbols. In 99% of the cases such a diode is really a diode-connected NPN transistor. Here the base and collector are connected together, as shown below:



One often sees this element in circuit diagrams as a base-collector shorted transistor—in which case one can conclude that the transistor is used as a diode. While other kinds of diode can be made, there are some great advantages to this form of diode which account for its near-universal use:

- The voltage drop across the diode precisely matches the V_{be} of an NPN transistor carrying the same emitter current.
- This form of diode injects minority carriers only into the thin active base region. Consequently, it has a fast turn-off.

Other forms of PN junction diode will inject minority carriers into the substrate, where nearby PN junctions can act as collectors, giving rise to spurious currents in them. The relatively long recombination times for carriers in clean silicon also make such diodes relatively slow to turn OFF. It can be seen that this diode is really not a simple PN junction, but rather a feedback circuit in which the current gain of the transistor acts to clamp the collector voltage at V_{be}. One limitation of this type of diode is the reverse breakdown voltage of about 4.5 V (BV_{ebo}). In cases where a higher breakdown voltage is needed, the guard-ring Schottky diode (see below) may be preferable. Diode-connected transistors are sometimes operated in reverse breakdown, in which case they are referred to as Zener diodes (see Section 4.6). The SPICE model for a diode-connected transistor is just the transistor model with a CB short.

4.2 Schottky Diodes

The VJ900 series master chips allow the use of Schottky diodes. The properties of a Schottky diode are summarized as follows:

- The Schottky diode is a metal-semiconductor junction and is created by directly contacting metal (PtSi) to silicon.
- The nature of the contact formed depends on the doping level of the silicon. Good Schottky diodes are only formed on lightly-doped silicon. On heavily-doped Si the tunneling of carriers through the junction barrier predominates, and the contact is ohmic.
- In the usual bipolar process, the N- epi region forms the semiconductor part of the diode. This N region results in parasitic elements which are described in Section 4.3
- For Schottky diodes on N- silicon, the forward current flows when the metal is + relative to the silicon.
- A key property is that Schottky diodes inject no minority carriers. In our case, the current is entirely made up of electrons. For this reason the diode is very fast.
- The PtSi process is used for the Schottky diodes in the VJ900 series master chips. This provides a diode with a relatively high forward turn-on voltage and provides good uniformity and repeatability of the Schottky diode characteristics.
- The reverse current of a Schottky diode follows the same laws as that of a PN junction diode, and the reverse breakdown occurs by the same mechanism (avalanche breakdown) as in PN junctions.
- There is a maximum current for Schottky diodes. The forward current SHOULD NOT EXCEED 0.2 mA for the small Schottky diodes in the VJ900 series master chips or 10 mA for the large Schottky diodes near the output pads. When the forward voltage of a Schottky diode is too high, it can inject, which can lead to PNP parasitic problems (see Part 7).

Probably the biggest use of Schottky diodes is for antisaturation clamps in Schottky TTL and other circuits. They are also used for suppression of parasitic transistor action.

When a Schottky diode is properly connected in parallel with a transistor CB junction they both have the same direction of rectification, but the Schottky diode turns ON at a lower forward voltage. Thus, it bypasses almost all of the forward current of the PN junction. The forward current now flows without injection of minority carriers. It is this property which allows one to suppress parasitic PNP transistors by placing a Schottky diode in parallel with the CB junction.

One of the problems occurring in the use of Schottky diodes is that of premature reverse breakdown and leakage. The edge of a metal-silicon contact is very abrupt—not rounded by side diffusion like a diffused region. Because of this, the electric field concentrates very sharply at the edge of the diode under reverse bias, and avalanche breakdown occurs here long before bulk avalanche breakdown is reached. In order to evade this problem certain special geometries are used. In the VJ900 all of the Schottky diodes are of the guard-ring type.

In guard-ring Schottky diodes, the edge of the Schottky contact is made to terminate at a P type ring. The electric field lines terminate on the rounded P type region and not at the edge of the contact. The breakdown voltage will be approximately the same as BV_{cbo} for an NPN ($BV_{cbo} > BV_{ces}$; see Section 2.7).

4.3 Schottky Diode Parasitic Elements

The N region (cathode) of the Schottky diode is formed from an epi-and-buried-layer tub, and this results in substantial parasitic elements. These parasitic elements are shown in the schematic diagram below for the Schottky diode used in the VJ900 series master chips.

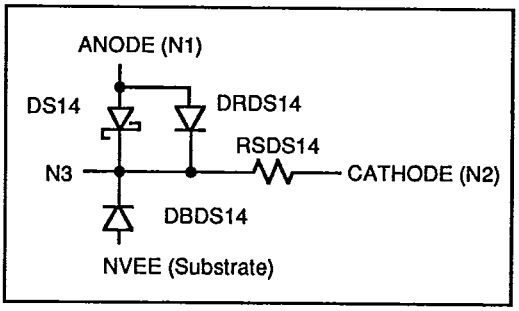


Figure 4.1: Parasitic Elements Used in the SPICE Simulation of a VJ900 Schottky Diode

The SPICE element statements corresponding to this schematic diagram are:

```
Minimum Schottky:
DS14 N1 N3 SCH3 71
RSDS14 N2 N3 103 TC = 0.004
DBDS14 NVEE N3 DRN 0.246 OFF
DRDS14 N1 N3 DRP 0.053 OFF

I/O Clamp Schottky:
DS14 N1 N3 SCH3 1682
RSDS14 N2 N3 17.4 TC=.0005
DBDS14 NVEE N3 DRN 1.21
DRDS14 N1 N3 DRP .30
```

RSDS14 is the series resistance of the body of the diode. DBDS14 is a parasitic diode representing the parasitic capacitance to the substrate. DRDS14 is a parasitic diode representing the capacitance of the guard-ring.

4.4 Junction Capacitors

Junction capacitors are useful for a number of purposes. While many capacitor uses call for true linear capacitors, some kinds of analog circuitry require capacitors for stabilization (i.e., in order to keep the circuit in its stable condition and prevent oscillations). This is true of many kinds of feedback circuits. Feedback is a powerful tool for improving the precision of analog circuitry, and consequently the need for rolloff or compensation capacitors arises fairly often. In most cases it is the value of the capacitance rather than linearity that is important; the functional operation of the circuit is satisfactory with a nonlinear capacitor because the signal voltage swings are small. Because junction capacitances are voltage-dependent, the capacitor must be big enough to adequately compensate the circuit at the worst-case high DC voltage applied across it. An example of a circuit type which often needs rolloff capacitors is a bandgap reference circuit. In this case the output is a DC voltage, and the nonlinearity of the junction capacitor is of no importance. Junction capacitors are usually operated under fairly low reverse-bias. (The polarity convention calls for the most positive voltage on the N region for a reverse-biased junction capacitor.) This is done because the capacitance is voltage-dependent and is highest with a low bias voltage, and because the reverse breakdown voltages for the junction capacitors with the highest capacitance density are fairly low. A circuit using junction capacitors must be designed such that the junction capacitor never gets forward-biased (even under transient conditions such as chip power-up). Such forward-bias can lead

to severe parasitic problems (see Part 7). The use of a Schottky clamp diode in parallel with the junction capacitor is another solution to parasitic transistor problems. The ratio matching should be 1% or better for identical junction capacitors. The temperature dependence of C is quite weak, and comes in through the weak temperature dependence of the built-in voltage (see Grove, listed in the references). The worst-case absolute tolerance on junction capacitor values should be taken as ±15%. In cases where the junction capacitors are used as rolloff or compensation capacitors in DC circuits, it is very common to connect the capacitor such that it is a Miller capacitor for a common-emitter transistor. This multiplies the effective capacitance by the voltage gain of the stage, and permits a small capacitance to act like a much bigger one. The kinds of junction capacitors available in the VJ900 series master chips are limited.

Collector-base capacitor

In this case, the positive terminal is the collector region of an NPN transistor (or the base region of a PNP) and the negative terminal is the collector region of an NPN (or the base region of a PNP). This type of capacitor has high breakdown voltage, but a modest capacitance per unit area. In the VJ900 series master chips these junction capacitors are made using the base and collector connections of an otherwise unused transistor. The capacitance at V=0 is just the SPICE parameter CJC. The voltage dependence of this capacitance versus the collector-base bias voltage V_{cb} is represented in SPICE by:

$$C(V) = \frac{CJC}{\left(1 + \frac{Vcb}{VJC}\right)^{MJC}}$$

The needed parameters can be found in the SPICE transistor model listings in the SPICE Models section.

Capacitor-connected NPN transistor

The E and C electrodes are connected together (i.e., both N regions). This places the EB and CB junctions in parallel, and increases the total capacitance. Note that the reverse voltage cannot exceed the minimum BV_{ebo} of an NPN transistor (about 4.5 V, but typically should be taken at 4 V max in practical designs). This type of capacitor can be made with any of the NPN transistors on the chip. Usually, unused low-noise or output driver type NPN transistors are the best ones to use since they are geometrically large and have large parasitic capacitances.

The capacitance at zero bias is just the sum of the SPICE parameters CJC and CJE. The dependence on bias voltage V_{bias} is given by:

$$C(V) = \frac{CJC}{\left(1 + \frac{Vbias}{VJC}\right)^{MJC}} + \frac{CJE}{\left(1 + \frac{Vbias}{VJE}\right)^{MJE}}$$

It is sometimes found that junction capacitors will have excessive reverse leakage currents at high temperatures due to the rather large junction areas involved. The models which are defined here should take this into account in a realistic way. In cases where significant leakage current is a problem, the amount of high-temperature leakage current should be carefully checked with a high-temperature SPICE simulation.

4.5 Parasitic Diodes

All of the parasitic and junction capacitor diodes mentioned above are usually operated under reverse-bias. Consequently, in modeling, most of the forward-bias parameters will go to their default values. The Schottky diode is an exception to this. Parasitic capacitances occur in many sizes, and one must account for this in simulations. The means used for this is the area parameter in diode statements. The area-dependent parameters of the diode in the .MODEL statement are multiplied or divided by this factor for the particular diode in the statement. Depending on the situation, the diode .MODEL is defined in one of two ways: the .MODEL statement can refer to a diode of unit area (usually 1 sq. μ) or unit capacitance (usually 1 pF). Then a diode statement with an area of K represents a diode of physical area K sq. μ or K pF (at V = 0). The transistor and resistor parasitic diodes are represented by models of unit capacitance (1 pF). This is desirable because the effective area of the junction capacitor bears little direct relation to the as-drawn layout area. It includes the capacitance of vertical sidewalls, is affected by lateral diffusion, edges, etc. In writing the diode statement the designer needs C(0) in pF, and this is given in this user's guide. The unit used to define the .MODEL is given for each junction type in the following Table 4.1 (following page). Here, SPIC1 and SPIC2 refer to different SPICE revisions. As an example of the method for representing parasitic diodes, consider a diode between an N tub and the substrate (e.g., the body of a junction capacitor). Suppose the junction has 2.85 pF of capacitance at V = 0. Since it is a capacitance to the substrate, it is the

capacitance of an N region and hence uses the model DRN. The appropriate SPICE .MODEL statement is:

.MODEL DRN (IS=2E-19 CJO=1E-12 VJ=.63 M=.42)

This statement suffices for any number of DRN-type parasitic junctions called by separate diode statements. Only those parameters needed for capacitance modeling are used—the rest are defaulted. For the case at hand, if the designer calls a diode D27 where the N region is node 19, the following SPICE statement will be used:

D27 NSUB 19 DRN 2.85

Where:

NSUB is the substrate node number.

Table 4.1: Diode Model Parameters

PARASITIC AND SCHOTTKY DIODE MODELS				
Parameter name	Model name and value*			
SPICE 2G.6	DRP	DRN	DBE	SCH3
IS	2E-16	2E-16	2E-16	4.7E-16
N	D	D	D	1.02
CJO	1E-12	1E-12	1E-12	5.6E-16
PB	.81	.63	.91	.83
M	.39	.42	.34	.50
RS	D	D	D	4000
–	D	D	D	.0040
BV	D	D	D	15**
EG	D	D	D	.83
XTI	D	D	D	2
Area unit	1 pF	1 pF	1 pF	1 sq. μ

**Some of the parameters listed above are given as "D". These are to go to their default values. The reader will note that the different simulation programs use slightly different sets of parameters (i.e., not all parameters enter all lists).*

***The worst-case low breakdown voltage for a Schottky diode differs for the different geometries. For a guard-ring type diode it is equal to BV_{cbo} ($>BV_{ces}$) for the NPN transistor (see Section 2.7).*

4.6 Zener Diodes

The Zener diode is really just the diode-connected NPN transistor used in reverse (avalanche) breakdown of the EB junction. The designer cannot use the usual SPICE transistor model, however, since it does not permit the inclusion of a breakdown voltage. There are several things which a designer should think about when using Zener diodes:

- There is a substantial manufacturing tolerance associated with the Zener voltage. The circuit must be designed so it will allow this. The Zener voltage is just BV_{ebo} (values given in Section 2.7).
- Zener diodes may have noise arising from microplasmas. These are localized avalanching regions which may turn off and on, resulting in a rather irregular source of low-frequency noise. Whether a given Zener has this kind of noise or not often depends on the occurrence of localized defects, and the incidence of microplasma noise is probably low (i.e., it is a yield and AQL factor).
- Zener level shifters offer few problems where digital signals are passed. When analog signals are passed through Zeners their use is more questionable, especially if the analog signal is at a low level.
- Zener diodes are susceptible to permanent damage from current surges. Therefore, they should not be connected directly to I/O pins in order to avoid electrostatic discharge damage.
- The reproducability and matching of the Zener voltage is poor at low current levels (see Section 4.7
- The use of Zener diodes for creating DC reference voltages is not recommended due to drift and aging problems seen with these circuits. Bandgap-type DC reference generators are the preferred approach. The Zener models for this process should be regarded as preliminary due to limited data and experience. To find the worst-case limits on the Zener voltage at room temperature the designer can look under BV_{ebo} in Section 2.7

4.7 Zener Matching

In many instances there will be a need to use Zener diodes as matched elements—for example, in level shifters for differential signals. Data taken previously on other similar processes indicates the following for minimum-geometry Zener diodes:

- With 100 μA current, the standard deviation of the difference in voltage dropped across two identical minimum-sized diodes will be about 4 mV.
- With 10 μA current, the standard deviation of the difference will be 50 to 100 μV.
- With currents greater than 100 μA, the matching improves slightly. The Zener current should not exceed the maximum rated Ic for the corresponding NPN transistor.

4.8 Dielectric Capacitors

The CBP process inherently features thick and thin oxide regions. The thin oxide regions can be used as capacitors. There is only one such capacitor geometry available on the VJ900 series chips. Larger capacitors can be created by paralleling several of them. The SPICE model for such a capacitor is given below in Section 4.9. The oxide capacitors have first metal as one plate and a P+ silicon region as the other plate. The P+ lower plate always has a substantial parasitic (junction) capacitance to a surrounding N region. The N region in turn has a parasitic capacitance to the substrate (V_{EE}). Thus, a capacitor is a four-terminal device here (upper plate, lower plate, N tub, substrate), with three terminals (all but the substrate, which is at V_{EE}) avaliable for connections. It is possible in some cases to neutralize the effect of the capacitance from the lower plate to the substrate using the N-tub. This N region can be driven with the same waveform (with some DC offset) as the lower plate (for example, through an emitter follower) effectively canceling out the parasitic capacitance. The use of dielectric capacitors involves serious reliability hazards (see Part 7). The thin capacitor dielectric undergoes irreversible dielectric breakdown with voltage above approximately 60 V. Such voltages commonly occur due to electrostatic discharge during handling. Because of this, such capacitors must not be directly connected to I/O pins. If there is an inescapable need to connect them to I/O pins, then a suitable ESD protection device must be used at that pin to protect the capacitor from over voltages.

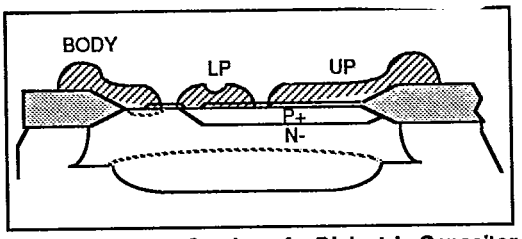


Figure 4.2: Cross Section of a Dielectric Capacitor, Showing the Parasitic Elements

4.9 Substrate Parasitic Elements for Dielectric Capacitors

The upper plate of a dielectric capacitor is the first metal layer, while its lower plate is the silicon substrate. The lower plate (LP in Figure 4.2) has a substantial junction capacitance. The lower plate is a P region and it has a junction capacitance to the N tub in which it is embedded. In SPICE simulations these junction capacitances must be represented as load diodes (see Section 4.5).

The SPICE element listing for a capacitor C1 and its parasitic elements is given below. The node labels are NBDY for the body, NUP for the upper plate, NLP for the lower plate, and NV_{EE} for the substrate.

```
C1 NUP NLP 1.45E-12
DC1A NLP NBDY DRP 1.211 OFF
DC1B NVEE NBDY DRN 0.860 OFF
```

When necessary, a 100Ω series resistance for the capacitor lower plate can be included:

```
RSC1 N1 NLP 100 TC=.00076,2.05E-6
```

The parasitic junction capacitance has a serious influence on the operation of a circuit in any configuration in which the lower plate is not at a DC potential (e.g., at GROUND). Figure 4.3 (following page) shows how the effect of the body capacitance can be largely cancelled (at least at low frequencies) when a P type region is used as the lower plate. Here the PNP emitter follower Q1 acts to maintain a reverse-bias of V_{be} across the parasitic junction capacitor D1. This means that the charge on the junction capacitance of D1 remains the same (provided that the variation of V_{be} for Q1 during under typical dynamic conditions is small) and the amount of charge stored on this capacitance is constant, so that the parasitic junction capacitance has no influence on circuit behavior. The simple emitter follower Q1, R1 can be

replaced by a variety of all-NPN unity-gain buffers in real circuit designs. The arrangement shown in Figure 4.3 does load the lower plate to the extent that base current is drawn by Q1, so that the lower plate cannot be used for dynamic charge storage when long time constants are needed. This can be overcome by using the upper plate for such situations, and in some cases by using base-current cancellation for Q1.

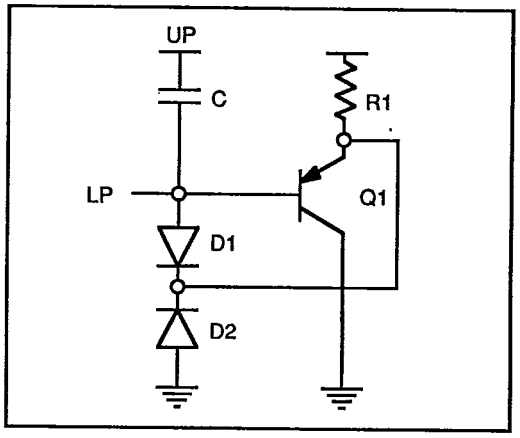


Figure 4.3: An Example of the Use of Active Gain to Cancel Out the Capacitance from the Lower Plate to the Body Region When a P Type Lower Plate is Used

5. RESISTORS

5.1 Basic Facts About Integrated Resistors

An integrated resistor is not as simple to use as a discrete resistor. It is embedded in a silicon chip, and has a substantial capacitance to the underlying silicon region associated with its isolating PN junction. This capacitance is significant, and in some instances may even be dominant, in determining the circuit behavior. It cannot be ignored and must be modeled if good results are to be obtained. The isolating PN junction can also act as an element of a parasitic transistor under some circumstances (see Part 7).

An integrated resistor acts like a distributed RC delay line when fast signals are present. Such a line has an inherent delay. Even if a signal with zero rise time is applied at one end, the signal arrival at the other end will be delayed due to the time needed to charge up the distributed capacitance through the distributed resistance. The delay through the distributed resistor with total resistance R and total capacitance C is approximately RC/2. Further information on resistor capacitance and its modeling is given in Section 5.5.

Doped silicon resistors have a significant temperature coefficient (see Section 5.5) on the order of 500 to 3000 ppm/°C, depending on the doping level. The temperature coefficient is nearly always positive (i.e., R goes up as the temperature rises). Integrated resistors have a voltage dependence (i.e., the value of R depends on the resistor-body bias). This is usually not important for any except the most intricate analog designs. The voltage dependence is greater for resistors with a high sheet resistance such as P- base resistors. The voltage dependence is occasionally of importance for DC design (e.g., in current sources). It may also be significant in a few AC designs, since a voltage-dependent resistor is nonlinear, and hence may contribute to harmonic distortion. The resistor voltage dependence is important in op-amp feedback networks when high precision is expected. With enough open-loop gain it is possible in principle to control closed-loop amplifier gains (or other properties) to a precision of 1 part in 1000 or better. This is not possible if the resistors in the feedback network have voltage dependences such that the amount of feedback depends on the DC operating point of the circuit.

5.2 Resistor Usage in the VJ900 Series Master Chips

In full-custom design, resistors may be of any length and width, and hence can have any nominal value. In a master chip, only a limited set of values are possible which gives rise to the question, "How does one pick the best resistor set?" In setting up the VJ900 series chips, binary-valued multi-tapped resistors have been provided. Such a resistor consists of a stripe of resistive material with four contacts. Thus, it represents three resistors in series. The lengths are chosen so the resistance values of the different segments have the ratio 1:2:4. This arrangement allows the designer to create many different values from a single resistor body.

There are two resistor types: the P+ enhancement resistors with lower values and the P– base resistors with higher values. The nominal values of the resistor segments are given below:

P+ : 260, 521, 1042 Ω
P– : 2013, 4075, 8200 Ω

Each tapped resistor can be used to create 13 different resistor values. These are listed below, and Figure 5.1 shows how the different values would be created for a resistor with 1Ω, 2Ω, and 4Ω segments.

Table 5.1: Resistor Combinations

Series Resistors	Parallel Resistors	Net Resistance Value	
		Enhancement (P+)	Base (P–)
1, 2, 4	—	1823	14288
2, 4	—	1563	12275
1, 4	—	1302	10213
4	1, 2	1215	9547
4	—	1042	8200
1,2	—	781	6088
1	2, 4	607	4735
2	—	521	4075
—	2, 4	347	2722
1	—	260	2013
—	1, 4	208	1616
—	1, 2	173	1347
—	1, 2, 4	149	1157

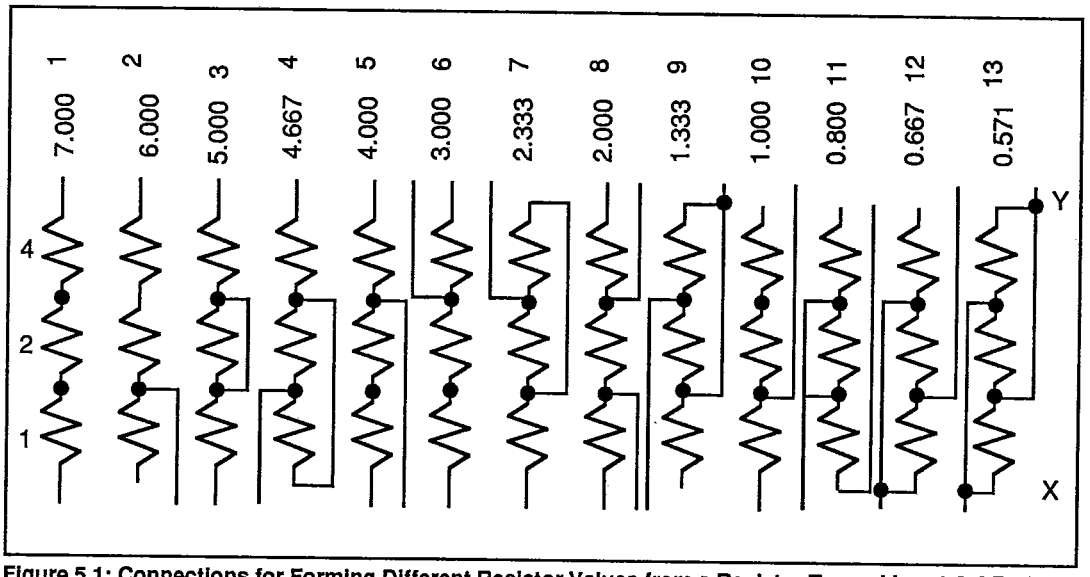


Figure 5.1: Connections for Forming Different Resistor Values from a Resistor Tapped in a 1:2:4 Ratio

5.3 Resistor Parasitic Capacitance and Capacitance Modeling

The distributed delay is readily calculated from the numbers given below. If R is in Ω and C/2 in pF, the product is the time constant in ps. This number should be checked for high-valued resistors to make sure there are no difficulties with a built-in delay. Resistors where the inherent delay is a problem tend to be those with high values. Where the distributed delay is significant, a multi-section RC model should be used in simulations.

The most popular model for a resistor is a "pi" section with a resistor R in the center and C/2 at each end. If either end of the resistor goes to a supply voltage, then the C at that end can be omitted. This model adds no extra nodes to a simulation, and represents the effect of the parasitic capacitance fairly well. It does not, however, represent the effects of the distributed delay. If this is important, a multi-section RC model should be used—for example, a "T" with R/2 at the input and output legs and C from the center of the resistor to ground. Various models for integrated resistors are shown in Figure 5.2. Figure 5.3 shows how these apply to the tapped resistors used in VJ900 series master chips. A resistor is ordinarily thought of as a symmetrical entity—the ends can be reversed without changing its properties. This is not so for an AC model of a segmented resistor.

Study of Figure 5.1 shows that in each case the RC model is nonsymmetric with respect to the ends, i.e., the ends marked X and Y are not equivalent. It is also clear that one cannot just divide the resistance by N for N resistors in parallel or multiply by N for N resistors in series, but must also correctly account for the parasitic capacitance. Many segmented resistor combinations have dangling segments, which make no contribution to the DC behavior of the resistor but do affect its AC behavior. These include types 2, 3, 5, 6, 8, 9, 10, and 12 in Figure 5.1. Such a dangling end must be modeled unless it connects to a DC voltage.

The parasitic capacitance is modeled using a SPICE diode element (see Section 4.5) since the junction capacitance is a nonlinear function of the junction voltage. Table 5.2 gives the zero-bias capacitances of the various resistors.

5.4 Ratioed Resistors

Ratioed resistors are subject to the following rules:

1) For large ratios, series and parallel combinations of resistors with the same L should be used as much as possible.
2) For critical matching applications, the higher-valued (geometrically longer) resistors are more favorable.

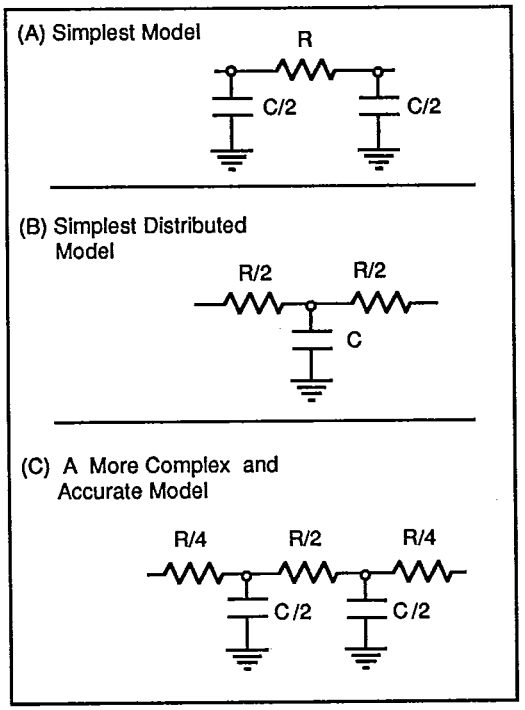


Figure 5.2: AC Models for Integrated Resistors

3) All members of a ratioed set must be of the same type (i.e., do not attempt to ratio base resistors against enhancement resistors).
4) The members of a matched set must be kept as physically close together as possible. Even if the lengths and widths of two resistors track perfectly, there are temperature and mechanical stress gradients across a chip (see Part 7) which can cause resistor value mismatches.
5) Matched resistors will often consist of several resistor elements in series or parallel, so that it is possible to interdigitate the individual elements for two ratioed resistors (i.e., mix them together physically, using metal to connect them suitably*). This minimizes mismatch caused by temperature and stress gradients.

**As an example, consider a situation where there are two matched resistors, each consisting of two segments in series. To interdigitate these a set of four identical resistor cells would be placed in a row. R1 would then be made up from the 1st and 3rd segments, while R2 would consist of the 2nd and 4th segments.*

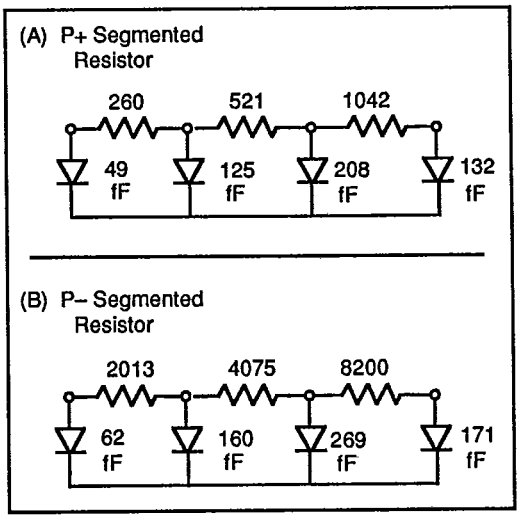


Figure 5.3: Complete Resistor Schematics for the Tapped P+ and P– Resistors Showing the Parasitic Load Diodes

Table 5.2: Resistor Parasitic Capacitance

Type	Value (Ω)	C/2 @ V = 0 (pF)	RC/2 @ V = 0 (pF)
P +	260	.049	13
P +	521	.076	40
P +	1042	.132	138
P –	2013	.062	124
P –	4075	.098	400
P –	8200	.171	1402

5.5 Resistor Temperature Dependences

As noted above, monolithic silicon resistors have a substantial temperature dependence. This is usually expressed in simulation programs in terms of a TCR expressed as fractional change per °C, with a reference temperature of 27°C (300K). For example, if there was a resistor with a variation of 2500 ppm/°C the simulation program would express this by the equation:

$$R_T = R_{27}\,(1 + t_{c1}\,(T\text{-}27) + t_{c2}\,(T\text{-}27)^2)$$

Where:

$t_{C1} = .0025$ and $t_{C2} = 0$, and T is the temperature in °C.

Most simulation programs allow for both a linear TCR (t_{c1}) and a quadratic TCR (t_{c2}). It is often observed that the temperature variation of R is not linear in T. In some cases (especially for heavily doped P type resistors below room temperature) the resistance falls with increasing temperature (i.e., the TCR is negative). The different simulation programs use different parameter names for t_{c1} and t_{c2}; the manual for the particular program used should be consulted for the right parameter name. The TCRs of the resistor types used in the CBP process are shown in Table 5.3.

Table 5.3: Resistor Temperature Coefficient

Type	t_{c1}	t_{c2}
Base (P–)	.00057	6.9E–6
Enhancement (P+)	.00076	2.05E–6

The R versus T curves for the different kinds of resistors are shown in Figure 5.4. The base (P–) resistor shows a minimum R below room temperature, and a negative TCR below that temperature. Accurate modeling of this requires the use of both t_{c1} and t_{c2}. The temperature coefficient is relatively low for both base and enhancement resistors compared. An area of design where resistor temperature modeling must be especially precise is in the design of bandgap references.

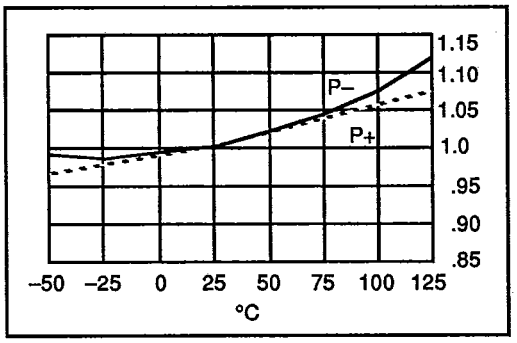


Figure 5.4: The Normalized Temperature Dependences of VJ900 Resistors

5.6 Resistor Tolerance and Matching

The tolerance on resistor absolute value should be taken as ±20% for base (P–) and enhancement (P+) resistors. This refers to the tolerance at a fixed temperature. The variation in R arises from differences in sheet resistance (doping level) and differences in resistor width (photoresist and etch variability). The tolerance on resistor ratio is much tighter than this. Data has been gathered on matched resistor sets connected as Wheatstone bridges, which has allowed the determination of matching accuracy with good precision. Our statistical model for resistor matching is a large group of identical resistors (same drawn L and W) placed nearby on the same chip. Assume that one measures the values of these resistors, getting R1, R2, . . . , RN. These results can then be subjected to a statistical analysis resulting in a mean and standard deviation. It is convenient to express the standard deviation as a percentage of the mean value. The measured results show that:

THE P+ AND P– RESISTORS HAVE A STANDARD DEVIATION OF ±.12% IN THEIR VALUES.

This only includes the mismatch due to doping and dimension variation. Mismatch arising from gradients of mechanical stress and temperature may add to the mismatch, but can be controlled to a substantial extent by design and applications practices. The ratio standard deviation will be 1.414 times as great as the figures given above. If the percentage standard deviation of R1 is X % and that of R2 is X %, then the percentage standard deviation of

$$\frac{R2}{R1} = X\sqrt{2\%}$$

(see Section 1.6)

The percentage standard deviation of R will be less for a resistor composed of several resistors in parallel or series. In this case the percentage standard deviation can be divided by the square root of the number N of series or parallel resistors to find the approximate percentage standard deviation for the combination (e.g., two .1% resistors in series or parallel will have a percent standard deviation of .1 / 1.414 = .0707%). The figures given above are for one standard deviation. The designer must decide how many standard deviations will be used as a worst case. The choice here is affected by the chip size. For example, a large chip may have 100 tightly ratioed resistors while a small chip may have only 2 or 3. With the larger set of ratioed resistors the probability of having one fall out in the tail of the distribution is greater, and all it takes is a single out-of-tolerance resistor to produce a nonfunctional chip in either case. The best way of determining whether the resis-

tors match satisfactorily is to find the expected statistical distribution of some overall chip parameter such as gain or offset on the basis of matching distributions of the resistors and transistors. Examples of how this is done are given in VTC's *Design Note DN-1*. The designer should keep in mind that resistor matching tolerances can also be affected by temperature gradients across the chip. While silicon is a very good thermal conductor, some temperature gradient nevertheless exists on a chip. The amount of temperature difference within the chip area depends on the overall power dissipation, the chip size, and the nature of the package. For typical DIPs dissipating .5 to 1 W, the temperature differences with a die are of the order of 1°C. This affects resistor matching through the temperature coefficient of R.

5.7 The Resistor Voltage Coefficient

Silicon monolithic resistors have a finite voltage coefficient. Because the resistor is actually made of a semiconductor material, the extent to which the isolating depletion region extends into the resistor doped region will vary somewhat depending on the resistor-body bias voltage. In other words, the resistor acts a little like a JFET (with the body acting as the gate). Because of the relatively high doping level of resistors, the effect is not a large one—but it must nevertheless be taken account of in some instances. Table 5.4 gives the effect of body-substrate bias resistor value.

Table 5.4: The Voltage Dependencies R(V)/R(O) of Resistors

Rev. Bias (V)	P–	P+
0.00	1.00000	1.00000
1.00	1.00603	1.00089
2.00	1.01127	1.00165
3.00	1.01610	1.00236
4.00	1.02065	1.00301
5.00	1.02501	1.00364

Thus, the voltage dependence amounts to about a 2.5% correction for 5 V back-bias for the P– resistors, and about .3% for the P+ resistors. A typical resistor will have different back-bias along its length, so a suitable procedure is to evaluate the percentage change in R at each end, and then average. If a more accurate model is desired, it is necessary to represent the resistor with a SPICE JFET model. The data given above can be represented as follows for modeling purposes:

$$\frac{1}{R_V} = \frac{1}{R_O}\left(1-\left(\frac{V+V_{bias}}{V_{po}}\right)^{\beta}\right)$$

Where:

R(V) is the resistance at reverse bias voltage V.
V_{bias} is the built-in voltage (about .75 V at 25°C).
V_{po} is the pinchoff voltage.
β is a dimensionless constant relating to the shape of the junction profile.

The pinchoff voltage V_{po} is the value of V for which 1/R goes to zero. Using this value, K can be found for any particular resistor. For further information on the theory of JFETs and how to use a JFET model for a resistor, see Grove, Chap. 8. The following table gives values of the parameters used in the equation above.

Table 5.5: Parameters for Resistor Voltage Dependence

Type	V_{po}	β	V_{bi}
P–	590	.75	.77
P+	7400	.75	.81

5.8 The Resistor Body Connection

The resistor body region is the surrounding silicon of opposite conductivity type. The resistor is isolated from this region by a PN junction. This PN junction must be kept reverse-biased at all times (including power-up and transient conditions) for proper circuit operation. Load diodes are used in simulations to provide parasitic capacitance modeling having the proper voltage dependence. The body region is one of the terminals of this load diode, so the designer must know how to connect the parasitic diode. The rules for this are as follows:

FOR P TYPE RESISTORS (ALL OF THE USUAL RESISTORS ARE P TYPE) THE BODY NODE IS V_{CC} (DEFINED AS THE MOST POSITIVE SUPPLY VOLTAGE).

In interpreting these rules GROUND is viewed as one of the supply voltages.

5.9 Resistor Statements in SPICE Simulations

As an example, consider the use of the 2013Ω P-resistor segment in a SPICE simulation of a resistor R33 between nodes 7 and 12. The SPICE elements used are as follows:

```
R33  7  12  2013  TC=.00057,6.9E-6
DAR33  7  NVCC  DRP  .062 OFF
DBR33  12  NVCC  DRP  .062 OFF
```

Here, NV_{CC} is node number of the most positive supply voltage. The parameters have been taken from Sections 5.3 and 5.5. Such a model represents a single segment of a segmented resistor. The complete model requires three such segments, and usually some extra nodes (see Part 8 for examples). We have labeled the parasitic load diodes the same as the resistor but prefixed them with DA- and DB-. This helps to keep the nature of the diode clear. If one of the resistor ends were at a DC potential, there would be no need to place a load diode at that point.

6. METALIZATION AND INTERCONNECTIONS

6.1 Basic Properties of Aluminum Interconnections

In designing the chip interconnections, there is concern with the parasitic resistance and capacitance of the metal lines. There are also concerns with the fundamental problem of electromigration, a physical phenomenon which provides a wear-out mechanism for interconnections. This section of the user's guide provides data on these matters. The designer should keep in mind that aluminum and its alloys have a substantial temperature coefficient of resistance, which should be taken as .0044/°C (.44%/°C). The TCRs of all metals are positive. An additional concern arises in vias. The effective resistance of a via should be taken as (worst-case) .5Ω, with a typical value of .1Ω. It is the practice to make all vias the minimum size and to use multiple vias for high-current connections. There is also a rule for maximum via current:

MINIMUM-SIZED VIAS SHOULD NOT CARRY MORE THAN 3 mA EACH.

Metal line width

Metal lines on integrated circuits are typically do not have the same finish width as drawn width. With the VJ900, a minimum first metal line is drawn 6u wide and its finish width is 4μ. 1μ on each side of a first metal line is removed during processing. This causes a first metal line to be 2μ narrower than drawn. A minimum second metal line is drawn 8μ wide and its finish width is 4μ. 2μ on each side of a second metal line is removed during processing. This causes a second metal line to be 4μ narrower than drawn. All calculations for metal capacitance, resistance, and electromigration concerns should be done with finish metal widths.

6.2 Power Bussing

Power bussing is an important matter in IC design. Aluminum is far from a perfect conductor, and substantial IR drops occur in the supply voltage lines. Careful calculations of the IR drops in the supply lines should be made. Some important aspects of supply bussing are these:

- Typical power busses have 10 to 30 mV variation in the supply voltage from the best- to worst-case locations within the chip. Reduction of this voltage difference to very low values requires careful design and the use of wide busses.
- The variation in supply voltage from one place to another gives rise to current hogging for common-emitter stages.
- It is common in linear and ECL circuits to have active current sinks/sources which drive much of the circuitry. These are often tied to a single common VCS bias line. In view of the usual variations in the supply voltage across a chip, one should always use emitter resistors in current sources, and should drop at least 200 to 400 mV across such resistors.
- Because of the large TCR of aluminum, IR drops in supply lines and DC bias lines should be estimated at a worst-case temperature.
- Since power busses can consume large amounts of chip area, this provides yet another reason for keeping power dissipation and operating currents to the lowest practical levels.

6.3 Capacitance and Resistance of Interconnection Lines

Table 6.1 (following page) contains metal resistances and capacitances. The numbers in the table for resistance are in Ω per square, where one square is an area of metal where the length is equal to its width. The capacitance numbers are given in pF per square μ. The capacitance values calculated using finish width metal lines are intended to be connected between the interconnection node and AC ground. The numbers shown are worst-case values and should be used when simulating a circuit for worst-case slow performance. Most interconnection lines run over the thick oxide between devices. The mesa oxide in the thin oxide present in active areas. The only mesa oxide areas open to routing on VJ900 circuits are over resistors and routing over resistors is not recommeded because of the MOS effects on the resistor value.

Table 6.1: Parasitic R and C for Interconnection Lines

Type of Line	C, pF/mm	R,Ω/mm
1st metal over field oxide with no 2nd metal on top	.29	20
1st metal over field oxide with 2nd metal on top	.77	20
1st metal over mesa oxide with no 2nd metal on top	3.13	20
1st metal over mesa oxide with 2nd metal on top	3.40	20
2nd metal over field oxide	.24	5.4
2nd metal over mesa oxide	.38	5.4
2nd metal over first metal	.53	5.4

Most interconnection lines run over the thick field oxide between devices. The mesa oxide is the thin oxide present in the active areas.

6.4 Electromigration Rules

Electromigration is a phenomenon in which the electron wind in a conductor transfers enough momentum to the metal atoms making up the crystal lattice that their diffusive jumps are affected. They jump more often downwind than upwind, resulting in a net material transport in the metal. Because the frequency of the diffusive jumps depends strongly on the temperature, the electromigration rate is also strongly (exponentially) temperature-dependent. The results of electromigration are cumulative (i.e., this is a wear-out mechanism for an IC). Under prolonged stress, metal piles up at the downwind end of a metal stripe (where the current fans out to a lower density) and is subtracted at the upwind end. The metal disappearing at the upwind end leaves voids, and these progressively increase in size until an open metal line results. Electromigration failure rates depend substantially on the current density in the conductor*. The following rules apply:

FIRST METAL: DO NOT EXCEED 3.5 MA FOR A MINIMUM-WIDTH FIRST METAL LINE.

SECOND METAL: DO NOT EXCEED 10 MA FOR A MINIMUM-WIDTH SECOND METAL LINE.

** A useful review of the basic features of electromigration and a bibliography of papers has been given by A. J. Learn, J. Electrochem. Soc., 123, 894, (1976).*

It should be kept in mind that these are upper limits. It is good practice to keep below them. It is unusual to see electromigration problems in power supply busses, since IR drop considerations are usually more restrictive than electromigration requirements. Where electromigration requirements really do come into play is for power transistors such as output drivers. The designer must call attention in the schematic drawings and/or other documentation to any interconnection line carrying more than 3.5 mA of current so that VTC can ensure that such lines are wide enough to meet the electromigration current density requirements.

6.5 DC Supply Lines

If logic and analog are combined on the same chip, it is often desirable to run separate supply lines (with separate package pins) for TTL push-pull outputs or ECL outputs in order to minimize noise coupling. Such I/O drivers can generate large current spikes, and the resulting noise can get into analog signal paths if care is not taken. Even if a separate supply pin is not used, it is still very desirable to use a separate supply line for the I/O drivers which only joins the supply metal near the supply pad.

6.6 Package Parasitics

A discussion of interconnections would not be complete without at least a brief description of the properties of the connections to the outside world (i.e., the package I/O leads). The detailed properties of these connections depend substantially on the nature of the package. The high-performance processes used for the VJ900 series master chips are able to produce bandwidths and rise times beyond those of ordinary packages. In some cases the bandwidth, stability, etc., of a chip may be largely limited by package parasitic elements. Therefore, the designer should choose the package and the pinout for a high-speed or wideband chip with great care. For best performance it is also important to choose an optimum pinout. Do not place outputs directly adjacent to low-level analog inputs. In some cases it may be desirable to leave guard pins (and/or board traces) between package I/O leads which need to be well isolated from each other. Use separate supply lines for digital and analog portions of a chip.

Pad capacitance

This is about .3 pF, which is low compared to the package capacitance in most cases.

Wirebound Inductance

This is about 2 nH for 1 mil bonding wire.

Wirebound resistance

The resistance of 1 mil aluminum wire is about 57 mΩs/mm. The resistance of gold wire is slightly less—about 49 mΩs/mm. A typical wirebond length is 2 to 4 mm.

Package pin inductance and capacitance

The values depend substantially on the package type. The following are representative examples:

Package Type	Inductance Per Pin	Capacitance Per Pin
DIP	10–20 nH	5 pF
SOIC	4–5 nH	2 pF
PLCC	5–6 nH	2 pF

Almost all ceramic packages are made with Kovar lead frames. This can be detrimental to achieving low inductance since Kovar and similar alloys are ferromagnetic. Many plastic packages use copper lead frames and, therefore, will have substantially lower lead inductances.

Package pin resistance

This is .05 to .25 for DIPs, depending on the pin. While the use of the corner pins for power supplies is conventional for TTL, if the supply current is substantial the pins near the center of the pin row are a better choice for a DIP.

7. PARASITIC PROBLEMS AND RELIABILITY FACTORS IN BIPOLAR IC DESIGN

This part of the user's guide brings together a number of issues relating to elements not shown on the circuit schematic diagram. Many of the hazards and effects described here are subtle and do not show up in normal IC testing, either on the bench or in automatic test equipment. They sometimes only show up as field failures when unusual conditions occur. Thus, attention paid to parasitic problems has a great deal to do with circuit quality and reliability, and with first-pass success.

7.1 Parasitic Elements

This section contains some non-ideal behaviors which do not usually show up in simulations, but are important for success of an overall design. In the previous text there has been much mention of parasitic R and C elements. Stress has been placed on making sure that these elements are included in simulations so that the simulated performance will match fairly closely with the measured performance. In general, the hazards of leaving out these passive parasitic elements do not extend beyond errors in the predicted frequency and time domain behavior. It can be quite the contrary for the active parasitics in an IC design. There are many lurking active parasitic transistors in an IC, and they do not appear in the schematic diagram. Experienced bipolar designers have a feel for avoiding parasitic problems, usually acquired from unhappy experiences. Here we hope to impart enough information to the less experienced designers so they too can avoid problems.

Some of the active parasitic elements are as follows:

- Every NPN transistor contains a lateral PNP. The emitter is the NPN base, the base is the NPN collector, and the collector is the substrate. The β of this transistor will be between 7 to 15 for the CBP process.
- P type (base and enhancement) resistors also can act as the emitters and collectors of parasitic lateral PNPs.
- If the collector-substrate junction of an NPN or a resistor tub gets forward-biased, an adjacent N tub can serve as a collector (i.e., there is a lateral NPN parasitic).
- A source of stray current which may cause trouble is photoinjection due to stray light from the normal room ambient. The typical values are μA for small geometries. Since most packages are opaque to light, this is not usually a problem in packaged devices, but can cause trouble in lab evaluations.
- Unique to the vertical PNP in the CBP process is a collecor-to-substrate parasitic PNP transistor. The emitter is the vertical PNP collector, the base is the N well (normally tied to V_{CC}), and the collector is the substrate. The down β for this transistor is about 40, while the up β is about .05.

It can be emphasized that parasitic transistors are everywhere. If minority carriers are injected into silicon, they will diffuse for up to 50μ to 100μ and can be collected by any junction within that radius, resulting in bipolar transistor action. The carriers diffuse particularly far in lightly-doped material such as an epi tub or the substrate. This might seem to be a lot of parasitics to deal with. Moreover, they do not appear on the schematic, and their properties are layout-dependent. It might appear to be a hopeless situation. Nevertheless, the basic rule for avoiding parasitic problems is quite simple:

NEVER ALLOW ANY PN JUNCTION TO BECOME FORWARD-BIASED EXCEPT A TRANSISTOR EMITTER-BASE JUNCTION.

If no junction is forward-biased, then parasitic transistor action cannot occur. Many standard practices have evolved to ensure that non-active junctions are never forward-biased, and if these are followed the designer should not have trouble. Many such practices have been described in previous text, but it will be repeated here in the context of parasitic suppression.

Is any amount of forward-bias safe? Will even 1 mV of forward-bias cause a problem? In fact, very little current flows in a forward-biased PN junction until the bias reaches 500 to 600mV (at room temperature). In other cases, the transistor β is what is important, and β generally falls to a very low value (<1) when V_{be} is even below 200 mV. Thus, a good rule of thumb might be that the forward-bias should be kept below 200 mV (at room temperature).

7.2 Biasing of the Substrate and Resistor Tubs

The biasing rule given above has the following consequences:

- THE SUBSTRATE IS CONNECTED TO THE MOST NEGATIVE SUPPLY VOLTAGE.
- N TYPE RESISTOR TUBS ARE CONNECTED TO THE MOST POSITIVE SUPPLY VOLTAGE.

Assuming that the signal voltages in the chip circuitry never go above or below the supply voltages, this ensures that all parasitic PN junctions are under zero or reverse-bias. Exceptions occur at inputs and outputs, where transients of various kinds are sometimes seen, resulting in voltage overshoot and undershoot. This often happens because of inductance in the I/O leads. Thus, parasitic problems should be guarded against with particular vigilance at I/O pads. The rules above can be extended to include connecting the substrate to a potential more negative than the most negative supply voltage. This is sometimes done in MOS circuits using an on-chip substrate bias generator. Such an arrangement ensures a finite reverse-bias at all times.

7.3 Biasing of N Wells

The purpose of the N well in the CBP process is to electrically isolate the collector of the vertical PNP from the P type substrate by placing an intervening N region between them. The requirement that no isolating junction become forward biased leads to the rule:

> THE N WELLS MUST BE TIED TO THE MOST POSITIVE SUPPLY VOLTAGE BY NUMEROUS CONNECTIONS TO V_{CC} METAL.

This rule is similar to that for N type resistor tubs, and in fact the resistor tubs and N wells can be merged into joint resistor/well tubs with shared V_{CC} connections.

7.4 Current and IR Drops in the Substrate and Tubs

The current flowing in the substrate and in resistor tubs would ordinarily be expected to be at most a μA or so—only the very small reverse leakage currents of back-biased junctions. As long as these currents are quite small, the IR drops in the substrate and in tubs can be expected to be small, and these regions can be viewed as equipotentials. However, if any substantial current flows in the substrate or in a tub, it may cause some parts of the junction surrounding the tub or the substrate to become forward-biased due to IR drops within the silicon. The biggest source of such DC currents is saturation of NPN and PNP transistors. If an NPN saturates, it contributes substrate current due to its intrinsic lateral PNP parasitic whose collector is the substrate. In most of these cases substrate current flows into the substrate, which is a P type region. This tends to forward-bias the substrate with respect to nearby N tubs. All tub to substrate junctions can become emitters if the substrate potential becomes sufficiently positive. Any nearby P region (e.g., a resistor) can then become a collector. The solution to this problem is contained in the rule:

> PLACE SUBSTRATE CONTACTS AT NUMEROUS LOCATIONS AROUND THE CHIP, WITH METAL CONNECTIONS TO THE MOST NEGATIVE SUPPLY VOLTAGE.

The net effect of this rule is to sharply limit the amount of IR drop in the substrate by keeping the nearest path to the supply metal short. Then the substrate current will be unable to build up enough forward-bias in the substrate to cause substantial current to flow in any parasitic PN junction. There is an analogous rule to ensure that excessive IR drops do not occur within resistor tubs:

> PLACE NUMEROUS CONNECTIONS (CONTACTS) TO V_{CC} METAL IN RESISTOR TUBS.

The VJ900 series master chips contain many V_{CC} connections to the resistor tubs and many substrate contacts placed around the chip. The wide transistor spacings used to allow the use of autorouting tools inherently reduce the substrate resistance.

7.5 Thyristor Latchup

When an NPN and a PNP transistor are connected so the collector of one is the base of the other and vice versa, the resulting structure is called a thyristor (or SCR, or 4-layer diode). A schematic for such a structure is shown in Figure 7.1 (following page).

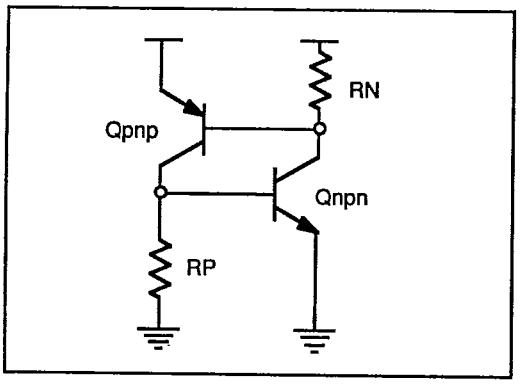


Figure 7.1: A Thyristor Structure

Here there are two transistors connected as inverters with collector resistors RP and RN. These resistors set the voltage gains of the inverters, and physically they arise from current paths through silicon. In this arrangement the two transistors form a feedback loop and turning one transistor ON will have the effect of turning the other ON in a regenerative fashion (i.e., the feedback is positive). In many practical cases one or both of the transistors in the thyristor is a parasitic transistor. It may operate in either the normal or inverted mode. Since the thyristor contains a feedback loop, the conditions for loop stability are of interest. Under what conditions will the thyristor be guaranteed not to turn ON? Analysis of this question gives the result:

> LATCHUP REQUIRES THAT THE PRODUCT OF THE NPN AND PNP β BE GREATER THAN 1.

In other words, if this condition is met an OFF thyristor is guaranteed to stay OFF. Of course, another approach is to observe that if neither of the transistor EB junctions ever becomes forward-biased the thyristor will always stay safely OFF. The (parasitic) collector resistors RP and RN also influence the behavior of the thyristor, giving rise to the additional stability condition:

> THE NET VOLTAGE GAIN AROUND THE LOOP MUST EXCEED 1 FOR THYRISTOR LATCHUP TO OCCUR.

The book by Sze (cited in the Section 1.7) contains an extensive treatment of thyristors. Both of the conditions above must be met simultaneously if thyristor latchup is to occur. The first condition (product of $\beta > 1$) is nearly always met for practical cases. The second condition (loop voltage gain >1) may or may not be met. The rules given above which are intended to minimize the resistance for substrate and tub currents also have the effect of reducing the voltage gain in parasitic thyristor loops. The voltage gain condition can be formulated quantitatively as follows. The voltage gains Ap and An of the PNP and NPN devices are:

$$A_p = I_{cp} \frac{RP}{V+}$$

$$A_n = I_{cn} \frac{RN}{V_t}$$

Where:

I_{cp}, I_{cn} are the collector currents of the PNP and NPN.
RP and RN are the collector resistances (see Figure 7.1).

$$V_t = \frac{kT}{q}$$

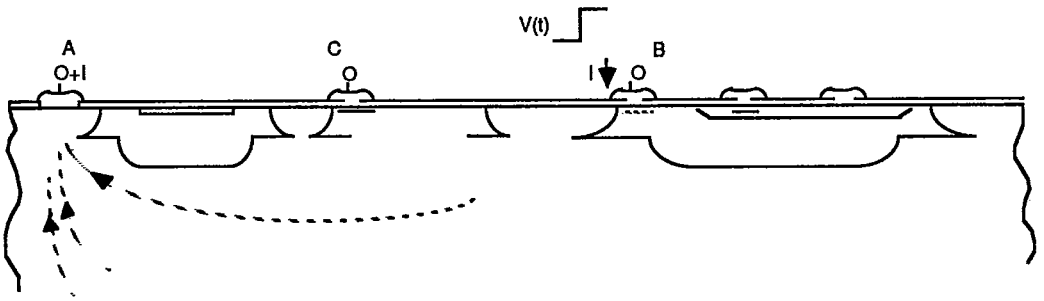
is the thermal voltage.

The voltage gain condition for stability is then:
$A_n A_p < 1$
which translates to:

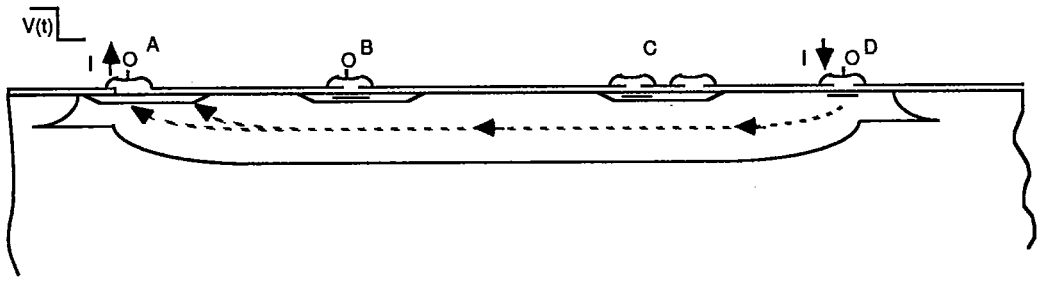
$$I_{cp}\, I_{cn} < \frac{V_t^2}{RN \cdot RP}$$

The right side of this inequality is more-or-less fixed by the design and layout, while the collector currents will be influenced by temperature, turn-on transients, current surges at I/O pins, etc. The conclusion reached from this equation is that for any thyristor there will be some critical current above which it will turn ON. We can now see some design strategies for defeating thyristors. Keeping RP and RN small raises the threshold current for thyristor latchup. The use of series resistors at I/O ports limits the maximum current which can flow and thus inhibits thyristor latchup. Temperature has a significant effect on thyristor latchup, and the problems are generally more troublesome at high temperatures*. To see how this can happen look again at the voltage gain condition for stability. The condition requires that the product of two collector currents be less than some design-

** This is one of the diagnostic symptoms of a thyristor—it leads to an electrical problem which is often only seen at elevated temperatures.*



a) Substrate current I arising from a positive-going transient pulse applied to a collector region. The effect is to give a local positive potential to the substrate, causing current to flow to a substrate contact A. If any N regions (collector tubes, epi resistors) in the vicinity of the pulsed collector tub are at a bias close to the most negative supply voltage (i.e., the potential of the substrate contact) they may see a forward-bias condition. The epi resistor C is an example of such a possibility. The effect of such forward bias depends on how the various doped regions are connected in the overall circuit.



b) Voltage drop in a resistor/emitter follower tub arising from a transient voltage on one of the resistors. The negative-going transient on resistor A may forward-bias the isolating junction of resistor B if it is close to the potential of the tub (i.e., to the most positive supply voltage). Resistor B could also be forward-biased if a large current flows in the emitter-follower C. The situation gets worse if the collector-region resistance between points C and D is high (for example if the buried layer were not continuous).

Figure 7.2: Illustration of Conditions Leading to Transient Forward Biasing of Parasitic PN Junctions in Bipolar ICs. Such Conditions Can Sometimes Lead to Thyristor Latchup.

related value. In many cases one transistor in the thyristor is a parasitic transistor which is nominally OFF and has a quite small collector current arising from junction leakage only. Thus, one of the collector currents is extremely small at room temperature and the condition for stability is easily met (i.e., the threshold current for the other transistor is very large). As temperature rises, however, the junction leakage increases by many orders of magnitude (it doubles about every 10°C) so the threshold current for instability falls steadily and may be dangerously low at high temperatures.

We should stress the latching nature of thyristor behavior here—once a thyristor has been turned ON, there is usually no way to turn it OFF other than powering down the chip. (This, incidentally, is one way of diagnosing thyristors in finished chips.) In fact, thyristor turn-ON may be initiated by transient conditions in the chip—peculiar things happening during power-up or due to transient surges at I/O pins. Once initiated,

the thyristor action persists and destroys chip functionality. In the most extreme cases, the thyristor ON current may be so high (if the path resistance is low) that currents of several amperes flow in the supply pins and the chip destroys itself. (This was common in early CMOS chips, which have a similar hazard.) Thyristors can often be detected by looking at the I-V characteristics of the supply or I/O pins with a curve tracer. If a thyristor is present it often shows up as hysteresis in the I-V trace, because the turn-ON and turn-OFF points of the thyristor are different.

Transient substrate or tub currents can initiate thyristor action just as DC currents can. An example could be the sudden switching of a large NPN collector from LOW to HIGH. This causes a capacitor-charging current to flow in the substrate which tends to make the P substrate region under the transistor more positive in potential. The resulting forward-bias of the substrate can cause parasitic problems in nearby devices. The general remedy of keeping resistive paths short in the substrate also helps here. Some situations leading to transient forward-bias of parasitic PN junctions are shown in Figure 7.2. In most cases when a thyristor turns ON, both of the transistors saturate. This is why thyristors can carry very high currents and are so useful as power devices. But one consequence of this is that very large injected minority carrier currents flow in the region of the thyristor. These can be collected by nearby PN junctions causing other malfunctions.

7.6 SPICE Modeling of the Parasitic PNP

It has been noted several times in this user's guide that every NPN has a parasitic PNP whose collector is the substrate. Its emitter is the normal base region, and its base is the normal collector region. It is sometimes useful to be able to model this parasitic transistor in SPICE. We have made some detailed measurements which allow this to be done. The SPICE model for the parasitic PNP of a T3NW NPN in the CBP process is:

```
.MODEL T3NWP PNP (IS=1.5E-17 BF=15 BR=2
+IKF=1.9E-4 RE=60
+CJE=6.4E-14 MJE=.39 VJE=.81 CJC=2.0E-13
+MJC=.42 VJC=.63
+RC=200 NE=1.5 NC=1.5 ISE=1.5E-17
+ISC=1.5E-17
+TF=1E-7 TR=1E-6 VAF=80 VAR=80
+RC=<value> )
```

The average latching voltage LV_{ceo} for these parasitic transistors was found to be about 12 V for CBP based on a limited sample of material. If a different NPN transistor model is used (other than T3NW) then a different area factor for this model should be used. The area should be increased in the ratio of CJC for the NPN models of the two transistors. The same basic model can also be used for the parasitic PNP associated with a P type resistor. Here one would use an area factor:

$$\text{AREA} = \frac{\text{2(C/2 VALUE IN FARADS FOR THE RESISTOR)}}{\text{CJE FROM THE ABOVE MODEL}}$$

The BF and BR values given above would continue to be about right for a resistor parasitic PNP if it is immediately adjacent (minimum spacing) to the edge of the resistor tub. For a resistor out in the middle of a tub the BF and BR values would be substantially less (and parasitic problems less likely).

7.7 The Use of Schottky Diodes to Suppress Thyristors

It was noted previously in the discussion of Schottky diodes that such a diode is a non-injecting diode. It also turns on at a lower forward voltage than a PN junction. Thus, by paralleling a PN junction with a Schotty diode, it can be made non-injecting. It can then never be the emitter of a parasitic bipolar transistor. This solution to parasitic problems has been used in many cases and found quite effective. The designer who wants to see the effectiveness of this can look at a typical Schottky NPN on a curve tracer and look at the inverse β. In most cases this is so low, it is unmeasurable (<.001). Thus, the use of suitable Schottky diodes can often cause the product-of-β condition for thyristor latchup to fail. When a designer suspects a parasitic problem, it is good insurance to use a Schottky-clamped NPN or PNP transistor. An example is the use of Schottky-clamped transistors for any devices which can be expected to saturate under normal or power-up conditions.

7.8 Inductive Loads

RC circuits will not usually have signal voltages which go above or below the supply voltages. When inductance is present, however, such surges (overshoot and undershoot) can occur. Thus, inductive loads (or inputs) present a special case. The I/O circuitry should be designed and placed with special care when the load to be driven is a relay, a motor, an inductive read/write head, or even just a fairly long board trace. Careful consideration should be given to the rules and principles provided above for avoiding thyristor latchup or other parasitic problems which can occur when the overshoot forward-biases parasitic PN junctions. When inductive loads are to be

driven it is quite common to use off-chip discrete elements (rectifiers, Zener diodes) to control the destructive voltage kick as the current through the inductance is switched. An interesting description of these techniques and the associated chip parasitic problems can be found in an article by P. Emerald, *Electronic Design*, March 14 (1985), p. 195.

7.9 Off-Chip Capacitors—Power-Up Current Surges

Since the available on-chip (junction) capacitors are low in value and nonlinear, it is often necessary to use off-chip capacitors. These may have quite large values. In designing the circuitry that connects to such capacitors the designer should keep in mind that large amounts of current may be needed to bring the capacitor voltage to its quiescent point when the power is turned on, even if the capacitor current is quite low in normal circuit operation. In other words, one should design for the power-up transient as well as for normal operation. Consider the case of a high-value capacitor with its chargeup current supplied by an NPN emitter follower and the other terminal connected to V_{EE}. The base of the emitter follower is held at some voltage by a fast bias or driver circuit. If V_{CC} rises rapidly, the capacitor looks momentarily like a short-circuit to the emitter follower (until it is charged up to its normal DC value). The short-circuit current of an emitter follower can reach tens or hundreds of mA, and this may be enough to do permanent damage to a transistor, especially if it is a minimum-sized device.

Another possibility is that the surge current can trigger a parasitic thyristor (the diagnostic test for this is to see if the problem goes away when the chip is powered up very slowly). The circuit should be designed so the initial charging current for large capacitors is limited. The simplest way to do this is to use a high-impedance circuit to charge the capacitor. A simple example of this is the inclusion of a series resistor in the charging path with a resistance low enough that it does not affect normal circuit operation, but high enough to limit power-up current surges to reasonable values. As a rule of thumb, transient power-up currents of up to 10 times the rated maximum collector current can be tolerated without permanent damage.

7.10 Electrostatic Discharge; Input Protection

As noted above, I/O pins tend to be special points in an IC. They often get unusual voltage or current transients due to events happening outside the chip. One common cause of such unusual transients is electrostatic discharge. This often happens during handling of the packaged IC. The fingers or tools used to handle the IC may build up to a high electrostatic charge (tens of kV) due to rubber shoes on carpets, etc.

A related problem is the use of plastic shipping and storage containers for ICs, which may build up a static charge high enough to do damage. (To prevent this, today most of these are made of electrically conductive plastics). When a package pin comes in contact with an electrostatically-charged object, the entire charge stored on its stray capacitance (often tens or hundreds of pF) may discharge through the chip in a very short time. This usually results in highly localized energy dissipation in those circuit elements connected most directly to the I/O pin, and can cause sudden local heating. This heating can cause a localized spot of the chip to exceed the eutectic point of the Al-Si system (577°C), and this can lead to shorted junctions and other kinds of damage.

For analog ICs, such discharges may alter the parameters enough to cause circuit malfunction without actually causing the chip to be nonfunctional. Very high electrostatic voltages on oxide films can lead to irreversible dielectric breakdown (rupture) in an IC structure. This is especially prevalent with MOSFET devices, but can be a problem with bipolar devices as well (especially for high-density oxide-isolated structures, which often have rather thin oxide films).

Electrostatic discharge can also lead to thyristor latchup as described above (Section 7.5). In addition to the irreversible kinds of damage mentioned above, it is also possible to have reversible damage. The most common form of this arises from injection of hot electrons into an oxide when a junction is in reverse (avalanche) breakdown. The hot electrons create space charge in the oxide which can cause low breakdown voltages and unexpected leakage paths resulting in a nonfunctional circuit. The hot electrons will leak out of the oxide in a matter of minutes or hours (especially fast if the device is placed in an oven) and proper device functioning will be restored. When electrostatic discharge is observed to cause device damage, it is always important to determine whether it is reversible or irreversible, since the corrective action is quite different in the two cases.

Sometimes it is possible to solve ESD problems outside the chip; for example, by putting Zener clamp diodes on signal and power lines. Early ICs showed few ESD problems because the dielectric layers were thick and the junction areas were large. The discharge energy was spread over a large physical volume, and excessive localized temperatures did not develop. The further evolution of IC technology has

brought shallower junctions and smaller features, so that the ESD energy is much more concentrated and more likely to do permanent damage. Today, virtually all IC technologies require some attention to ESD problems. The usual remedy for ESD problems is to redesign the input(s). This can be slow and painful, so it is desirable to try to design out ESD problems from the outset.

- Outputs are generally not a problem since they are usually connected to physically large driver devices which can sustain large surge currents without damage.
- Zener diodes (reverse-biased EB diodes) are also susceptible to ESD damage, and should not be connected directly at I/O pins if precision and stability of their properties is important.
- In Schottky TTL, it is customary to place a large Schottky diode at inputs, connected between the input and GROUND such that if the input goes below GROUND it turns ON. This diode is physically quite large and can pass large ESD current spikes without damage.
- In ECL circuits, one often places a fairly large diode-connected transistor between the input pin and V_{CC}, such that if the pin goes above V_{CC} the diode becomes forward-biased. Since the usual diode-connected transistor has a reverse breakdown voltage of about 5 V, this also protects against negative voltage transients. A resistor is sometimes placed in series with the diode.
- In some cases it is desirable to place a resistor in series with the input to limit the current.
- When dielectric capacitors are used they can undergo irreversible electrical damage due to electrostatic discharge. They should not be connected to I/O pins if this can be avoided, and if it is unavoidable then the I/O pin should have an ESD protection device.

It can be seen that in general the solutions to ESD problems involve 1) using diodes (and Zeners) to clip voltage spikes, and 2) placing large devices at inputs which can pass ESD currents without damage.

Input protection diodes are usually connected from the input to one or the other (or even both) of the supply voltages, in such a manner that they are normally reverse-biased (see Figure 7.3). TTL design conventions inherently call for such a diode to GROUND. If $V_{CC} > 5$ V, care must be taken that the reverse breakdown voltage of the diode is not exceeded in normal chip operation. Such diodes are usually physically large so they can pass current spikes without damage. The capacitance of such a diode is usually driven satisfactorily at an input since it is small compared to typical (card-level) wiring capacitances.

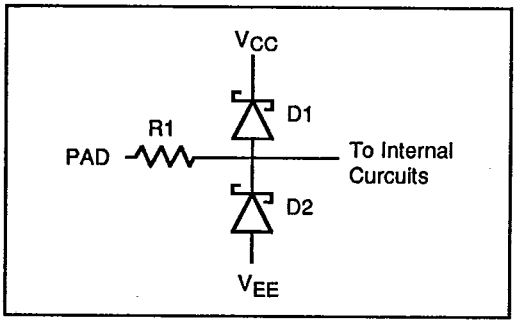


Figure 7.3: Input Protection Elements

7.11 Hazards from Multiple Supply Voltages

We have noted above that each P type resistor has a diode connected to V_{CC}, where V_{CC} is the most positive supply voltage (Section 5.8). The N side of this parasitic diode is connected to V_{CC} so that it is always reverse-biased. A somewhat different situation arises when we have two supply voltages in addition to GROUND. Such situations can occur, for example, with supplies of +5, 0, -5 V, and +12, +5, 0 V. In this case one must choose to connect the resistor tubs to one supply voltage or the other. This can result in a situation where the resistor parasitic diodes can become forward-biased if the supply voltages are turned ON in the wrong sequence. The total area of the resistor parasitic diodes in a chip can be quite large, and if they are forward-biased the current which flows can be very large—in amperes! Such large currents will usually destroy the chip unless the power supply current is limited in some way. To see how the parasitic diodes can become forward-biased, see Figure 7.4 showing a portion of a circuit operating with +12 and +5 V supply voltages. We show the resistor parasitic diodes DP1 and DP2, with all of the tubs connected to the +12 V supply line. Now consider what can happen if the +5 V supply is energized while the +12 V supply is at GROUND. Parasitic diode DP2 is heavily forward-biased and a very large current flows.

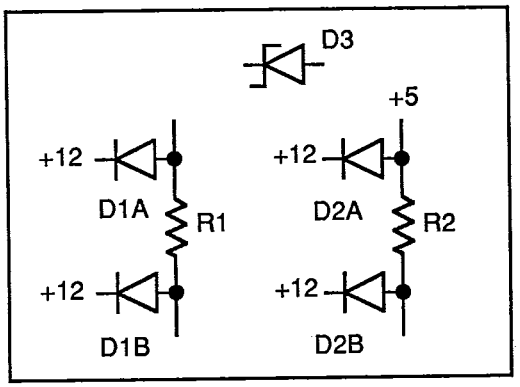


Figure 7.4: Resistors in a Chip Operating from +12 and +5V Power Supplies

If +12 V is connected to a high-impedance source (for example, a power supply which is OFF may have a high output impedance), the result will be to pull the +12 V supply line to (5-Vfwd) V where Vfwd is the forward drop of the parasitic diodes (about .6 to .7 V). In this case it may happen that no destructive current surge occurs, since the heavy current only flows for a very short time. On the other hand, if the +12 V line is solidly grounded (or has a lot of capacitance connected off-chip), severe damage is almost certain to occur. Even if the +12 V supply is rapidly pulled to (5 -Vfwd), it is still possible to get into trouble by momentary parasitic transistor action while the resistor-body junction is briefly forward-biased if it acts as the emitter of a parasitic PNP. If other elements are present which can lead to thyristor latchup (Section 7.5), then normal circuit operation may be prevented. In some cases it may thus happen that a circuit works normally if the power supplies are turned ON in a certain sequence, while malfunction is seen when the supplies are turned ON in a different sequence. It is evident from a study of Figure 7.4 that there would be no supply sequencing problem if all of the 5 V resistors were in 5 V tubs and all of the 12 V resistors in 12 V tubs. It is often possible to rigorously separate the resistors into 5 V and 12 V categories (or other similar categories when other supply voltages are used), and when this can be done the sequencing problem can be solved by suitable layout of the resistor tubs.

The VJ900 series master chips have their resistors in several isolated tubs so this kind of separation can be done. Another way of solving the sequencing problem is shown in Figure 7.4 —by using the Schottky diode D3. This is a Schottky rectifier device external to the chip (it could also be a germanium diode). In effect, this diode is in parallel with all of the parasitic diodes of the resistors. Since it is a Schottky device, it will conduct at a lower voltage than the resistor parasitic diodes, and hence will bypass all of the current, preventing any of the resistors from acting as a parasitic emitter of a PNP. By this means thyristor latchup can be defeated by an extra component added at the card level. To prevent potential power-up sequencing problems, the entire VJ900 circuit should be simulated under different power-up sequence conditions. It is important that the parasitic diodes which represent resistor parasitic capacitances be included (with the different tubs connected to different DC supplies if this is done in the real chip) when these simulations are carried out.

7.12 Temperature Gradients Across a Chip; Warmup

While this is not an electrical parasitic, such temperature gradients do exist and can affect circuit behavior. Some data for a particular case can be found in Hamilton and Howard, p. 298 (see the references in Section 1.7). Some rough guides for thermal parasitics follow:

- The magnitude of the temperature difference within a chip is of the order of 1°C.
- The size of the temperature difference depends in detail on the particular package, the die size, and the total power dissipation.
- The corners of a chip will be especially cold with respect to the rest of the chip, so temperature-sensitive circuits should not be located there.
- It has been reported that thermal feedback can cause circuit instabilities in some cases. For instance, it is stated that if op amps are designed with DC open-loop gains above about 200,000, there can be instabilies at low frequencies due to heat dissipation slowly altering the circuit parameters. Such instabilities are only to be expected at very low frequencies since the thermal response of the chip is quite slow. Thermal feedback can manifest itself as a low-frequency hysteresis in the transfer characteristic of an amplifier.
- A chip will have a significant warmup transient when it is turned ON, and during this period the temperature gradients can be expected to be larger than in the steady state. For ceramic DIPs, the warmup transient will have a time constant of 1 to 5 min.

7.13 Mechanical Stress; Piezoresistance

An IC chip always has a certain amount of mechanical stress in it. Much of this stress appears during package assembly due to the different thermal expansion coefficients of the die and the package material. Thus, the stress can vary from one packaged unit to another because of the random variation in the die attach process. This stress causes small changes in the properties of the transistors, diodes, resistors, etc. These stress-induced changes are not ordinarily a problem, but if high precision is to be achieved such second order effects can be significant. In some cases they set the upper limit to precision—for example, the precision in the output voltage of a bandgap reference source.

Other areas where it can be significant are in the offset voltages of differential amplifiers and in the precision of R-2R resistor ladder networks for DACs and ADCs. The stress-induced change in resistance is called piezoresistance, and has been studied in detail for silicon. The effect is used to advantage in certain kinds of integrated pressure transducer and accelerometer devices which incorporate a thin silicon plate or slab with resistors diffused into it. In order to minimize stress effects in resistors it is desirable that they be close together physically. The most effective way of minimizing stress effects for matched transistors is to use centroid-weighted quads (see Gray and Meyer, cited in references, Section 1.7).

8. SPICE LISTINGS

8.1 Introduction

Software has been developed by VTC for checking chip interconnection artwork from SPICE netlists (deck). In order for this to work properly certain conventions must be followed by the user. This section shows the user the proper format to use when encoding a SPICE file. The next several pages contain VTC component symbols, lower-level schematics, and the required code for using the component in SPICE. Following the descriptions of each device a SPICE example will be explained in detail.

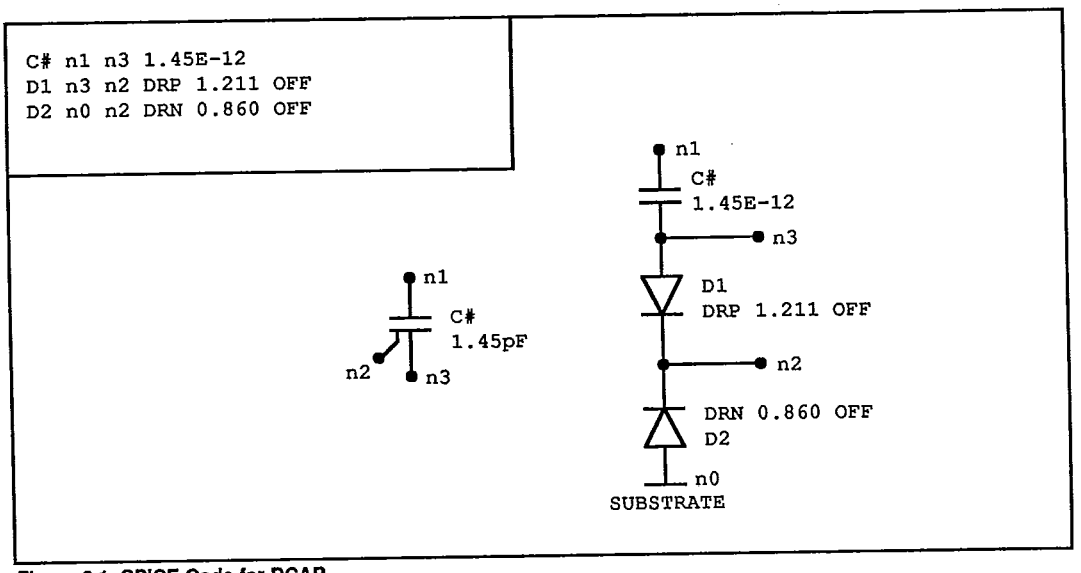


Figure 8.1: SPICE Code for DCAP

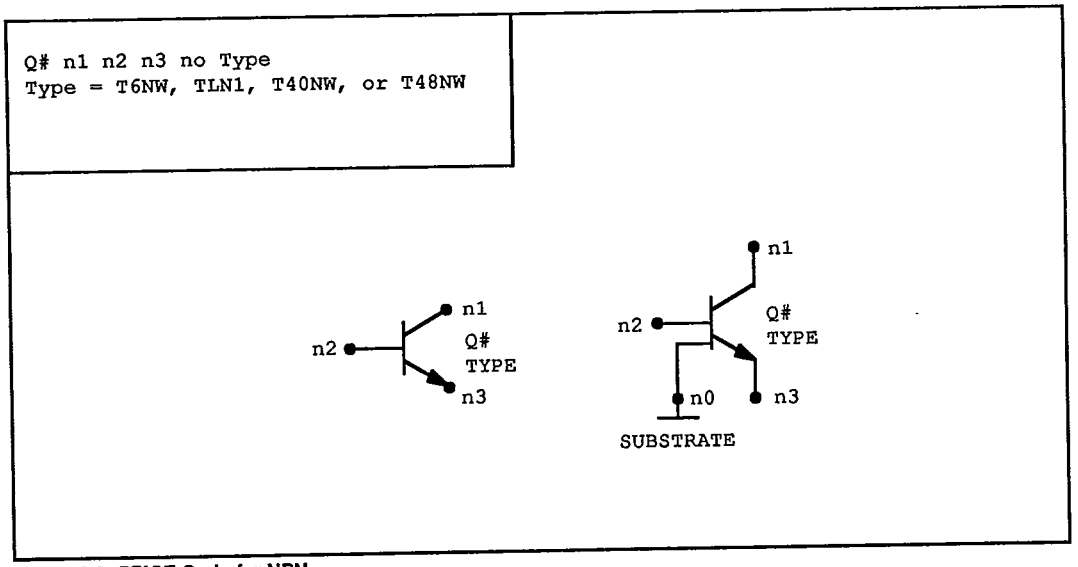


Figure 8.2: SPICE Code for NPN

```
Q# n3 n2 n1 n4 Type
Type = TVPA8, TVPA35, or TVPA40
```

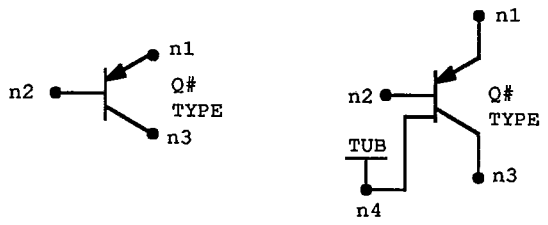


Figure 8.3: SPICE Code for PNP

```
R# n1 n2 5090 TC=5.7E-4,6.9E-6
D1 n1 n3 DRP 0.030 OFF
D2 n2 n3 DRP 0.030 OFF
```

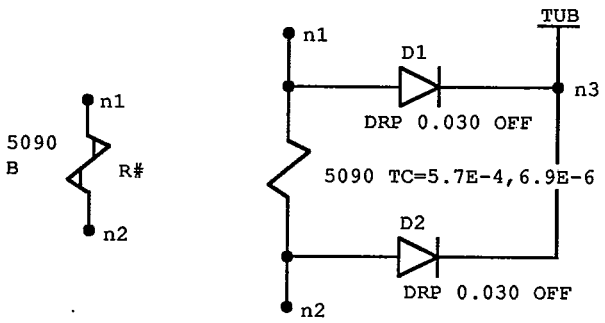
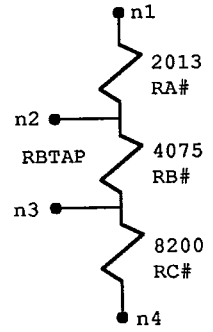


Figure 8.4: SPICE Code for RB5090

```
RA# n1 n2 2013 TC=570E-6,6.9E-6
RB# n2 n3 4075 TC=570E-6,6.9E-6
RC# n3 n4 8200 TC=570E-6,6.9E-6
D1 n1 n5 DRP 0.062 OFF
D2 n2 n5 DRP 0.16 OFF
D3 n3 n5 DRP 0.269 OFF
D4 n4 n5 DRP 0.171 OFF
```



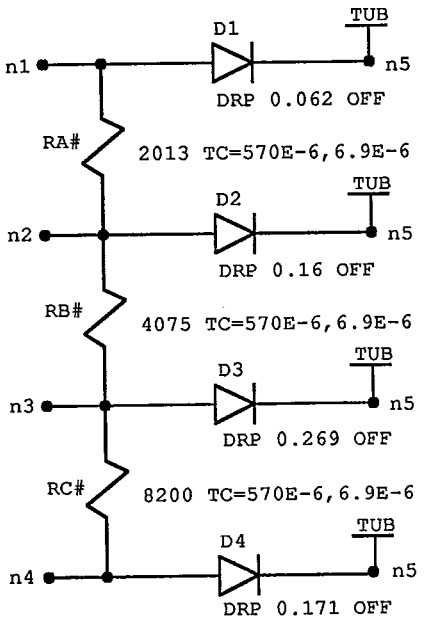
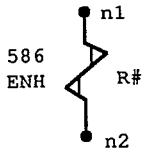


Figure 8.5: SPICE Code for RBTAP

```
R# n1 n2 586 TC=7.6E-4,2.05E-6
D1 n1 n3 DRP 0.022 OFF
D2 n2 n3 DRP 0.022 OFF
```



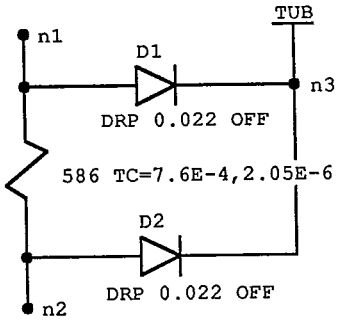
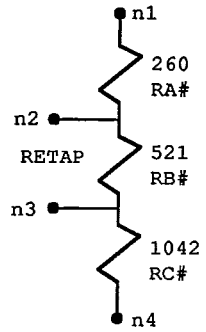


Figure 8.6: SPICE Code for RE586

```
RA# n1 n2 260 TC=760E-6,2.05E-6
RB# n2 n3 521 TC=760E-6,2.05E-6
RC# n3 n4 1042 TC=760E-6,2.05E-6
D1 n1 n5 DRP 0.049 OFF
D2 n2 n5 DRP 0.125 OFF
D3 n3 n5 DRP 0.208 OFF
D4 n4 n5 DRP 0.132 OFF
```



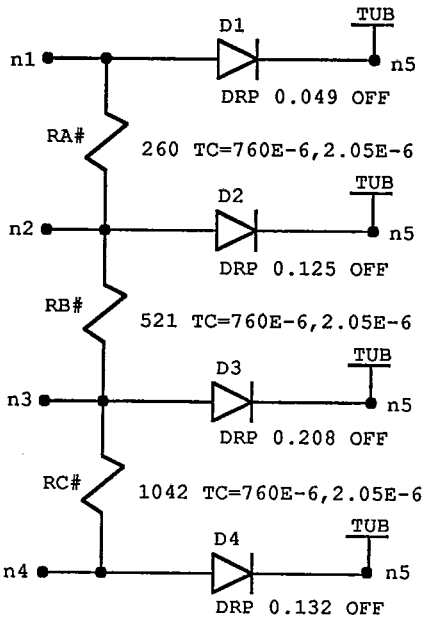
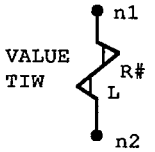
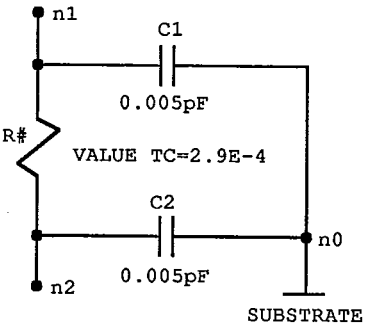


Figure 8.7: SPICE Code for RETAP

```
R# n1 n2 VALUE TC=2.9E-4
C1 n1 n0 DRP 0.005E-12
C2 n2 n0 DRP 0.005E-12
```





See Table 8.1 for Value and Length information.

Figure 8.8: SPICE Code for RTIW

T-42-21

```
DS1# n1 n3 SCH3 71
DGR1# n1 n3 DRP 0.053 OFF
DSUB1# n0 n3 DRN 0.246 OFF
RGR1# n3 n2 103 TC=0.004
```

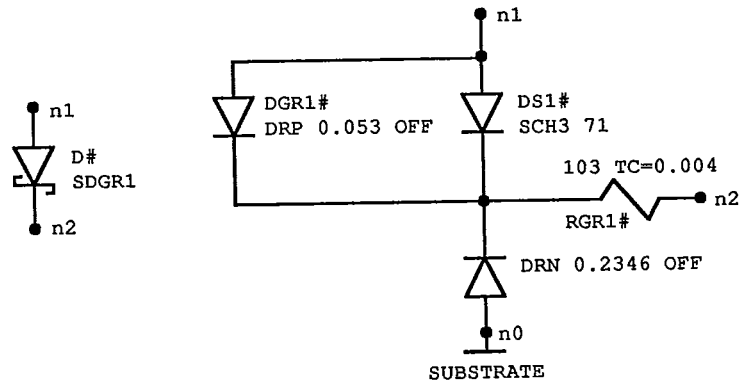


Figure 8.9: SPICE Code for SDGR1

```
DS40# n1 n3 SCH3 1682
DGR40# n1 n3 DRP 0.080 OFF
DSUB# n0 n3 DRN 1.15 OFF
RGR40# n3 n2 19.3 TC=0.004
```

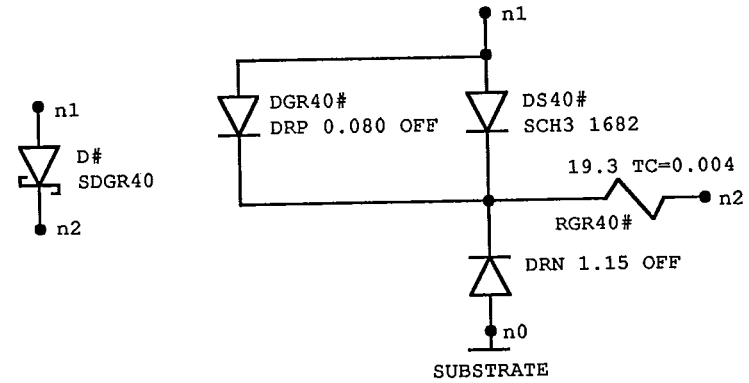


Figure 8.10: SPICE Code for SDGR40

```
D# n2 n1 T6NWAC
DS1 n0 n2 DRN 0.263 OFF
```

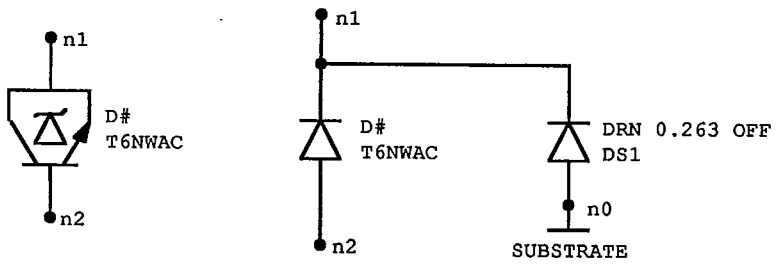
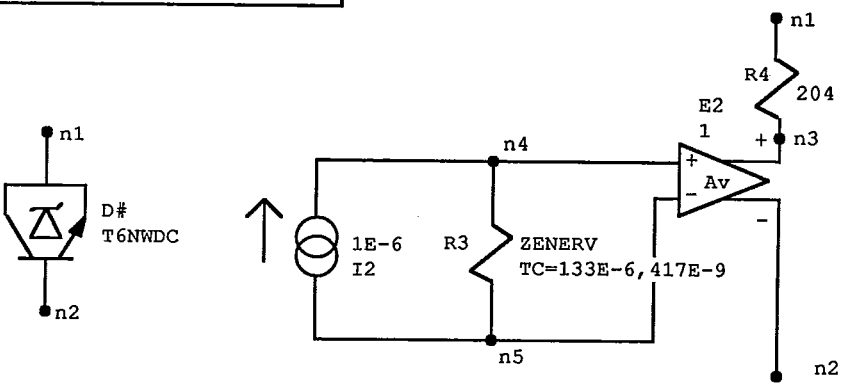


Figure 8.11: SPICE Code for AC ZENER

```
I2 n5 n4 1E-6
R3 n4 n5 ZenerV TC=133E-6,417E-9*
E2 n3 n2 n4 n5 1
R4 n1 n2 204
```



**ZenerV sets the Zener Voltage.*
Aener = 4.7E-6, or 5.1E-6

Figure 8.12: SPICE Code for DC ZENER

Table 8.1: TI/W Resistors

Resistor Length (μ)	Resistor Value (Ω)	Resistor Length (μ)	Resistor Value (Ω)	Resistor Length (μ)	Resistor Value (Ω)
8.0	42	23.5	104	38.5	164
8.5	44	24.0	106	39.0	166
9.0	46	24.5	108	39.5	168
9.5	48	25.0	110	40.0	170
10.0	50	25.5	112	40.5	172
10.5	52	26.0	114	41.0	174
11.0	54	26.5	116	41.5	176
11.5	56	27.0	118	42.0	178
12.0	58	27.5	120	42.5	180
12.5	60	28.0	122	43.0	182
13.0	62	28.5	124	43.5	184
13.5	64	29.0	126	44.0	186
14.0	66	29.5	128	44.5	188
14.5	68	30.0	130	45.0	190
15.0	70	30.5	132	45.5	192
15.5	72	31.0	134	46.0	194
16.0	74	31.5	136	46.5	196
16.5	76	32.0	138	47.0	198
17.0	78	32.5	140	47.5	200
17.5	80	33.0	142	48.0	202
18.0	82	33.5	144		
18.5	84	34.0	146		
19.5	88	34.5	148		
20.0	90	35.0	150		
20.5	92	35.5	152		
21.0	94	36.0	154		
21.5	96	36.5	156		
22.0	98	37.0	158		
22.5	100	37.5	160		
23.0	102	38.0	162		

8.2 The Use of Subcircuits in SPICE

Currently, the use of the SPICE .SUBCKT statement is not valid for input to the VTC CAD software. All SPICE files must be flat (i.e., not nested). It is intended that future versions allow subcircuits. This is not an especially important restriction for small circuits which can be simulated from a single SPICE source listing without excessive run times. For the larger VJ900 series chips, a SPICE input file which includes the whole of the circuitry would have an impractically long run time. There is no real problem with using a SPICE input file for sections of circuitry which were simulated separately. The only important limitations are that: 1) The same node number cannot be re-used for distinct nodes in different blocks; and 2) Interblock signals must have the same node number in different simulation files.

As an example of how a large circuit might be represented, consider the following set of node assignments for three separately simulated large blocks:

NODES 0-99INTERBLOCK SIGNALS, POWER, GROUND
NODES 100-199 SEPARATELY SIMULATED BLOCK 1
NODES 200-299 SEPARATELY SIMULATED BLOCK 2
NODES 300-399 SEPARATELY SIMULATED BLOCK 3

These separate blocks of SPICE input code would have to be combined in the final file used as CAD input.

8.3 A SPICE Example

An example of an analog circuit which might be simulated with SPICE is shown in Figures 8.5 and 8.6 (facing page). Figure 8.5 shows an ordinary schematic of the circuit that would be drawn by a typical designer. By comparing this drawing with the SPICE listing given below it can be seen that a number of additional components and nodes have been added to represent the real circuit. Figure 8.6 shows the complete circuit generated with a Mentor workstation at VTC, including all of the components except the parasitic diodes of the resistors (which are actually created in the SPICE file, but not shown in the element symbols). This circuit realizes a differential integrator function, that is the output voltage (node 9) represents the integral of the difference between two input voltages (nodes 6 and 7). The SPICE source code for this circuit is given below, followed by a detailed line-by-line explanation of the function of the various statements.

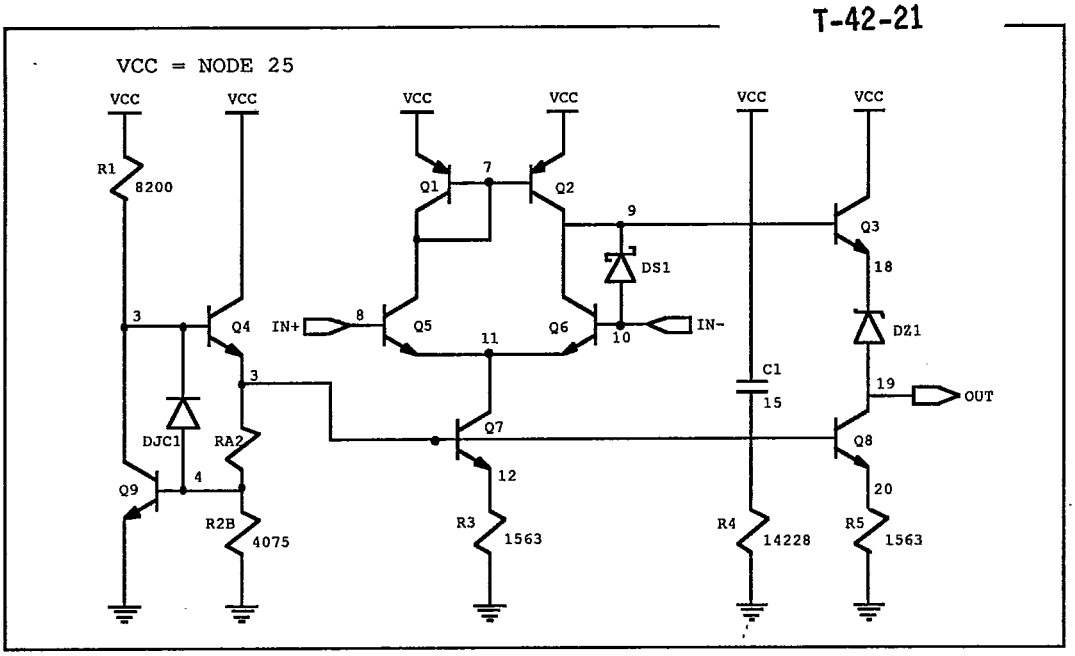


Figure 8.13: SPICE Circuit Example Using the Usual Schematic Notation

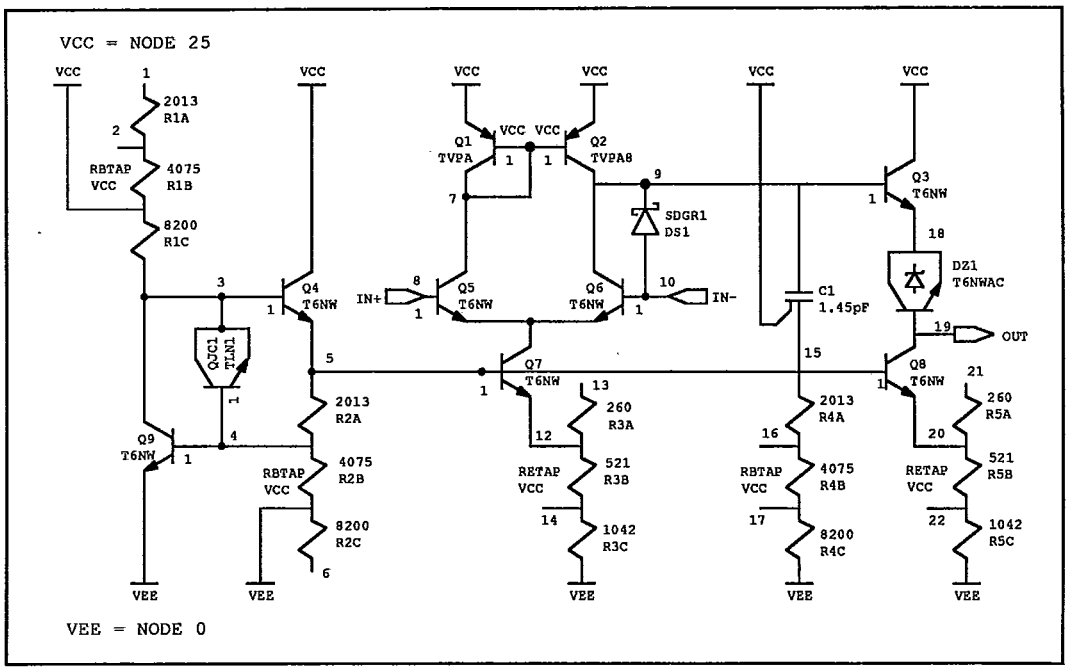


Figure 8.14: SPICE Circuit Example Using VTC VJ900 Device Symbols

8.4 SPICE Netlist (for Figures 8.13 and 8.14)

```
*SPICE INTEGRATOR EXAMPLE - VERSION D - 3-15-86
*BIAS GENERATOR
Q4 25 3 5 0 T6NW
Q9 3 4 0 0 T6NW
QJC1 3 4 3 0 TLN1
R1A 1 2 2013 TC=5.7E-4,6.9E-6
R1B 2 25 4075 TC=5.7E-4,6.9E-6
R1C 25 3 8200 TC=5.7E-4,6.9E-6
DPR1A 1 24 DRP 0.062 OFF
DPR1B 2 24 DRP 0.16 OFF
DPR1C 24 24 DRP 0.269 OFF
DPR1D 3 24 DRP 0.171 OFF
R2A 5 5 2013 TC=5.7E-4,6.9E-6
R2B 4 0 4075 TC=5.7E-4,6.9E-6
R2C 0 6 8200 TC=5.7E-4,6.9E-6
DPR2A 5 24 DRP 0.062 OFF
DPR2B 4 24 DRP 0.16 OFF
DPR2C 0 24 DRP 0.269 OFF
DPR2D 6 24 DRP 0.171 OFF
*INTEGRATOR
Q1 7 7 25 25 TVPA8
Q2 9 7 25 25 TVPA8
Q3 25 9 18 0 T6NW
Q5 7 8 11 0 T6NW
Q6 9 10 11 0 T6NW
Q7 11 5 12 0 T6NW
Q8 19 5 20 0 T6NW
*SCHOTTKY DIODE
DS1 10 23 SCH3 71
DS1GR 10 23 DRP 0.053 OFF
DS1SB 0 32 DRN 0.246 OFF
RDS1 23 9 103 TC=0.004
*AC ZENER DIODE
DZ1 19 18  T6NWAC
DZ1SB 18 0 DRN 0.263 OFF
*DIELECTRIC CAPACITOR
C1 9 15 1.45E-12
DC1T 15 25 DRP 1.211 OFF
DC1SB 0 25 DRN 0.860 OFF
*RESISTORS
R3A 13 12 260 TC=7.6E-4,2.05E-6
R3A 12 14 521 TC=7.6E-4,2.05E-6
R3A 14 0 1042 TC=7.6E-4,2.05E-6
DPR3A 13 25 DRP 0.049 OFF
DPR3B 12 25 DRP 0.125 OFF
DPR3C 14 25 DRP 0.208 OFF
DPR3D 0 25  DRP 0.132 OFF
R4A 15 16 2013 TC=5.7E-4,6.9E-6
```

```
R4B 16 17 4075 TC=5.7E-4,6.9E-6
R4C 17  0 8200 TC=5.7E-4,6.9E-6
DPR4A 15 24 DRP 0.062 OFF
DPR4B 16 24 DRP 0.16  OFF
DPR4C 17 24 DRP 0.269 OFF
DPR4D  0 24 DRP 0.171 OFF
R5A 21 20 260 TC=7.6E-4,2.05E-6
R5A 20 22 521 TC=7.6E-4,2.05E-6
R5A 22 0 1042 TC=7.6E-4,2.05E-6
DPR5A 21 25 DRP 0.049 OFF
DPR5B 20 25 DRP 0.125 OFF
DPR5C 22 25 DRP 0.208 OFF
DPR5D  0 25 DRP 0.132 OFF
*PARASITIC CAPACITANCES OF METAL LINES
CM3 3 0 200E-15
CM4 4 0 200E-15
CM5 5 0 200E-15
CM7 7 0 200E-15
CM8 8 0 50E-15
CM9 9 0 250E-15
CM10 10 0 50E-15
CM11 11 0 100E-15
CM12 12 0 100E-15
CM15 15 0 100E-15
CM18 18 0 100E-15
CM19 19 0 100E-15
CM20 20 0 100E-15
*BIAS VOLTAGES AND INPUTS
VCC 25 0 DC 5.0
VIN8 8 0 DC 3.5
VIN10 10 0 DC 3.5
*DEVICE MODELS

**********************************************************************
*
* CBP2.0 -- VERSION 3.1 -- 15 Apr 1987 SPEED: NOMINAL
* Additions 6 May 1987 --
* ZENER MODEL NAME CHANGE 8-26-87
*
*  VJ900_NOM models are nominal capacitance,
*  nominal beta, and nominal zener voltage models.

*
**********************************************************************
.MODEL T6NW NPN ( IS=3.885E-17 BF=128 NF=1 VAF=33.727
+IKF=.015571 ISE=0 NE=1.5 BR=2.366 NR=1 VAR=3.813
+IKR=.0002398 ISC=0 NC=1.5 RB=447.48 IRB=0 RBM=118.79
+RE=3.6743 RC=69.593 XTB=1.395 EG=1.115 XTI=4.004
+CJE=5.565E-14 VJE=.91 MJE=.419 TF=2.E-11 XTF=9.17
+VTF=2.24 ITF=.17493 PTF=0 CJC=6.8565E-14 VJC=.715 MJC=.38
+XCJC=.18423 TR=4.E-10 CJS=2.1623E-13 VJS=.567 MJS=.402
+FC=.5 )
```

8.4 SPICE Netlist *(continued)*

```
.MODEL TLN1 NPN ( IS=1.1322E-15 BF=128 NF=1 VAF=33.727
+IKF=.4538 ISE=0 NE=1.5 BR=17.238 NR=1 VAR=3.813
+IKR=.0069885 ISC=0 NC=1.5 RB=8.7667 IRB=0 RBM=2.8027
+RE=.12608 RC=4.0325 XTB=1.395 EG=1.115 XTI=4.004
+CJE=1.6218E-12 VJE=.91 MJE=.419 TF=2.E-11 XTF=9.17
+VTF=2.24 ITF=5.098 PTF=0 CJC=1.5687E-12 VJC=.715 MJC=.38
+XCJC=.15644 TR=4.E-10 CJS=1.1929E-12 VJS=.567 MJS=.402
+FC=.5 )

.MODEL T40NW NPN ( IS=7.548E-16 BF=128 NF=1 VAF=33.727
+IKF=.30253 ISE=0 NE=1.5 BR=5.746 NR=1 VAR=3.813
+IKR=.004659 ISC=0 NC=1.5 RB=16.745 IRB=0 RBM=5.0064
+RE=.18912 RC=4.1366 XTB=1.395 EG=1.115 XTI=4.004
+CJE=1.0812E-12 VJE=.91 MJE=.419 TF=2.E-11 XTF=9.17
+VTF=2.24 ITF=3.3986 PTF=0 CJC=1.0214E-12 VJC=.715 MJC=.38
+XCJC=.16019 TR=4.E-10 CJS=1.3357E-12 VJS=.567 MJS=.402
+FC=.5 )

.MODEL T48NW NPN ( IS=5.55E-16 BF=128 NF=1 VAF=33.727
+IKF=.22245 ISE=0 NE=1.5 BR=8.45 NR=1 VAR=3.813
+IKR=.0034257 ISC=0 NC=1.5 RB=48.262 IRB=0 RBM=7.1765
+RE=.2572 RC=5.7138 XTB=1.395 EG=1.115 XTI=4.004
+CJE=7.95E-13 VJE=.91 MJE=.419 TF=2.E-11 XTF=9.17 VTF=2.24
+ITF=2.499 PTF=0 CJC=6.8988E-13 VJC=.715 MJC=.38
+XCJC=.21797 TR=4.E-10 CJS=6.9873E-13 VJS=.567 MJS=.402
+FC=.5 )


.MODEL TVPA8 PNP ( IS=5.2163E-16 BF=100.2 NF=1
+VAF=11.015 IKF=.001324 ISE=0 NE=1.5 BR=9.8 NR=1 VAR=6.631
+IKR=.00040489 ISC=0 NC=1.5 RB=563 IRB=0 RBM=0 RE=4.21
+RC=146 XTB=2.806 EG=1.185 XTI=.1418 CJE=5.5136E-14
+VJE=.715 MJE=.38 TF=1.515E-11 XTF=13 VTF=2.56 ITF=0 PTF=0
+CJC=1.6889E-13 VJC=.76 MJC=.40191 XCJC=0 TR=6.E-9
+CJS=5.1968E-13 VJS=.76 MJS=.3738 FC=.5 )

.MODEL TVPA35 PNP ( IS=4.4512E-15 BF=100.2 NF=1
+VAF=11.015 IKF=.011299 ISE=0 NE=1.5 BR=9.8 NR=1 VAR=6.631
+IKR=.0034551 ISC=0 NC=1.5 RB=69.1 IRB=0 RBM=0 RE=.446
+RC=23.7 XTB=2.806 EG=1.185 XTI=.1418 CJE=4.4852E-13
+VJE=.715 MJE=.38 TF=1.515E-11 XTF=13 VTF=2.56 ITF=0 PTF=0
+CJC=8.1536E-13 VJC=.76 MJC=.61333 XCJC=0 TR=6.E-9
+CJS=1.9301E-12 VJS=.76 MJS=.3738 FC=.5 )

.MODEL TVPA40 PNP ( IS=5.1467E-15 BF=100.2 NF=1
+VAF=11.015 IKF=.013064 ISE=0 NE=1.5 BR=9.8 NR=1 VAR=6.631
+IKR=.003995 ISC=0 NC=1.5 RB=60.1 IRB=0 RBM=0 RE=.382
+RC=21.5 XTB=2.806 EG=1.185 XTI=.1418 CJE=5.1557E-13
+VJE=.715 MJE=.38 TF=1.515E-11 XTF=13 VTF=2.56 ITF=0 PTF=0
+CJC=8.2678E-13 VJC=.76 MJC=.69218 XCJC=0 TR=6.E-9
+CJS=1.9814E-12 VJS=.76 MJS=.3738 FC=.5 )
```

```
.MODEL DRP D ( IS=2.E-16 RS=0 N=1 EG=1.11 XTI=3 BV=15
+IBV=1.E-6 CJO=1.E-12 VJ=.715 M=.38 TT=0 FC=.5 )

.MODEL DRN D ( IS=2.E-16 RS=0 N=1 EG=1.11 XTI=3 BV=15
+IBV=1.E-6 CJO=1.E-12 VJ=.567 M=.402 TT=0 FC=.5 )

.MODEL SCH3 D ( IS=4.7E-16 RS=5230.1 N=1.02 EG=.83 XTI=2
+BV=13 IBV=1.E-6 CJO=4.67E-16 VJ=.83 M=.5 TT=0 FC=.5 )

.MODEL T6NWAC D ( IS=3.885E-17 RS=204 BV=4.8 IBV=1.E-6
+CJO=6.8565E-14 VJ=0.715 M=0.38 )
.END
```

8.5 SPICE Netlist Discussion

In this example extensive use has been made of comment statements. SPICE comment statements begin with an asterisk (*) and are used to identify subsections of the circuitry.

```
*SPICE INTEGRATOR EXAMPLE - VERSION D - 3-15-86
```

In most SPICE versions the first line is required to be the circuit name, and is repeated on the headings of the output listings. It is highly desirable to include version and date information in the circuit name to avoid confusion when reviewing old listings.

```
*BIAS GENERATOR
Q4 25 3 5 0 T6NW
Q9 3 4 0 0 T6NW
QJC1 3 4 3 0 TLN1
R1A 1 2 2013 TC=5.7E-4,6.9E-6
R1B 2 25 4075 TC=5.7E-4,6.9E-6
R1C 25 3 8200 TC=5.7E-4,6.9E-6
DPR1A 1 24 DRP 0.062 OFF
DPR1B 2 24 DRP 0.16 OFF
DPR1C 24 24 DRP 0.269 OFF
DPR1D 3 24 DRP 0.171 OFF
R2A 5 5 2013 TC=5.7E-4,6.9E-6
R2B 4 0 4075 TC=5.7E-4,6.9E-6
R2C 0 6 8200 TC=5.7E-4,6.9E-6
DPR2A 5 24 DRP 0.062 OFF
DPR2B 4 24 DRP 0.16 OFF
DPR2C 0 24 DRP 0.269 OFF
DPR2D 6 24 DRP 0.171 OFF
```

Bias generator

This segment of the code represents a DC circuit. In principle one could omit the parasitic diodes corresponding to the resistor parasitic capacitance since the junction capacitor QJC1 has a predominant influence on the AC behavior and stability. However, CAD considerations require their inclusion. To relieve circuit complexity during simulation, diodes connected between the same node or two DC nodes (DPR1C, DPR2C) could be omitted.

```
*INTEGRATOR
Q1 7 7 25 25 TVPA8
Q2 9 7 25 25 TVPA8
Q3 25 9 18 0 T6NW
Q5 7 8 11 0 T6NW
Q6 9 10 11 0 T6NW
Q7 11 5 12 0 T6NW
Q8 19 5 20 0 T6NW
```

Integrator transistors

These statements are rather straightforward, but note that the forth terminal on the devices is declared for all the devices. It is a good practice to include the forth terminal. The forth terminal on NPN transistors is always the most negative power supply used on the chip. The forth terminal on PNP transistors is the positive supply used to bias that PNP transistor's isolation tub.

```
*SCHOTTKY DIODE
DS1 10 23 SCH3 71
DS1GR 10 23 DRP 0.053 OFF
DS1SB 0 23 DRN 0.246 OFF
RDS1 23 9 103 TC=0.004
```

Schottky diode

The first statement represents the actual Schottky element. The second element represents the parasitic capacitance of the P type guard-ring. The third element represents the parasitic junction capacitance to the substrate. The fourth element represents the parasitic forward resistance of the Schottky diode. An extra node (node 23) must be added to model this device.

```
*AC ZENER DIODE
DZ1 19 18 T6NWAC
DZ1SB 18 0 DRN 0.263 OFF
```

Zener diode

This element is represented by a special "AC" model of the T6NW transistor, since the usual transistor model does not include avalanche breakdown. This model fails to represent the temperature dependence of the zener breakdown voltage, and hence is only good at room temperature. The diode DZISB represents the parasitic junction capacitance to the substrate.

```
*DIELECTRIC CAPACITOR
C1 9 15 1.45E-12
DC1T 15 25 DRP 1.211 OFF
DC1SB 0 25 DRN 0.860 OFF
```

Dielectric capacitor

The first statement represents the oxide capacitor. The second statement (DC1T) represents the parasitic capacitance between the lower plate and the isolation tub. The third statement (DC1SB) represents the parasitic capacitance between the isolation tub and the substrate.


```
*RESISTORS
R3A 13 12 260 TC=7.6E-4,2.05E-6
R3A 12 14 521 TC=7.6E-4,2.05E-6
R3A 14 0 1042 TC=7.6E-4,2.05E-6
DPR3A 13 25 DRP 0.049 OFF
DPR3B 12 25 DRP 0.125 OFF
DPR3C 14 25 DRP 0.208 OFF
DPR3D 0 25  DRP 0.132 OFF
R4A 15 16 2013 TC=5.7E-4,6.9E-6
R4B 16 17 4075 TC=5.7E-4,6.9E-6
R4C 17  0 8200 TC=5.7E-4,6.9E-6
DPR4A 15 24 DRP 0.062 OFF
DPR4B 16 24 DRP 0.16  OFF
DPR4C 17 24 DRP 0.269 OFF
DPR4D  0 24 DRP 0.171 OFF
R5A 21 20 260 TC=7.6E-4,2.05E-6
R5A 20 22 521 TC=7.6E-4,2.05E-6
R5A 22 0 1042 TC=7.6E-4,2.05E-6
DPR5A 21 25 DRP 0.049 OFF
DPR5B 20 25 DRP 0.125 OFF
DPR5C 22 25 DRP 0.208 OFF
DPR5D  0 25 DRP 0.132 OFF
```

Resistors

The resistors are shown using all of the segments and parasitics. VTC CAD software requires the inclusion of all resistor segments and parasitics. During simulation the parasitic diodes that are shorted out and connected to DC nodes may be omitted for shorter simulation runs.

```
*PARASITIC CAPACITANCES OF METAL LINES
  CM3 3 0 200E-15
  CM4 4 0 200E-15
  CM5 5 0 200E-15
  CM7 7 0 200E-15
  CM8 8 0 50E-15
  CM9 9 0 250E-15
  CM10 10 0 50E-15
  CM11 11 0 100E-15
  CM12 12 0 100E-15
  CM15 15 0 100E-15
  CM18 18 0 100E-15
  CM19 19 0 100E-15
  CM20 20 0 100E-15
```

Parasitic metal capacitances

The above lines of parasitic metal capacitances are estimates using 50 fF per element. Once the layout is completed by the designer the actual capacitance numbers should be included in the simulation file. All metal parasitics must be removed before submitting the netlist to VTC for layout verification.

9. MANUFACTURING TOLERANCES— WORST-CASE MODELS

As noted in SPICE Models section, three sets of models are provided which represent the worst-case manufacturing limits. The three model files are

- Worst-Case Slow, Low β Models,
- Nominal Models, and
- Worst-Case Fast, High β Models.

Simulations are normally done with the Nominal Models during the early phases of design.

Once a reasonably good design has been achieved, simulations should be run with both the worst-case slow and fast models. Worst-case slow models ensure that the circuit will be no slower that simulations predict if the metal, package, and loads are modeled correctly. Ordinarily, the worst-case fast models are used to check a circuit's AC stability.

The model sets provided are inadequate in some respects, since the random manufacturing variation is independent for the NPN and PNP transistors. That is, the NPNs may be "fast" and the PNPs "slow" on a given chip, while the NPNs may have high β and the PNPs low β simultaneously. The designer must judge whether these additional extreme cases are important for the circuit, and if necessary must edit the SPICE model files to create additional worst cases (e.g., simultaneous worst-case high NPN β with worst-case low PNP β).

It is also necessary to look at worst-case resistor modeling. Here there are four important cases:

1) P+ resistors 20% high, P– resistors 20% high
2) P+ resistors 20% low, P– resistors 20% high
3) P+ resistors 20% high, P– resistors 20% low
4) P+ resistors 20% low, P– resistors 20% low

The different transistor types "track" quite closely among themselves. For example if one P+ resistor is 12% high in value all of the others will also be very nearly 12% high.

10. DESIGN FOR A WIDE TEMPERATURE AND SUPPLY VOLTAGE RANGE

Nearly all ICs must operate over a substantial range of temperatures and supply voltages. SPICE simulations are a good tool for determining the effects of temperature and supply voltage, and when a satisfactory preliminary design has been achieved the SPICE simulations should be re-run for worst cases. The nature of the worst-case depends on the design objectives. Below we show the cases which would be simulated for a circuit operating at a nominal 5 V V_{CC} (+/– 10%) with expected ambient temperatures ranging from 0 to 70°C.

In considering the temperature aspects of the application, it is assumed that the package has a thermal impedance of 35°C/W (chip-to-ambient under the normal air-flow conditions) and that the chip dissipates 450 mW. Then the worst-case temperatures are: 1) 0°C for the low temperature, corresponding to a cold start at this temperature; and 2) 70 + 35*.45 = 86°C for the high temperature, corresponding to the highest service chip (junction) temperature after warm-up of the chip.

The SPICE simulations would then be done for the following cases:

1) V_{CC} = 5.5 V, T = 0°C
2) V_{CC} = 4.5 V, T = 0°C
3) V_{CC} = 5.5 V, T = 86°C
4) V_{CC} = 4.5 V, T = 86°C

The scheme with two supply voltages would be somewhat more complex, with eight worst-cases.

Typically, the high-voltage problems occur due to breakdown voltages (most troublesome at high temperatures), while the low-voltage problems often involve device saturation (which is most troublesome for low temperatures). Junction leakage currents roughly double each 10°C, and are worst at the high-temperature limit. β increases substantially with increasing temperature, so that base current effects are most important at the low temperature extreme.

For circuits which use two supply voltages, it is also important to do simulations of power-supply sequencing to identify hazards. The resistor parasitic diodes should all be included in the simulation, with the N type ends connected to the two most positive supply voltages as they are done in the reach chip. Various power-on sequences should then be simulated in SPICE to verify that no problems occur. Forward-biasing of any parasitic diode can indicate serious problems.

11. SPICE SIMULATION PROBLEMS

The SPICE simulation program is based on numerical integration of (nonlinear) differential equations. In most cases it does a good job; but there are, nevertheless, cases where it does not succeed in imitating real circuits. Sometimes the problem can be overcome by simple "tricks" such as those described here.

Flip-flops

A flip-flop or other bistable circuit has two stable states. The SPICE program may have a hard time deciding which one is the right one. A simple symmetric RS flip-flop may sit in an unstable state upon startup for quite a long time before "roundoff noise" pushes it (randomly) into one or the other of its stable states.

Most real flip-flops have SET, RESET, or PRESET inputs; by initially putting the right voltage levels on these, the circuit can be "forced" into the correct state. If this fails, the circuit can be made slightly asymmetric (for example, by making two nominally equal resistors 1% different).

Oscillators

Several types of astable oscillators are commonly used—LC, RC relaxation, ring, etc. All of these have the feature that there is no DC state. Since SPICE must find a DC solution before looking for the transient solution, it cannot be used for these circuits with the usual methods.

A common trick is to start the circuit with all power supply voltages at zero value, and then ramp them up during the transient solution. SPICE easily finds the "trivial" DC solution with all voltages and currents equal to zero.

Schmitt triggers

The Schmitt trigger uses feedback in such a way that hysteresis is produced (i.e., the circuit solution is double-valued).

SPICE has a routine for automatically choosing the time step to ensure that the changes in solution are not "too big". If the changes are too large, SPICE chooses a smaller time step. An implicit assumption is the circuit behavior is continuous (i.e., a smaller time step always leads to a smaller change in the solution).

For Schmitt triggers there is a "catastrophic" change in the solution at the switching point where the circuit goes from one solution to the other. SPICE will use ever-smaller time steps trying to keep the change in the solution small, but sometimes it never makes it. SPICE then ceases execution and puts out a "TIME STEP TOO SMALL" error message. The answer here lies in adjusting the convergence limits and/or using a SPICE version which permits one to fix the time step.

High-gain feedback loops

A feedback loop requires very accurate solution of the circuit equations. Suppose that the loop has a gain of 200,000 and that the output solution should be accurate to 10 mV. This requires that the input solution be accurate to .010/200 000 = 5E-8 V. SPICE options can be used to increase solution accuracy—but the accuracy is ultimately limited by the finite word length and roundoff errors of the computer used (most SPICE versions use double-precision variables).

12. VJ900 LAYOUT

12.1 Introduction

When designing high-speed analog circuitry, the layout is as much a factor in the design as the actual architecture chosen and simulation results are. An important thing for a designer to remember is that a poor layout can result in performance levels far below what is expected and in the worst-case the circuit could be completely nonfunctional. Metal capacitances that could be ignored at 1 MHz become very significant at 100 MHz and higher. Device matching also is a consideration and must be taken into account during design. Because layout is so important to the success of a design, it must be considered early in the design cycle.

This section of the VJ900 User's Guide will give the designer a detailed set of instructions on how to do layout on the VJ900 family. The following pages contain general procedures for layout, layout specifics with the VJ900 family, a description of each die plot, instructions for showing metal interconnections on mylar, a detailed description of each device layout, and device matching for the VJ900 family.

12.2 A General Procedure for Layout

The procedure as outlined is this section has been proven to be effective in producing the best circuit layout possible.

Before circuit layout can begin it is important to prepare certain circuit information to aid the layout process. The following three steps will provide the required information for beginning layout.

Circuit Planning

First, examine the circuit and mark the schematic(s) for devices that need good device matching and mark interconnections that carry more than 3.0mA. A good way of marking the schematics for matching is to circle the groups of devices that must be matched; and a good way of marking the interconnections is to draw an arrow in the direction of current flow and writing the maximum steady state current on the arrow.

Second, examine the circuit and assign a priority level to each circuit subsection. The priorities should be set according to the importance level of each subcircuits specifications to circuit operation. Then assign a priority to each set of matched devices in each subcircuit.

Third, calculate the total amount of current required in each supply in each subcircuit and note it on each subcircuit schematic.

Layout

At this point, all of the information is available to start the layout of the circuit. A detailed floorplan of the chip should be generated first. To do a general floorplan of the chip, draw the chip to scale with only the pads and resistor isolation tubs.

Using the die plot as a guide, estimate the area were each subcircuit would be placed, box that area in, and mark it with the name of the subcircuit. When placing circuit blocks, high-current circuitry should be placed close to the pads.

Next, route the power busing using the power supply current data to calculate the bus widths required for acceptable I/R drops. VTC suggests that second metal be used for all power busing because second metal can carry 2.5 times more current for a given width, as compared to first metal. The biasing of the resistor tubs and substrate should be considered when sketching the power busing, as routing to the tub and substrate contacts may be difficult after the circuit has been routed.

Now that a general floorplan has been completed, the detailed layout work can begin. Each subcircuit should be worked on individually and in the order set by the priority attached to them. When working on a subcircuit layout, the components should be placed and then the routing should be added to provide the interconnect. Matched devices should be placed first and in the order specified by the priority assigned to them.

The metal routing can also be a factor in device matching. When matching devices, the metal routing to these devices should be kept as symmetrical as possible. The maximum steady state current in the interconnection metal is also important. If the current is marked as more than 3 mA, then the number of vias (the connection between first and second metal) will have to be more than one (a via's maximum rated current is 3 mA). If the current is marked as more than 4 mA, then the first metal interconnect will have to be wider than minimum; and if the current is marked as greater than 15 mA, then second metal interconnect will have to be wider than the minimum.

After each subcircuit has been placed and its interconnection has been routed, the interconnection between subcircuits should be completed again in the order set by the subcircuits priority. After all of the circuit interconnection has been completed, the power busing, as drawn in the first layout step, should be enhanced where possible to provide as much margin as possible. In VTC's experience, the most frequent cause of analog master chip failure is inadequate power bussing.

Now that the layout is complete, it should be cross-checked to the schematics one last time before it's transferred to VTC. The best way to check the layout is to have a person that is not familiar with the circuit cross-check the layout to the schematic. Many errors that are not seen due to familiarity can be found by this method and much time can be saved once the design is handed-off to VTC.

12.3 Layout of the VJ900 AMCs

In the VJ900 Design Kit a plot of each of the VJ900 family members predefined layers is provided. The designer defines the layout by fixing a clear piece of mylar over the plot and marking the mylar with the coordinate marks shown on the plots, the required metal routing, and the text that identifies the components. To place a component, the SPICE name of the device should be written over the device in black ink. The metal routing should be drawn on the mylar following the grid lines as shown on the die plots. Wider than minimum lines are limited to a integer number of the grid lines.

12.4 Die Plot Descriptions

This section describes the VJ900 die plots in detail. Each of the chip plots is printed using the same fill patterns and the same layers. The grid is plotted using a thin dashed line in both directions. The first metal that is associated with each device is shown with a light grey fill pattern. The isolation (thin oxide region) is shown with a thin solid line. The Channel Stop (defines the outer edge of isolated n region in the p substrate) is shown with a bold dashed line. See Figure 12.2.

Die Specific Information

Each of the VJ900 family members has its own die plot and each will have some differences for the other family members. These family member specifics are described in the next few sections.

VJ910 Specifics

The VJ910 uses a 4µ x 4µ grid spacing to allow routing first and second metal in both directions using the minimum spacings in both directions.

VJ930, VJ960, VJ970, and VJ990 Specifics

The remaining family members all use the same grid spacing, 8µ x 14µ. The preferred direction for first metal is vertical while the preferred direction for second metal is horizontal. Table 1 shows each of the VJ900 family members die size and the scale factor of its die plot.

Table 12.1: Die Size and Scale Factor Metal Routing

Family Member	Die Size (mils)	Scale Factor
VJ910	42 x 44	1000
VJ930	77 x 75	500
VJ960	104 x 91	400
VJ970	134 x 118	375
VJ990	172 x 149	295

The interconnect of devices on VJ900 die is accomplished using three processing layers. These layers are two isolated metal layers (first and second metal) and one layer (via) used as an interconnection between the two metal layers. These interconnections are bounded by certain rules. Some of these rules are physical and some of them are electrical. The physical rules are those dealing with the widths, spacings, and required minimum overlaps of each of these interconnection layers. The physical rules are guaranteed if the metal routes are kept on the correct grid spacings as outlined below.

However, the electrical rules can only be guaranteed by the designer. There are two electrical rules that must be followed. The most important of the two is electromigration. Electromigration is a metal line wear-out mechanism when too much current is passed through a metal line and the metal is actually moved "downstream" and the metal line opens up at a weak point. The electromigration rules for the process used to fabricate the VJ900 family are outlined in Section 6.4. The interconnection's the point that is the weakest is the via. One via is limited to 3 mA of current.

The other electrical concern is voltage drop on high-current lines. Even though a line is wide enough for electromigration, the metal line may still have significant voltage drop because of its resistance. The metal line resistance numbers are also given in Section 6.4. High-current metal lines should also be checked for this problem.

12.5 VJ910 Routing

When working on the metal routing on the VJ910 it is important to know that the plot is 1000x and the shown grid is 4µ x 4µ. This allows both metal layers to be routed in either direction with the least difficulty. To show a first metal route use a permanent BLUE marker and draw a line along a grid line. This line is the center of the actual metal line. Because first metal routing has a minimum pitch of 8µ, one grid line on

each side of the drawn line must be left "open" for the required space between adjacent first metal lines.

To show a second metal route, use a permanent RED marker and draw a line along a grid line. This line is the center of the actual metal line. Because second metal routing has a minimum pitch of 12μ, two grid lines on each side of the drawn line must be left "open" for the required space between adjacent second metal lines.

To show a single via, use a permanent GREEN marker and draw an X on a grid line crossing of first and second metal along a grid line. Vias that are to be electrically-isolated are not allowed on adjacent metal lines drawn at the minimum spacing. Electrically-isolated vias may be on diagonal grid points at minimum first and second metal spacings.

To show a metal line that is wider than minimum width, draw another line on the grid line next to the original line and shade in between them. It is important to note that wider than minimum lines require the same spacings as minimum lines.

To show a via connection of more than one via, draw a green circle around the area and print the number of vias required inside the circle. To do this it is important to know the required via spacings and metal overlaps. The via center-to-center spacing is 8μ; the width of first metal required for one via is 6μ; and the width of second metal required for one via is 10μ.

VJ910 Metal Routing Example

A metal routing example using the three layers of interconnect is shown in Figure 12.1. This figure shows a power bus line (route A) with greater-than-minimum width lines and two signal routes (routes B & C) using minimum line widths. All of the routes in the example are drawn using all three layers and using the minimum spacings allowed.

It is relatively easy to route signals using minimum-width lines. All that is required is that a single line be drawn on the grid and that the spacing rules, as defined above, are followed. The routing of wider lines is no more difficult except that the line width is not just a integer number of minimum-line-widths. To mark a wide line fill between two lines that mark the edges of the line. The outer edges of the line are just

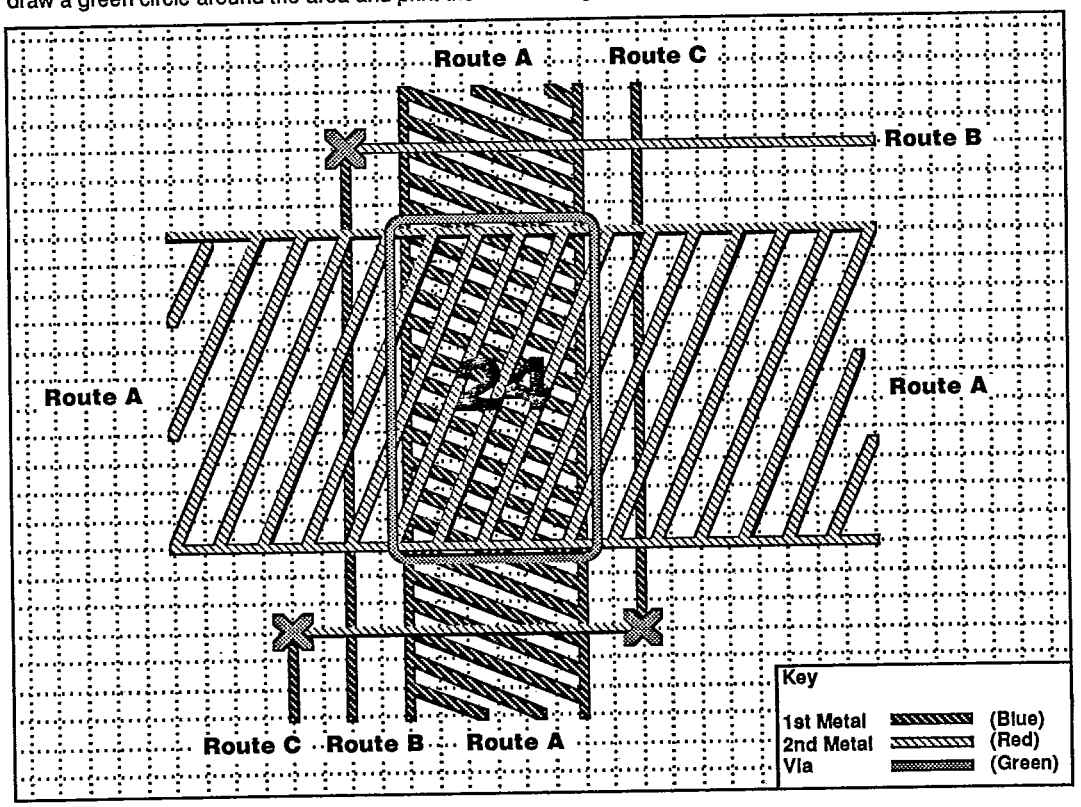


Figure 12.1: VJ910 Metal Routing Example

like minimum-width lines and require the same spacings as normal lines.

To calculate the width of a wider-than-minimum wide line follow the following equation:

Line Width = Number of Grid Spacings(4μ) + Standard Line Width.

As an example, the first and second metal line widths of route A are calculated below. Where the standard first metal line width is 6μ and the standard second metal line width is 8μ,

First Metal Line Width = 6(4μ) + 6μ = 30μ

Second Metal Line Width = 11(4μ) + 8μ = 52μ.

Multiple vias also need to be marked differently than a single via. To calculate the total number of vias that can be placed in any one area,

Vx = (First Metal Line Width - 6) / 8 + 1 round down to integer
Vy = (Second Metal Line Width - 10) / 8 + 1 round down to integer

Number of Vias = Vx(Vy).

As an example, the number of vias used in route A is calculated below:

Vx = (30μ - 6)/8 + 1 = 4.0
Vy = (52μ - 8)/8 + 1 = 6.5 (6.0)

Number of Vias = (4)6 = 24.

12.6 VJ930, VJ960, VJ970, & VJ990 Routing

When working on the metal routing on the VJ930, VJ960, VJ970, or VJ990 it is important to know what the plot scale is and that the shown grid is 8μ x 14μ. This allows both metal layers to be routed in either direction, although the preferred direction for first metal is vertical and the preferred direction for second metal is horizontal.

To show a first metal route use a permanent BLUE marker and draw a line along a grid line. Routing of first metal in either direction requires only one grid line. No grid lines are required as a spacing between adjacent first metal lines.

To show a second metal route use a permanent RED marker and draw a line along a grid line. Routing of second metal in the horizontal direction, or on the 14μ grid, requires only one grid line. Routing of second metal in the vertical direction, or on the 8μ grid, requires one grid line to be left "open" as a space between adjacent second metal lines, because the minimum second metal pitch is greater than 8μ.

To show a single via use a permanent GREEN marker and draw an X on a grid line crossing of first and second metal along a grid line. Vias that are to be electrically-isolated are not allowed on adjacent grid points. Vias on diagonal grid points are allowed.

To show a metal line that is wider-than-minimum width, draw another line on the grid line next to the original line and shade in between them. It is important to note that wider-than-minimum lines require the same spacings as minimum lines.

To show a via connection of more than one via, draw a green circle around the area and print the number of vias required. To do this it is important to know the required via spacings and metal overlaps. The via center to center spacing is 8μ; the width of first metal required for one via is 6μ; and the width of second metal required for one via is 10μ.

VJ930, VJ960, VJ970, or VJ990 Metal Routing Example

A metal routing example using the three layers of interconnect is shown in Figure 12.2. This figure shows a power bus line (route A) with greater-than-minimum-width lines and two signal routes (routes B & C) using minimum line widths. All of the routes in the example are drawn using all three layers and using the minimum spacings allowed.

It is relatively easy to route signals using minimum-width lines. All that is required is that a single line be drawn on the grid and that the spacing rules as defined above are followed. The routing of wider lines is no more difficult except that the line width is not just a integer number of minimum lines wide. To mark a wide line fill between two lines that mark the edges of the line. The outer edges of the line are just like minimum-width lines and require the same spacings as normal lines.

To calculate the width of a wider-than-minimum wide line follow the following equation:

Line Width = Number of Grid Spacings(Grid Dimension) + Standard Line Width.

As an example, the first and second metal line widths of route A are calculated below. Where the standard first metal line width is 6μ and the standard second metal line width is 8μ, and the vertical grid dimension is 8μ and the horizontal grid dimension is 14μ,

First Metal Line Width = 3(8μ) + 6μ = 30μ

Second Metal Line Width = 3(14μ) + 8μ = 50μ.

Multiple vias also need to be marked differently than a single via. To calculate the total number of vias that can be placed in any one area follow,

Vx = (First Metal Line Width - 6)/8 round down to integer
Vy = (Second Metal Line Width - 10)/8 round down to integer

Number of vias = Vx(Vy).

As an example, the number of vias used in route A is calculated below:

Vx = (30μ - 6)/8 + 1 = 4.0 (4)
Vy = (50 μ - 8)/8 + 1 = 6.25 (6)

Number of Vias = (4)6 = 24.

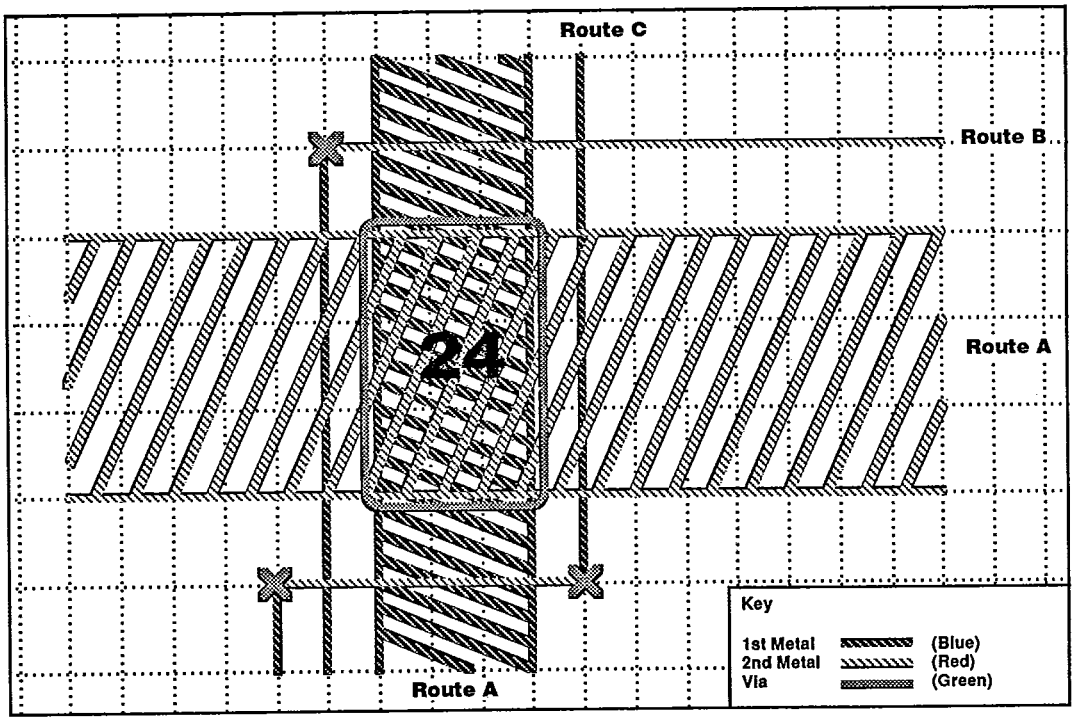


Figure 12.2: VJ930, VJ960, VJ970, or VJ990 Metal Routing Example

12.7 Component Details

The following sections describe the component layout and the metal connection points. A device plot along with the schematic representation are shown for each device.

VJ910 COMPONENTS:

T48NW

The T48NW transistor is a 12.5 mA NPN. The transistor has two collector contacts, three base contacts, and four emitter contacts. This transistor was designed to be used as a single device, operating the device in either a split collector or split emitter configuration is not allowed. The emitter, base, and collector first metal stripes are identified on the device plot with an E, B, or C placed on the metal stripe. Contact to the device can be made only with first metal.

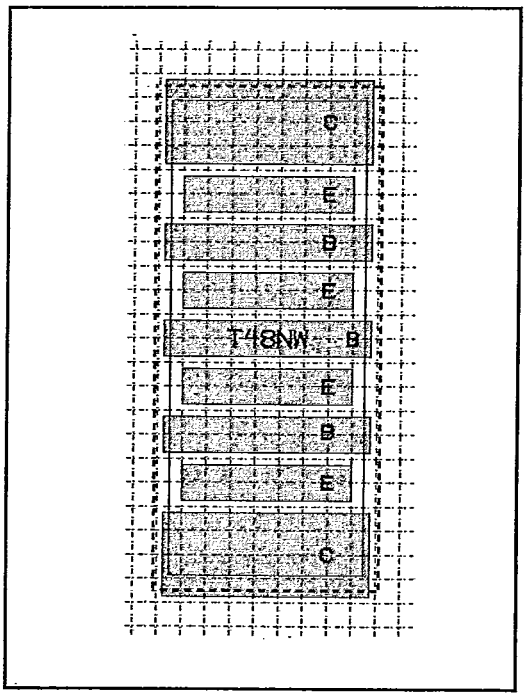


Figure 12.3: T48NW

T6NW

The T6NW transistor is a 1 mA NPN. The transistor has one collector, emitter, and base contact. The contacts are first metal as shown on the device below. The collector, emitter, and base metal are marked with a C, E, and B, respectively. Contact to the device can be made only with first metal.

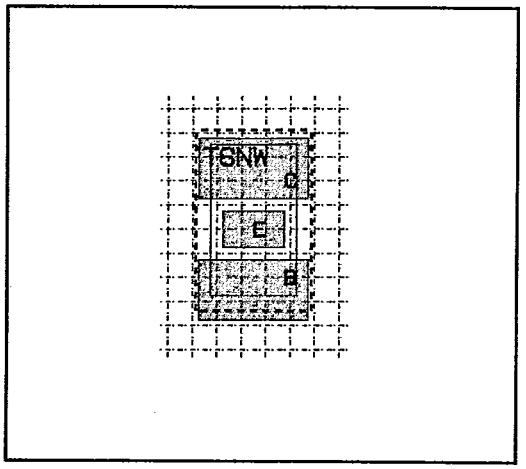


Figure 12.4: T6NW

TVPA40 (facing page)

The TVPA40 transistor is a 12.5 mA PNP. The transistor has three collector contacts, two base contacts, and four emitter contacts. This transistor was designed to be used as a single device, operating the device in either a split collector or split emitter configuration is not allowed. The contacts are first metal as shown on the device. The collector, emitter, and base metal are marked with a C, E, and B, respectively. Contact to the device can be made only with first metal.

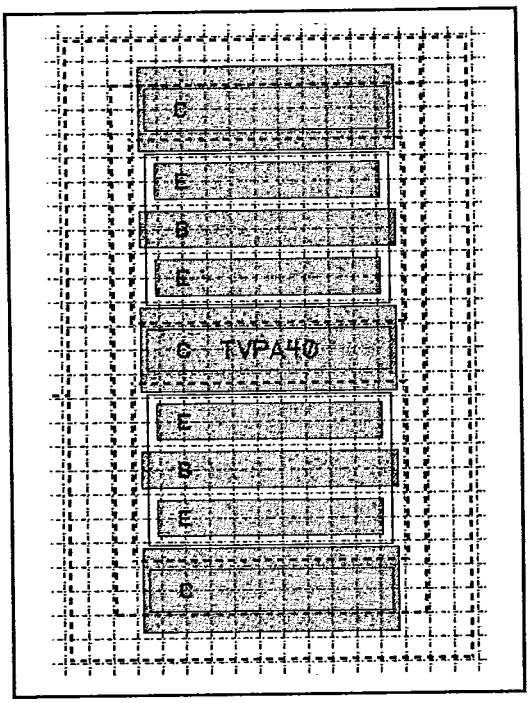


Figure 12.5: TVPA40

TVPA8

The TVPA8 transistor is a 1 mA PNP. The transistor has one collector, emitter, and base contact. The contacts are first metal as shown on the device below. The collector, emitter, and base metal are marked with a C, E, and B, respectively. Contact to the device can be made only with first metal.

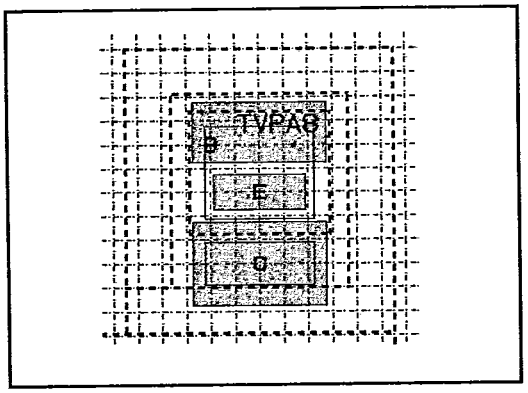


Figure 12.6: TVPA8

RE586

The RE586 resistor is a single enhancement resistor. The resistor has two contacts. The contacts are first metal as shown on the device below. Contact to the device can be made only with first metal.

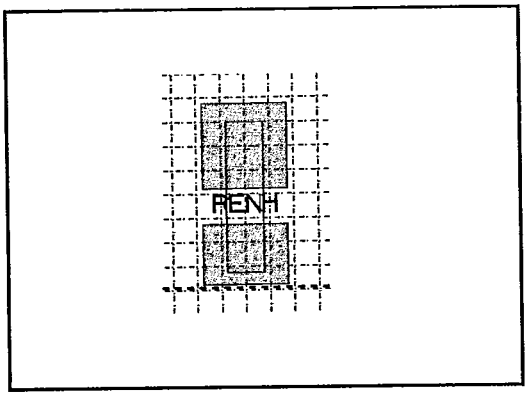


Figure 12.7: RE586

RB5090

The RB5090 resistor is a single base resistor. The resistor has two contacts. The contacts are first metal as shown on the device below. Contact to the device can be made only with first metal.

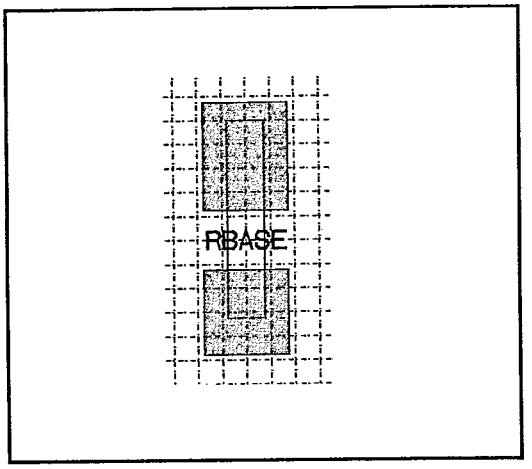


Figure 12.8: RB5090

RTIW

The RTIW resistor is a single Ti/W resistor stripe. Contact to the device is made by overlapping first metal over the resistor segment. The resistance is set by the length of resistor segment between the first metal contacts. Vias are not allowed over the resistor segment.

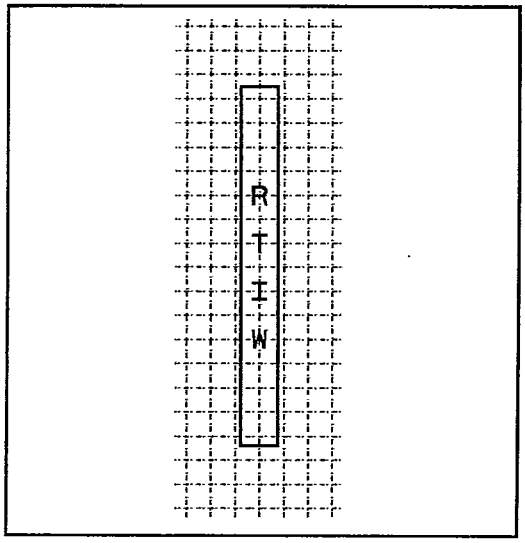


Figure 12.9: RTIW

VC1

The VC1 contact is a contact to the resistor and PNP isolation tub. This device is a single contact using first metal. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted as shown below.

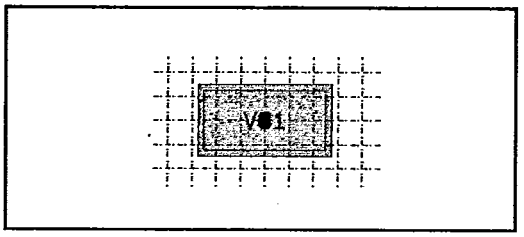


Figure 12.10: VC1

SC1

The SC1 contact is a contact to the circuit substrate. This device is a single contact using first metal. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown below.

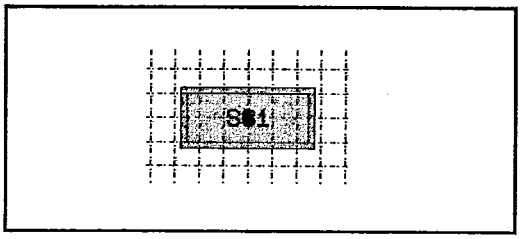


Figure 12.11: SC1

PAD

The Pad is the interconnection point to the circuit from outside the integrated circuit. The pad device uses first metal, via, and second metal. Contact to the Pad can be made using first metal or second metal. Vias are not required to make contact to the pad. First or second metal routes not connected to the pad must be kept a minimum of 25µ from an active pad. The circuit pin name, SPICE node number and package pin number must be printed on the pad where shown.

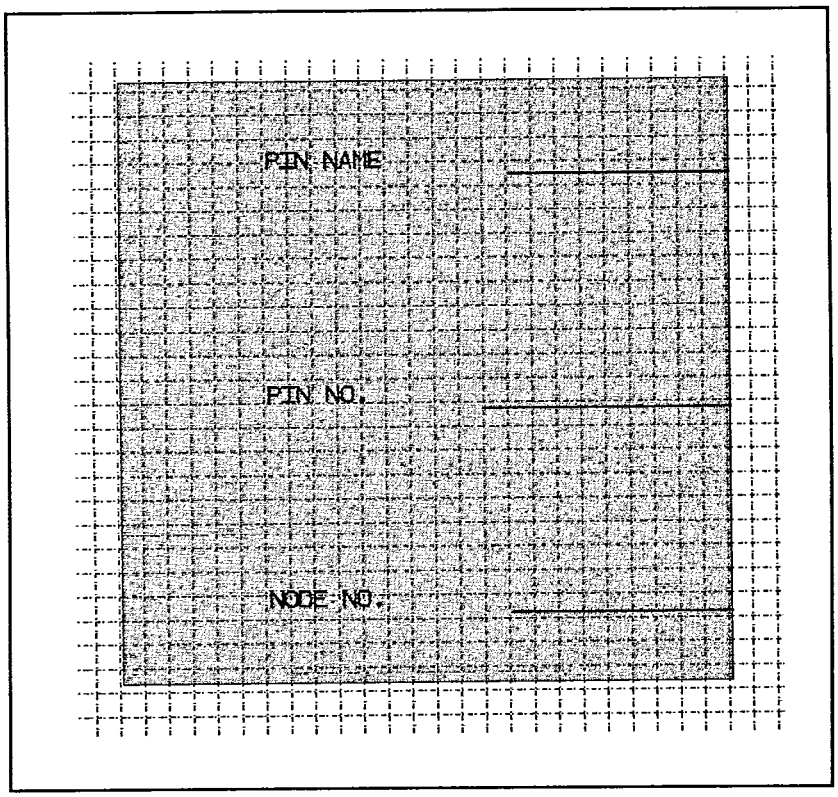


Figure 12.12: PAD

VJ930, VJ960, VJ970, & VJ990 COMPONENTS:

T6NW

The T6NW transistor is a 1 mA NPN. The transistor has one collector, emitter, and base contact. The contacts are first metal as shown on the device at right. The collector, emitter, and base metal are marked with a C, E, and B, respectively. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown at right.

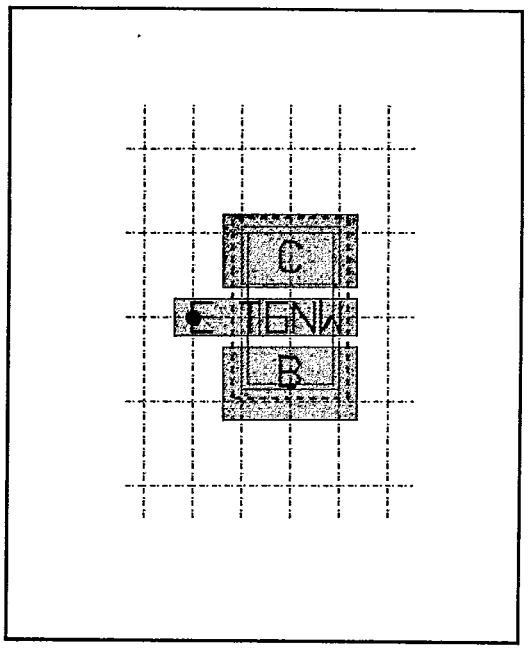


Figure 12.13: T6NW

TLN1

The TLN1 transistor is a low-noise 10 mA NPN. The transistor has two collector contacts, five base contacts, and four emitter contacts. This transistor was designed to be used as a single device, operating the device in either a split collector or split emitter configuration is not allowed. The contacts are first metal as shown on the device below. The collector, emitter, and base metal are marked with a C, E, and B, respectively. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown below.

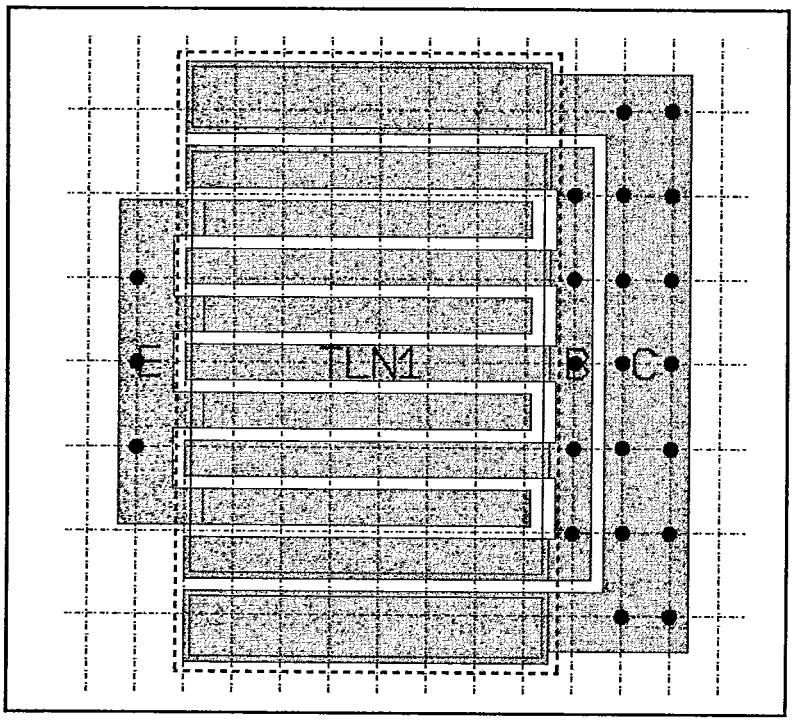


Figure 12.14: TLN1

T-42-21

T40NW

The T40NW transistor is a 22 mA NPN. The transistor has three collector contacts, eight base contacts, and six emitter contacts. This transistor was designed to be used as a single device, operating the device in either a split collector or split emitter configuration is not allowed. The contacts are first metal as shown on the device at right. The collector, emitter, and base metal are marked with a C, E, and B respectively. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown at right.

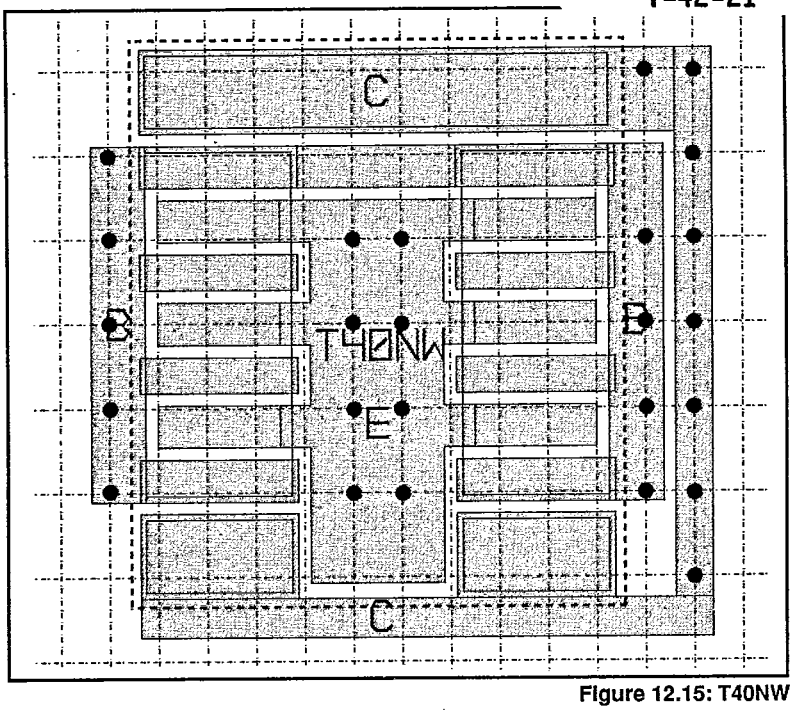


Figure 12.15: T40NW

TVPA8

The TVPA8 transistor is a1 mA PNP. The transistor has one collector, emitter, and base contact. The contacts are first metal as shown on the device below. The collector, emitter, and base metal are marked with a C, E, and B, respectively. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown below.

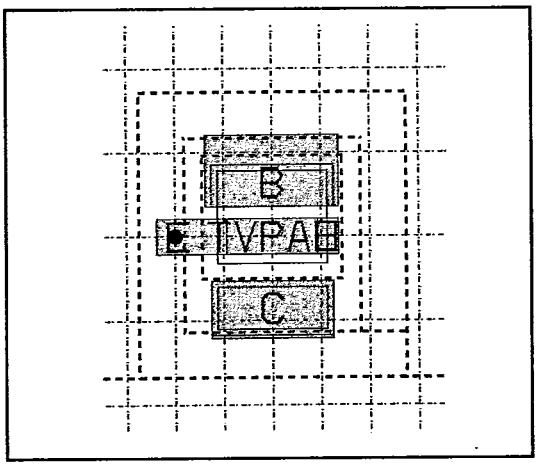


Figure 12.16: TVPA8

TVPA35

The TVPA35 transistor is a 9.1 mA PNP. The transistor has three collector contacts, two base contacts, and four emitter contacts. This transistor was designed to be used as a single device, operating the device in either a split collector or split emitter configuration is not allowed. The contacts are first metal as shown on the device below. The collector, emitter, and base metal are marked with a C, E, and B, respectively. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown below.

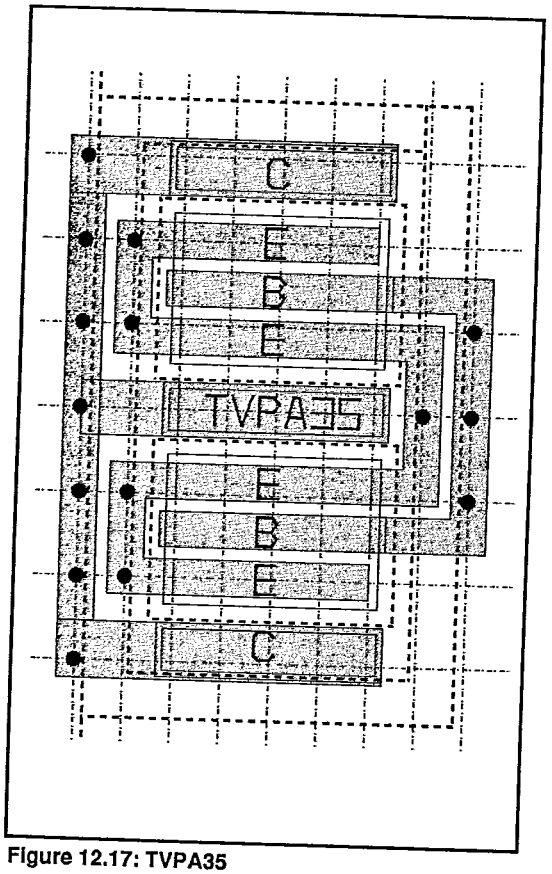


Figure 12.17: TVPA35

SDGR1

The SDGR1 diode is a 0.2 mA Schottky diode. This Schottky diode has one anode and cathode contact. The anode and cathode are marked with an A and C, respectively. Contact to the device can be made only with first metal.

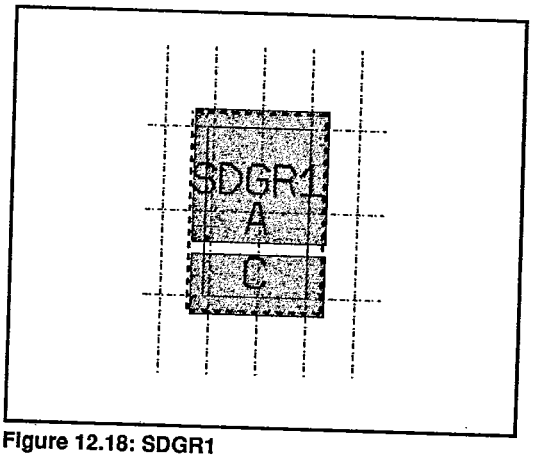


Figure 12.18: SDGR1

SDGR40

The SDGR40 diode is a 10 mA Schottky diode. This Schottky diode has one anode and cathode contact. The anode and cathode are marked with an A and C, respectively. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown below.

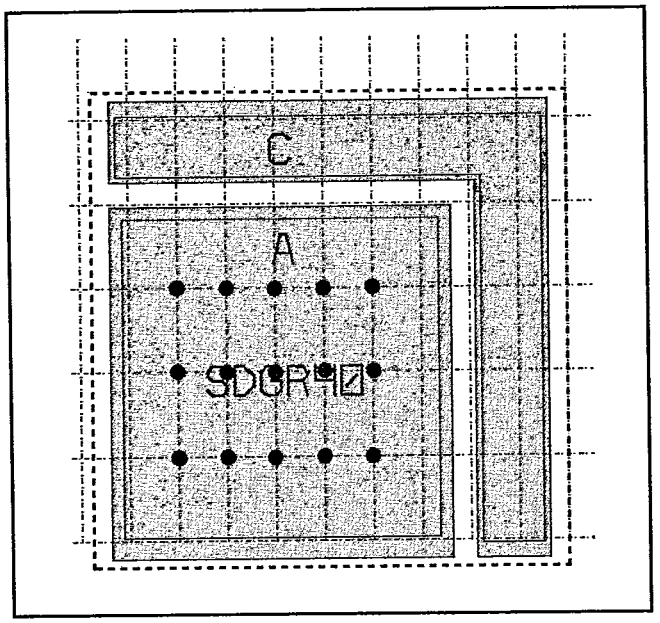


Figure 12.19: SDGR40

RETAP

The RETAP resistor is a triple series enhancement resistor. The resistor has four contacts. The resistor value directly related to the resistor segment length. The contacts are first metal as shown on the device below. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown below.

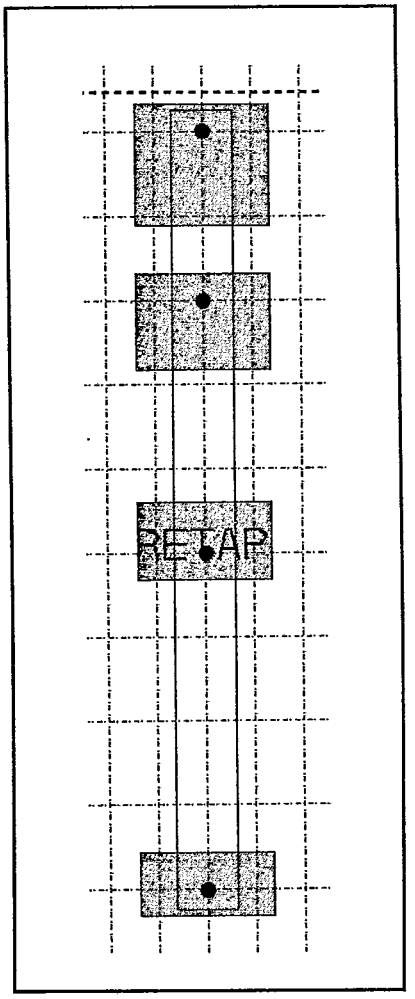


Figure 12.20: RETAP

RBTAP

The RBTAP resistor is a triple series base resistor. The resistor has four contacts. The resistor value directly related to the resistor segment length. The contacts are first metal as shown on the device below. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown below.

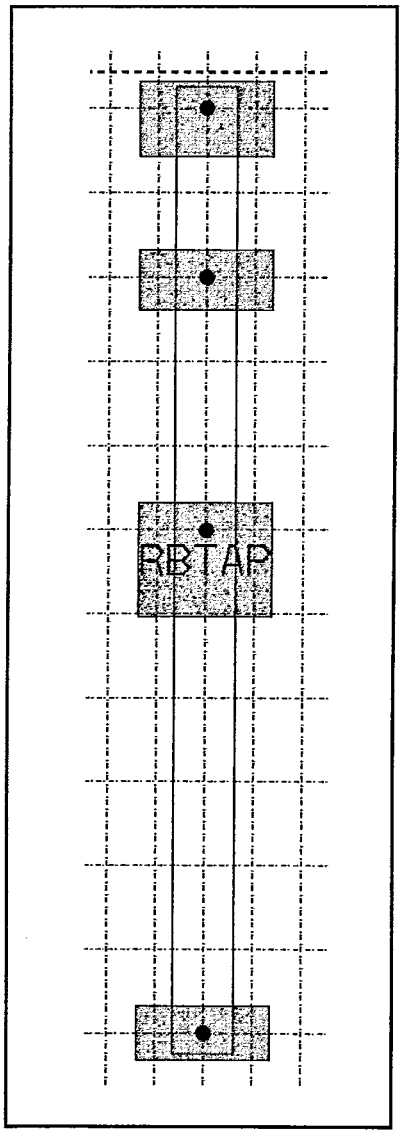


Figure 12.21 RBTAP

DCAP

The DCAP capacitor is a 1.2 pF dielectric capacitor. The capacitor has three contacts, a top plate, bottom plate, and an isolation tub. These three contacts are marked as POS, NEG, and TUB, respectively. The contacts are first metal as shown on the device below. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown below.

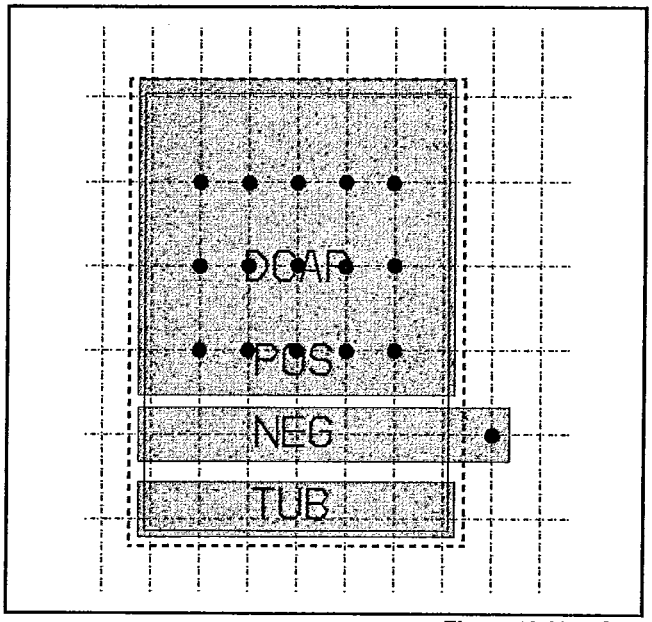


Figure 12.22: DCAP

VC1

The VC1 contact is a contact to the resistor and PNP isolation tub. This device is a single contact using first metal. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown below.

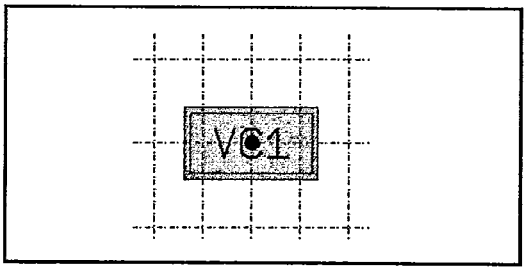


Figure 12.23: VC1

SC1

The SC1 contact is a contact to the circuit substrate. This device is a single contact using first metal. Contact to the device can be made only with first metal and via. A via can only be placed on the device where the grid intersection is dotted on the device shown at right.

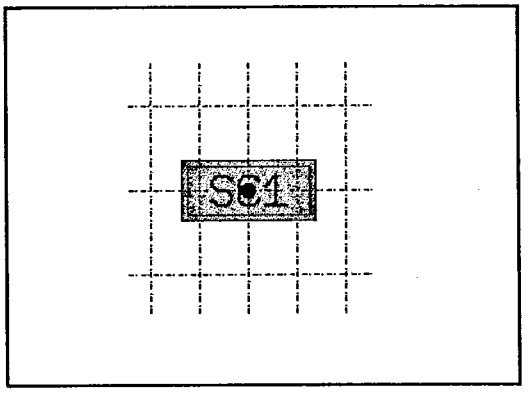


Figure 12.24: SC1

PAD

The PAD is the interconnection point to the circuit from outside the integrated circuit. The PAD device uses first metal, via, and second metal. Contact to the PAD can be made using first metal or second metal. Vias are not required to make contact to the pad. First or second metal routes not connected to the pad must be kept a minimum of 25µ from an active pad. The circuit pin name, SPICE node number and package pin number must be printed on the device where shown.

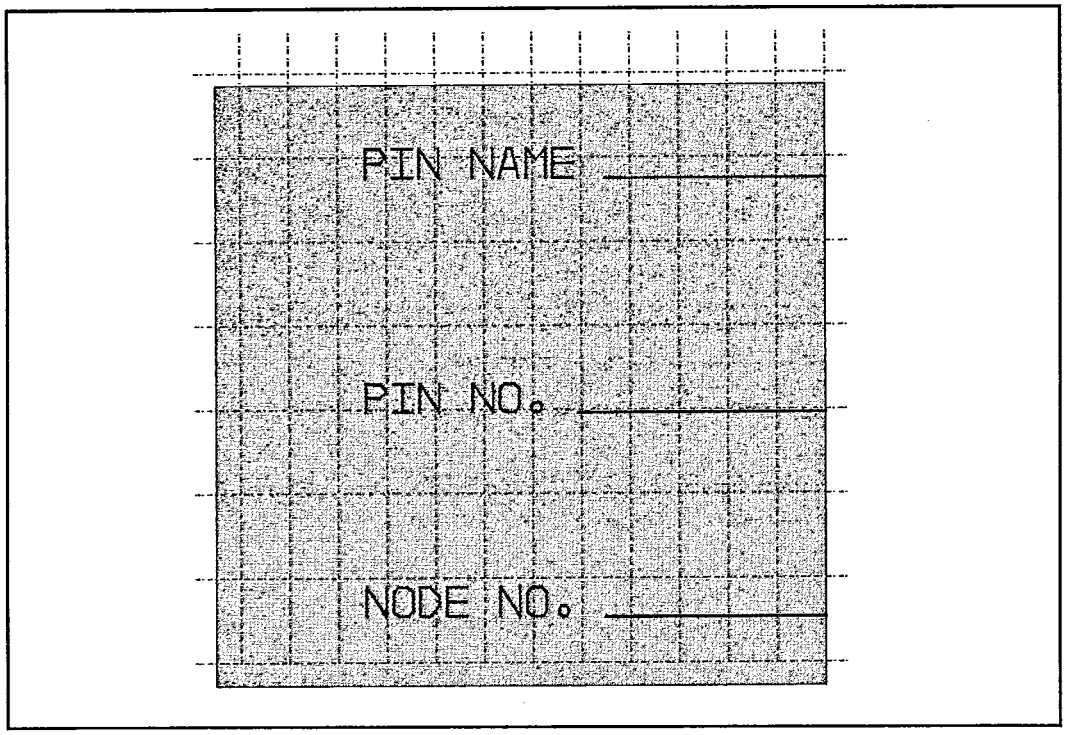


Figure 12.25: PAD

12.8 Device Matching

When designing on an integrated circuit the designer has to take into account the fact that the tolerance on components from die to die and wafer to wafer is poor. The one redeeming factor is that devices that are close to each other on a die will match (or track) each other typically to less than 1% on most parameters. Because of this the design of integrated circuitry has come to rely on matching to provide precision circuitry. The three main causes of device mismatch are process variations across a wafer, temperature variance across a die, and mechanical stress across a die. The mismatch between devices is directly related to the distance between devices, therefore to get the best device matching devices should be of the same type and be placed as close to each other as possible.

There are design techniques that can be used to improve the standard device matching figures as stated for one device to another. These techniques are discussed in this manual in the device sections. Also more information can be found on this subject in the texts described in the VJ900 User's Guide bibliography, Section 1.7.