SONY

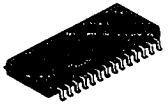
CXD1077M

8-mm Video AD/DA Converter

Description

CXD1077M is a 10-bit A/D, D/A converter developed for PCM audio of 8-mm video. It permits configuration of a PCM recording/playback system by combining it with the digital signal processing LSIs CX23011 and CX23012 and the analog noise reduction IC CX20099.

28 pin SOP (Plastic)



Features

- 5V single power supply
- Adoption of the integrating method achieves a low distortion factor 0.1% (Typ.), 5V in operation.
- The built-in integrator and sample-hold circuit reduces the number of external parts.
- The REC mode and the PB mode can be set with external signals.

Functions

- Sample-hold of input analog signal in the REC mode, and resample-hold of output analog signal in the PB mode.
- R time sharing A/D and D/A conversion based on the integrating method.
- Serial data input/output with LSB data leading.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3 to (V_{DD} + 0.3)	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

• Supply voltage	Vcc	4.75 to 5.25	V

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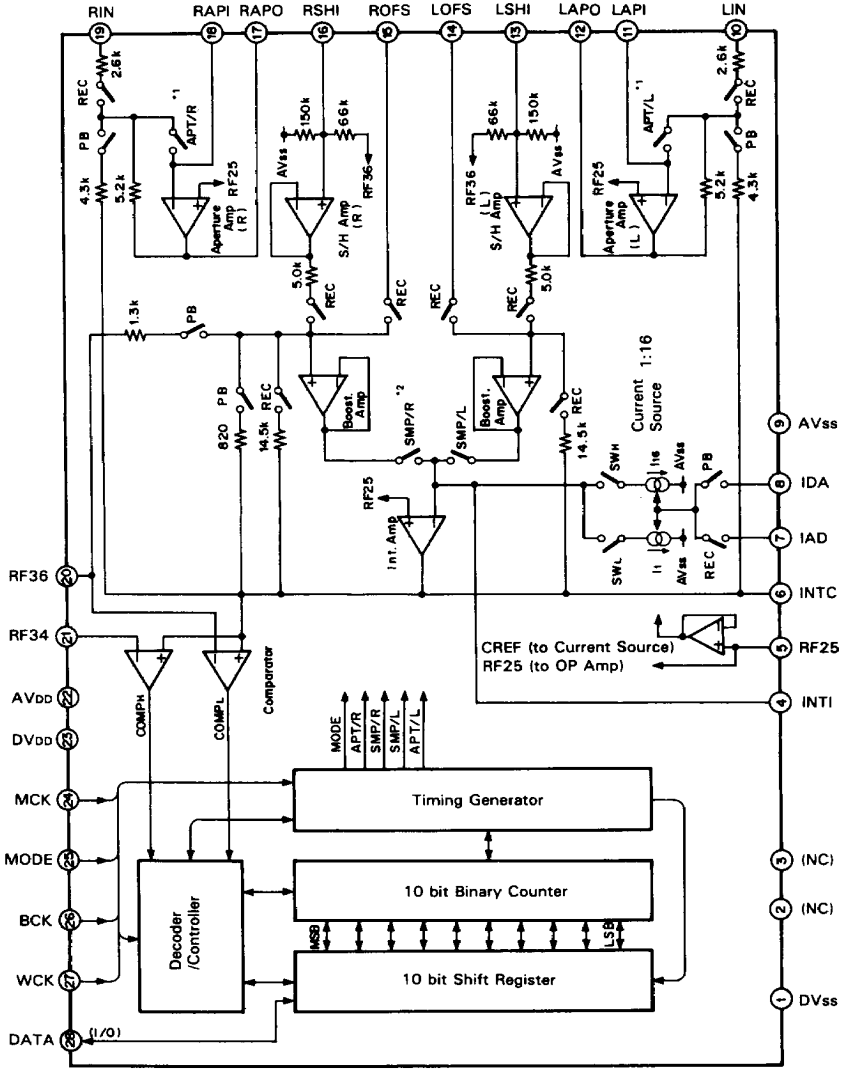
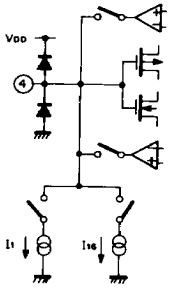
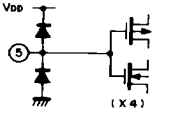
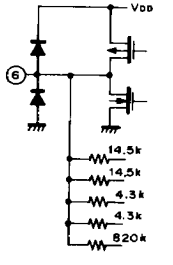
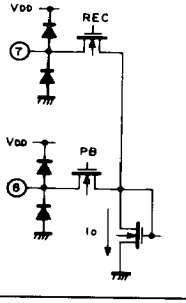
Block Diagram

*1. APT/L,R (REC mode) Ever on (PB mode) Aperture
*2. SMP/R Sampling Discharge



Pin Description

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
1	DVss	0V			Digital ground pin
2	NC				Non connection
3	NC				Non connection
4	INTI	2.5V	I		Amplifier input pin for integrator (common to L and R). Integrating capacitor is externally connected between this pin and 6 INTO. Connected to forestage buffer amplifiers (separately for L and R) and two constant current supplies via respective analog switches. I1: 5 µA in REC mode, 3 µA in PB mode I16: 80 µA in REC mode, 48 µA in PB mode
5	RF25	*2.5V	I		Virtual ground potential setting pin for four inverted operational amplifiers. Externally supplies DC2.5V. Requires external connection of coupling capacitor.
6	INTO		O		Amplifier output pin for integrator (common to L and R). Integrating capacitor is externally connected between this pin and 4 INTI. (This pin permits observation of integrated wave form.)
7 8	IAD IDA	1.6 to 2.2V 1.3 to 1.9V	I I		Integrating current setting pins: 7 IAD for REC mode, and 8 IDA for PB mode. Current Io proportional to integrating current can be provided by externally connecting resistors between these pins and external reference voltage 3.6V. Io: 3.6 µA in REC mode 2.1 µA in PB mode A coupling capacitor of about 1 µF is externally attached to each of 7 and 8.

*) External voltage

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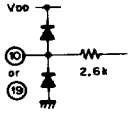
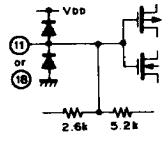
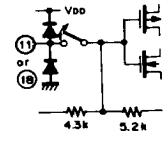
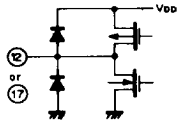
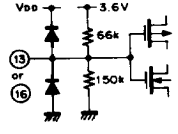
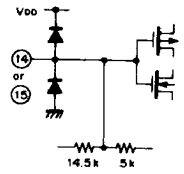
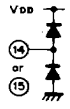
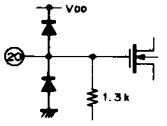
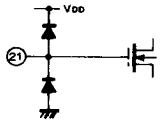
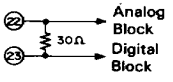
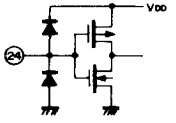
Pin Description

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
9	AVss				Analog ground pin.
10 19	L IN R IN		I I		Analog signal input pin (L, R). Appropriate full-scale input level is −10 dBs (0.693Vpp).
11 18	LAPI RAPI		I I	[REC mode]  [PB mode] 	Amplifier input pins (L, R) for aperture. Sample-hold circuit in PB mode (in the IC, the amplifier for sample & hold of PB is called "aperture amplifier," for the discrimination from the amplifier for sample & hold of REC "S/H amplifier") is configured by externally attaching a capacitor between 11 LAPI and 12 LAPO, or between 18 RAPI and 17 RAPO. The aperture amplifier serves as a simple input amplifier in REC mode, and Pins 11 and 18 make almost no sense.
12 17	LAPO RAPO		O O		Aperture amplifier (L, R) output pins. [In REC] Analog signal entered from 10 L IN and 19 R IN is amplified by about 6 dB and output from there. [In PB] Sample & hold wave form of DA conversion is output.
13 16	LSHI RSHI		I I		S/H Amplifier (Sample & Hold Amplifier: L, R) input pins. In REC, analog signal output from 12 LAPO or 17 RAPO passes through an externally connected low-pass filter and then is returned to IC from this pin. The value of AC level is substantially the same as that of 10 L IN and 19 R IN (−10 dBs full scale).

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
14 15	LOFS ROFS		I I	[REC mode]  [PB mode] 	Offset correction pins in REC (L, R). Offset in A/D conversion can be corrected by externally connecting a semi-fixed resistor between these pins and external reference voltage 3.6V and adjusting the DC level of these pins.
20	RF36	*3.6V	I		Pin for setting lower rank comparator comparison voltage in REC or discharge voltage in PB. Externally feeds DC3.6V. Requires external connection of a coupling capacitor.
21	RF34	*3.4V	I		Pin for setting upper rank comparator comparison voltage in REC. Externally feeds DC3.4V. Requires external connection of a coupling capacitor.
22 23	AVDD DVDD	*5V *5V			Analog power supply voltage pin and digital power supply pin. Externally supply DC5V. Requires external connection of a coupling capacitor.
24	MCK		I		Master clock input pin. (11.58 MHz). Only MCK is TTL-compatible.

*) External voltage

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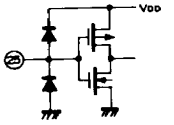
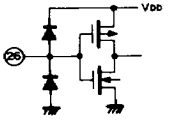
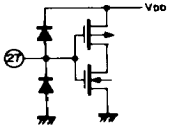
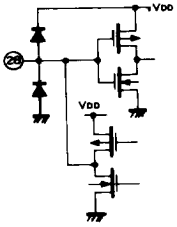
No.	Symbol	Voltage	I/O	Equivalent circuit	Description
25	MODE		I		REC mode/PB mode select input pin. "H" level: REC mode (A/D conversion) "L" level: PB mode (D/A conversion)
26	BCK		I		Bit clock input pin. Uses Pin 17 (BCK) output of CX23012 (CX23062) as shift clock for serial data.
27	WCK		I		Word clock input pin. (31.5 kHz) Used as an L/R channel identification signal of data, and "H" level: L channel data "L" level: R channel data in both REC (data output) and PB (data input). Uses output of Pin 18 (WCK) of CX23012 (CX23062) (in synchronization with the rise edge of BCK).
28	DATA		I/O		Data input/output pin. (2's complement) In REC: outputs 10-bit data in sync with the rise edge of BCK in the sequence of LSB, 2SB, ... MSB. In PB: inputs 10-bit data in sync with the fall edge of BCK in the sequence of LSB, 2SB, ..., MSB. L/R channels are alternately switched over in accordance with H/L of WCK.

Electrical Characteristics

Ta = 25°C Vpp = 5V (See Fig. 1 to 3)

Item		Symbol	Condition	Pin	Min.	Typ.	Max.	Unit
REC mode	Input impedance	Zin		10, 19		2.6		kΩ
	Full-scale input level	Vin		10, 19		−10		dBs
	Analog input gain	Gin	Aperture amplifier gain			6.0		dB
	Total harmonics distortion + noise	THD_1	Level = 1 dB, see Test method in 8-1.			0.10	0.14	%
		THD_2	Level = 6 dB, see Test method in 8-1.			0.18	0.20	%
PB mode	Total harmonics distortion + noise	THD_2	Level = 0 dB, see Test method in 8-2.			0.10	0.14	%
		THD_4	Level = 6 dB, see Test method in 8-2.			0.18	0.20	%
Power consumption		I_{DD}				24	36	mA

Test method of total harmonics distortion + noise in PB mode

The total harmonics distortion + noise characteristics (D/A conversion characteristics) in PB mode is measured by a method as shown in Fig. 1. Enter WCK and BCK generated by MCK (11.58 MHz) and CX23012 into CXD1077M, and at the same time, enter 0 dB (full-scale level) or −6 dB digital sine-wave data (1 kHz), and measure the total harmonics distortion + noise at this moment. Set −10 dBs (0.245 Vms) upon 0 dB input as the PB output level (interpolation filter output level) by adjusting the semi-fixed resistor 1 MΩ connected to the PB mode integrating current setting pin 8.

Test method of total harmonics distortion + noise in REC mode

The total harmonics distortion + noise characteristics (A/D conversion characteristics) in REC mode is measured by a method as shown in Fig. 2. Enter WCK and BCK generated by MCK (11.58 MHz) and CX23012 into CXD1077M, and at the same time, enter −11 dBs (full-scale level −1 dB) or −16 dBs (full-scale level −6 dB) sine-wave (1 kHz) as analog signal, and DA-convert the A/D-converted data with the reference playback DAC (provide another DAC previously adjusted so that a PB output level of −10 dBs is reached upon input of full-scale data, by the method described in the above). Make setting by adjusting the semi-fixed resistor 4.7Ω connected to S/H amplifier input Pins 13 and 16 so that the analog level becomes equal to the analog output level (interpolation filter output) of reference playback DAC (REC level adjustment). It is however necessary to previously adjust offset so that the wave form may not be clipped by the semi-fixed resistor 22Ω connected to the offset correction Pins 14 and 15, while observing the output wave form of the reference playback DAC when the input is near the full scale (offset adjustment is possible also by the method shown in the DC offset adjustment in REC on page 15).

After the completion of the adjustment as described above, measure the sum of total harmonics distortion + noise of analog output (interpolation filter output) of the reference playback DAC, and use the result as the REC mode conversion characteristics of the tested device.

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Electrical Characteristics Test Circuit
(For total harmonics distortion factor and noise characteristics in PB mode)

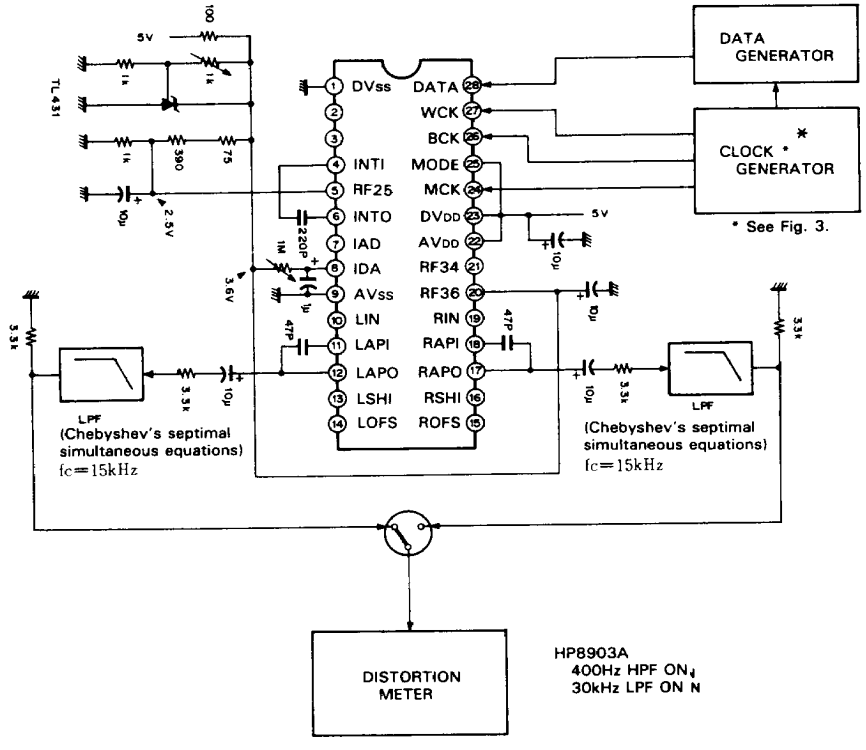
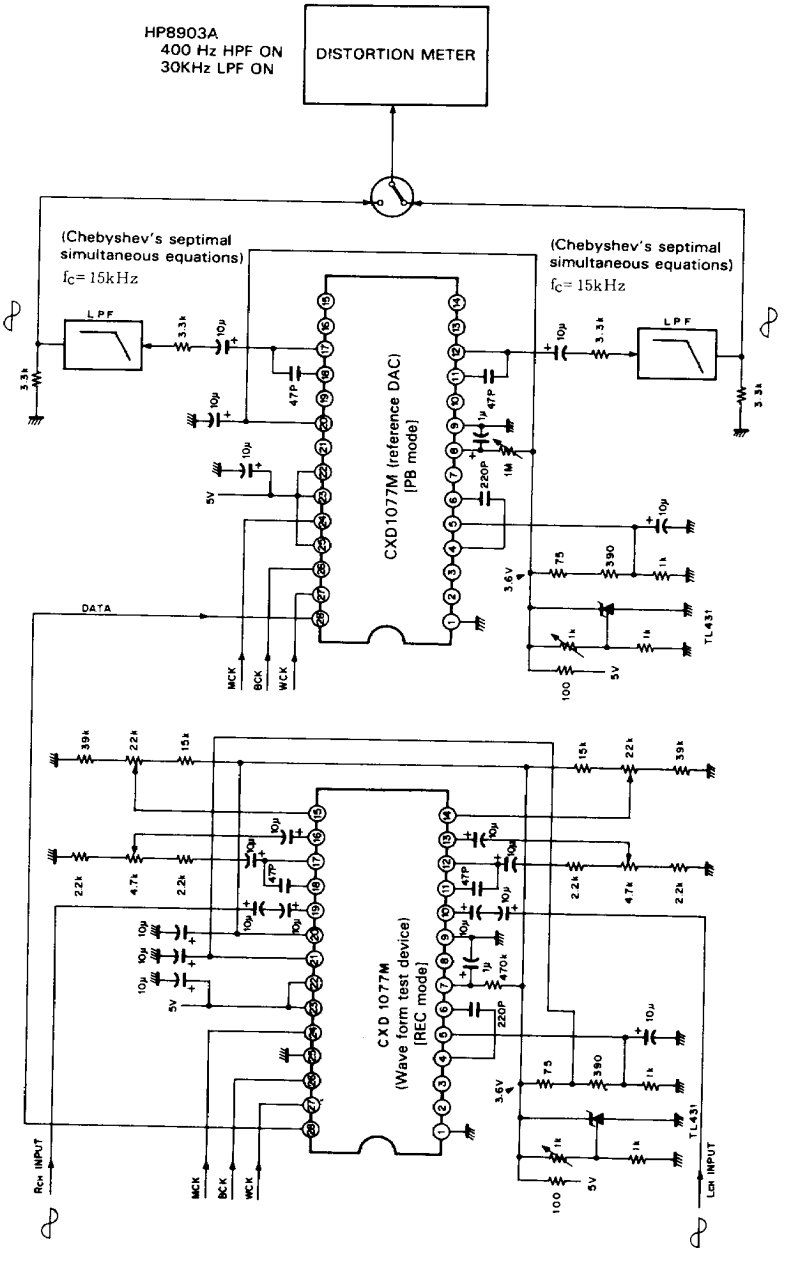


Fig. 1

Electrical Characteristics Test Circuit
(For total harmonics distortion factor and noise characteristics in REC mode)



Clock Generator Circuit
(For testing total harmonics distortion factor and noise characteristics)

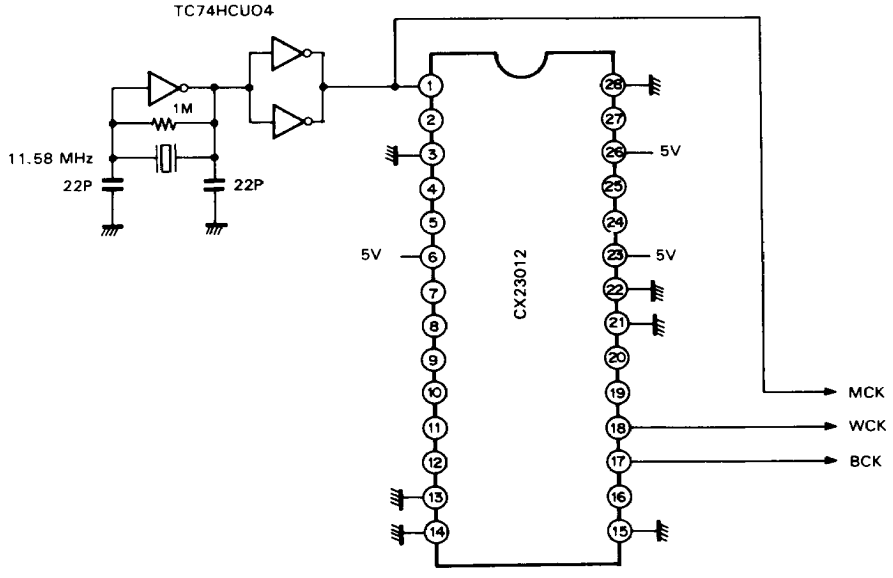


Fig. 3

Description of Function

The CXD1077M is a single-chip 10-bit A/D, D/A converter provided with every function required in A/D and D/A conversion. Particularly when combined with CX23011 (for modulation, demodulation and error correction), CX23012 (A/D, D/A interface) and CX20099 (analog noise reduction), it is used in the PCM processor for 8-mm video.

Description of REC mode function

1) Selection of operational mode
   REC mode (A/D conversion mode) is selected by setting the MODE signal to "L".
2) Analog block operation and gain
   The input signal applied to the analog signal input pins 10 and 19 is amplified by about 6 dB by the aperture amplifier and output to the aperture output pins 12 and 17. After component out of band area is removed from the output signal by the external attenuation filter, it is added to the sample-hold input pins 13 and 16 and output to the integrating output pin 6 after amplification by about 9.25 dB by the sample-hold amplifier.
   This gain is obtained assuming that the external filter's insertion loss is −6 dB. Therefore, the overall gain will be about 9.25 dB when the filter is included. Even when the external filter's insertion loss is different from the above value, or its insertion position is different, it is necessary to achieve an overall gain of about 9.25 dB. For details, refer to the REC level adjustment on page 16.

3) Digital block operation and clock (see Fig. 4: REC mode timing chart)
The Convert Command (C.C.) is generated internally by entering WCK and BCK. While C.C. is at "H", the analog signal applied to the S/H amplifier is sampled, and while C.C. is at "L", the constant current weighted with inverse polarity against the input signal is integrated by the integrating circuit for conversion. The 10-bit data is performed by calculating the integrating time of the coarse constant current and fine constant current separately using a counter. An MCK frequency of 11.58 MHz is used for 8-mm video as the counter clock frequency required when conducting full-scale A/D conversion. In the CXD1077M, it is necessary to maintain mutual synchronization of MCK, WCK and BCK because of the necessity of converting operation to be in synchronization with MCK, irrespective of the phase relationship of MCK with WCK or BCK. The data is loaded, on the other hand, in the shift register when C.C. becomes "H" again and is output serially with LSB leading in synchronization with the rise edge of BCK. The data is coded in 2's complement.

4) Integrating current in REC
The integrating current value $I_{A/D}$ required when performing a full-scale A/D conversion in the CXD1077M is obtained by the following equation:

$$I_{A/D} = \frac{C \cdot V_I}{1023 \tau_o}$$

where, C : Integration Capacitance
V_I : Integrator output voltage, and
τ_o : MCK cycle.

According to Fig. 6 representing an example of application circuit, C = 220pF, V_I = 2Vp-p' and τ_o = 86 ns (MCK frequency: 11.58 MHz), leading to an integrating current value of about 5 μA. The integrating current setting is done by applying an external constant current to the Rec mode integrating current setting pin 7 through a resistor from an external reference voltage (3.6V). Supposing a setting resistor value of 470 kΩ, the constant current applied to pin 7 has a value of about 3.6 μA (reference value), corresponding to an integrating current value of about 5 μA.

5) Comparison voltage and virtual ground voltage
Switching between the upper conversion and lower conversion is performed by the integrating output 6 surpassing the comparison voltages 20 RF36 and 21 RF34 in the next stage comparator. The integrating output based coarse constant current surpassing RF34 (about 3.4V) causes switching from the upper to lower conversion, and the integrating output based on fine constant current surpassing RF36 (about 3.6V) causes the lower conversion to end.
Since the CXD1077M operates with a single 5-V power supply, it is necessary to apply a virtual ground voltage of 2.5V to a non-inverted input of the internal operational amplifier. This voltage is applied to 5 RF25.

6) DC offset
As 8-mm video uses a non-linear quantization by 10-bit ≒ 8-bit compression/expansion, compatibility is affected when a DC offset component is included in the A/D conversion data in recording. When the analog signal input is so large as being close to the full-scale level, the A/D conversion data may be clipped on a single side of positive or negative. To correct this DC offset, the integrating output's center voltage must be shifted by applying an offset voltage to the offset correcting pins 14 and 15. As to details, refer to the DC offset adjustment in REC mode on page 15.

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Description of PB mode operation

1) Selection of operation mode
By setting the MODE signal to "H", the PB mode (D/A conversion mode) is selected.

2) Digital block operation and clock (refer to Fig. 5: PB mode timing chart)
DIS (Discharge clock) and APT (Aperture clock) are generated internally in the CXD1077M, by entering WCK and BCK. The serial data input with LSB leading is stored in the shift register in synchronization with the falling edge of BCK and set in the counter while DIS is "H". When DIS becomes "L", the counter starts counting, beginning from the value set in it, and at the same time, a constant current weighted corresponding to data is output. When the counter outputs the carry signal, the counting and constant current output stop. The counter clock frequency required when performing a full-scale D/A conversion is 11.58 MHz (MCK frequency) for 8-mm video.

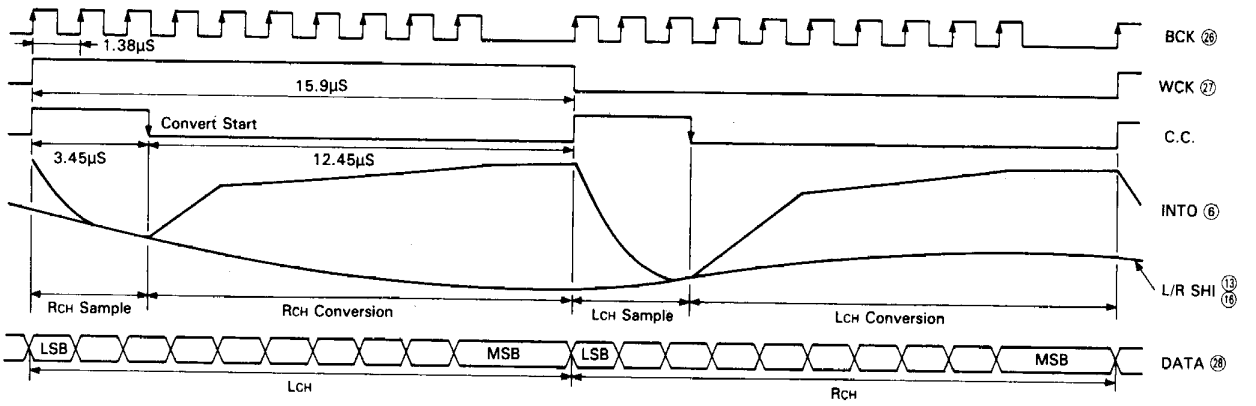
3) Analog block operation and gain
The integrating charge resulting from the previous conversion is discharged while DIS is "H" by sampling the external reference voltage 3.6V applied to 20 RF36 by means of the integrator. As a result, the integrating output in the discharge region is initialized to about 1.8V, and the output center voltage in input of sine-wave data becomes about 2.5V. When DIS goes to "L", D/A conversion operation is executed by integrating the constant current output. When the constant current output stops, integrating also stops, and the pin voltage held in the integrated capacitor at this moment takes the D/A converted value. This pin voltage is output, after being amplified by about 1.6 dB by the aperture amplifier, to the aperture output pins 12 and 17. Output signal's out-of-band components are removed by an external interpolation filter.

4) PB integrating current
Integrating current $I_{D/A}$ required when performing full-scale D/A conversion in the CXD1077M is determined from the following equation:

$$I_{D/A} = \frac{C \cdot V_I}{1023 \tau_o}$$

According to Fig. 6 representing an example of application circuit, C = 220pF, V_I = 1.2Vp-p' and τ_o = 86 ns, leading to an integrating current value of about 3μA. The integrating current setting is one by applying an external constant current to the playback mode integrating current setting pin 8 through a resistor from an external reference voltage (3.6V). Supposing a setting resistor value of 910 kΩ, the constant current applied to pin 8 has a value of about 2.1 μA (reference value), corresponding to an integrating current value of about 3 μA. It is possible to adjust the D/A conversion output level by altering this setting resistor. For details, refer to the PB level adjustment on page 15.

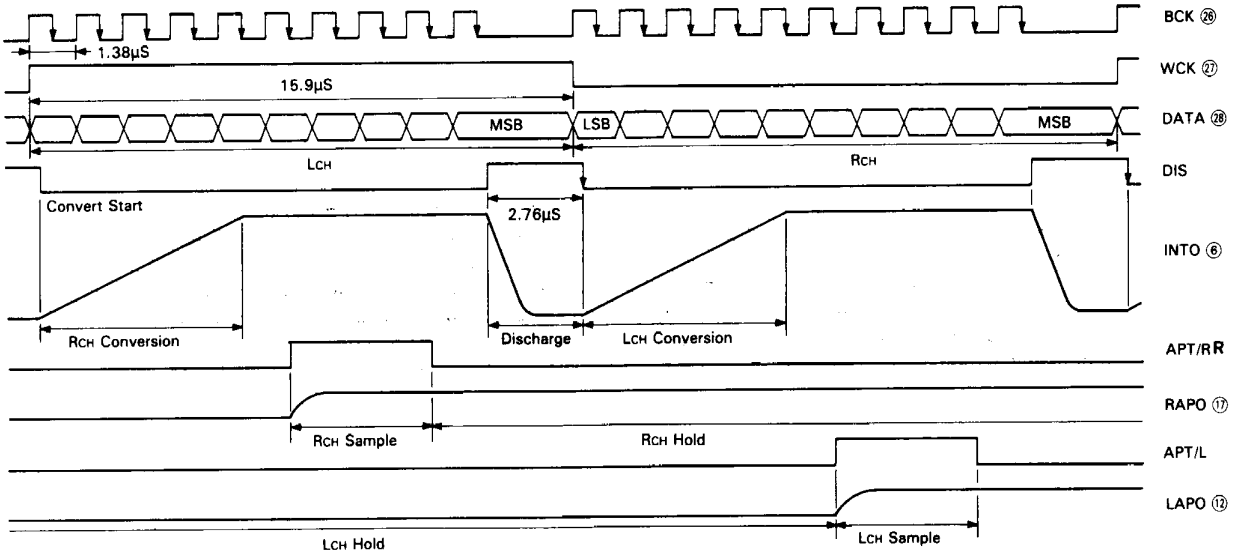
Timing Chart of REC Mode



When the MODE signal (pin 25) of the CXD1077M is set to "L", REC mode (A/D conversion mode) is selected. When BCK and WCK are entered from CX23012 (AD/DA interface LSI) in this mode, C.C. (Convert Command) is generated internally in the CXD1077M. While this C.C. is at "H" level, the analog signal input is sampled; A/D conversion is executed during "L" level. The sampling and conversion operations are performed in time division for each of the R and L channel analog signals. The converted final data is output serially with the LSB data leading in synchronization with the rise edge of BCK when the C.C. becomes "H" level again.

Fig. 4

Timing Chart of PB Mode



When the MODE signal (pin 25) of the CXD1077M is set to "H", PB mode (D/A conversion mode) is selected. When BCK and WCK are entered from CX23012 (A/D, D/A interface LSI) in this mode, DIS (Discharge clock) and APT R/L (Aperture clock) are generated internally in the CXD1077M. At the same time, the serial data input with the LSB leading is stored in synchronization with the fall edge of BCK. After DIS has discharged at "H" level, the integrating charge resulting from the previous D/A conversion, D/A conversion starts when DIS goes to "L" level. The discharge and conversion operations are performed in time division for each of the R and L channel data inputs. The final integrated output after conversion is sampled while APT R/L is at "H" and held at "L" level.

Fig. 5

Notes for Application and Adjustment Methods

(see Fig. 6. Application circuit)

As the conversion accuracy obtained is affected by the accuracy of parts used and adjustment in the CXD1077M, attention should be given to the following points:

Selection of parts to be used

1) For the integrating capacitor between pins 4 and 6, use a type with little dielectric absorption (e.g. styrol capacitor).
2) Adjust the semi-fixed resistor 1 kΩ so that the reference voltage generated from the reference voltage IC (TI's TL431) is 3.6V.
3) For the low-pass filters to be inserted between pins 12 and 13 and between pins 16 and 17, use passive-type ones with an input/output impedance of 3.3 kΩ, respectively.
4) Accuracy tolerance of the three divided resistors, 75 Ω, 390 Ω, and 1 kΩ, supplying voltage to pins 5 and 21 is 5%.

PB level adjustment

In adjustment of the PB level during D/A conversion, use a 470 kΩ semi-fixed resistor connected to pin 8. Input to pin 28 a full-scale level digital sine-wave data (1 kHz), and adjust the semi-fixed resistor so that the PB level (interpolation filter output level) becomes −10 dBs (0.245 Vrms).

REC level adjustment

Adjustment of REC level during A/D conversion can be accomplished by the use of a 470 kΩ semi-fixed resistor connected to pin 7 as well, in addition to the method described in 8-2 above. Apply a −16 dBs (−6 dB of full-scale level) sine wave (1 kHz) to pins 10 and 19 as the analog input signal, and conduct D/A conversion of the A/D-converted data by means of a reference playback DAC (prepare another DAC adjusted previously by the method mentioned in the PB level adjustment above so that the playback output level becomes −10 dBs when entering full-scale data). Adjust the semi-fixed resistor so that the reference playback DAC output level becomes equal to the analog signal input level (−16 dBs) to the tested A/D converter.

DC offset adjustment in REC

In the offset adjustment of A/D-converted data during A/D conversion, use a 22 kΩ semi-fixed resistor connected to pins 14 and 15. In practice, adjust the semi-fixed resistor so that the data output of pin 28 becomes "0000000000" when DC2.5V is applied as the analog input level of pins 10 and 19. In this adjustment, do not fail to conduct offset adjustment only after the completion of REC level adjustment as described in the REC level adjustment above.

Frequency characteristics

The CXD1077M frequency characteristics in REC is determined by an input attenuation filter. Meanwhile the frequency characteristics in PB is determined by the aperture effect and output interpolation filter. With the CXD1077M, degradation of high area frequency characteristics caused by the aperture effect is unavoidable. This is because a sample-hold aperture circuit is used to obtain −10 dBs as the interpolation filter output level during full-scale D/A conversion. To compensate the degraded characteristics, add a compensation filter, as shown in Fig. 7, with inverted response characteristics.

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Application Circuit

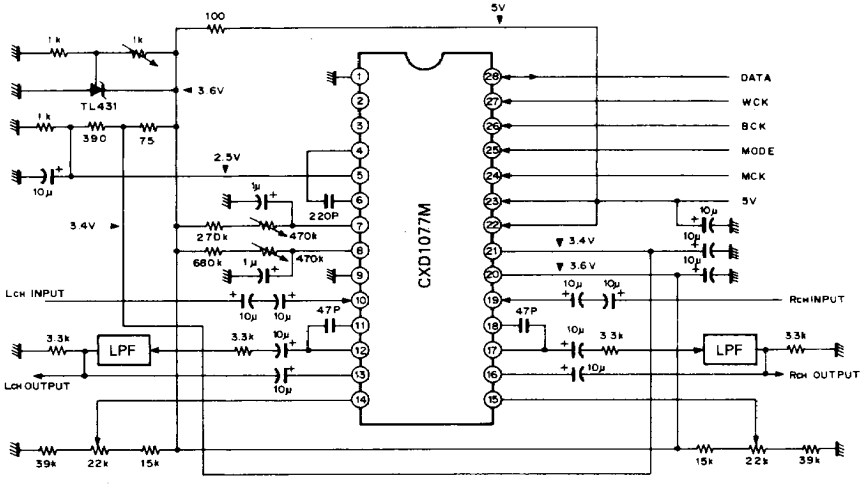


Fig. 6

Compensation characteristics of aperture effect

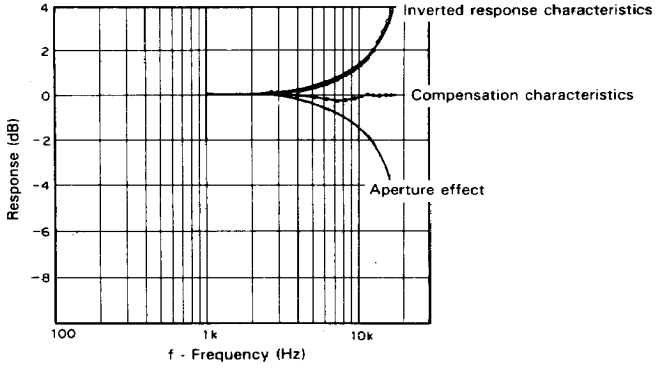
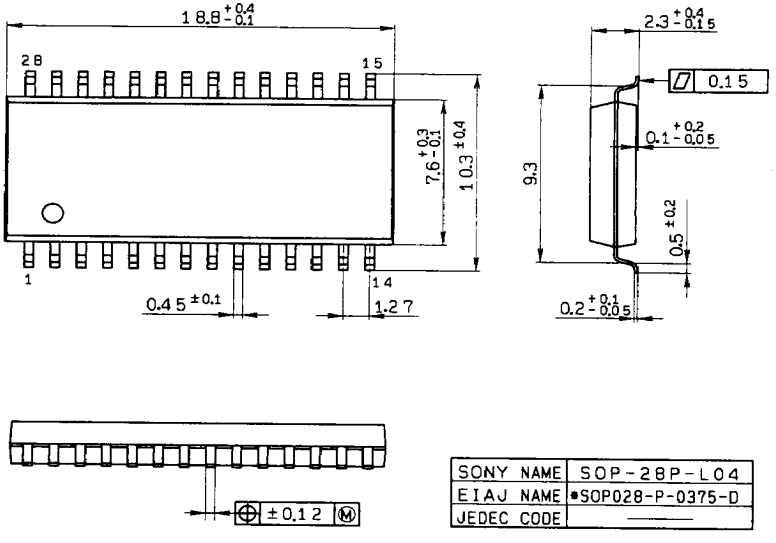


Fig.7

Package Outline Unit : mm

28 pin SOP (Plastic) 375mil 0.7g



SONY NAME	SOP-28P-L04
EIAJ NAME	*SOP028-P-0375-D
JEDEC CODE	———

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