SONY

CXD1158M

Synchronizing Signal Generator for Consumer Video Camera

Description

CXD1158M is a synchronizing signal generator for video camera.

Features

- Adapts to NTSC or PAL by switching mode
- Low power consumption
- Built-in phase comparator and inverter for active filter (separate power supply for the filter inverter)
- External sync

Structure

Silicon gate CMOS IC

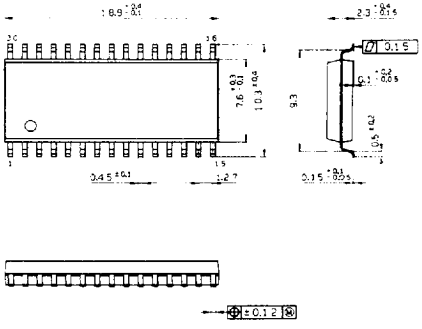
Application

Consumer video camera

Package Outline

Unit: mm

30 pin SOP (Plastic)



SOP-30P-L01

Absolute Maximum Ratings (Ta = 25°C)

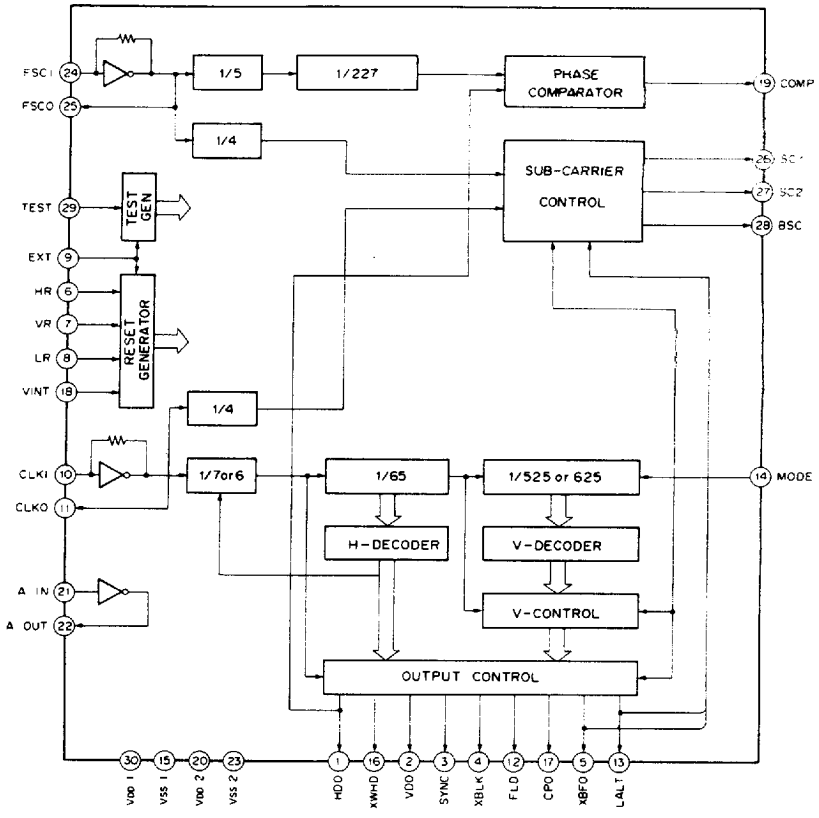
• Supply voltage	V_{DD}	V_{SS}*1	−0.3 to +7.0	V
• Input voltage	V_I	V_{SS}*1	−0.3 to V_{DD} + 0.3*2	V
• Output voltage	V_O	V_{SS}*1	−0.3 to V_{DD} + 0.3*2	V
• Operating temperature	Topr		−20 to +75	°C
• Storage temperature	Tstg		−55 to +150	°C

Note) *1. V_{SS} = 0V
*2. Normal value, Transient value 0.5V (20 to 30 ns)

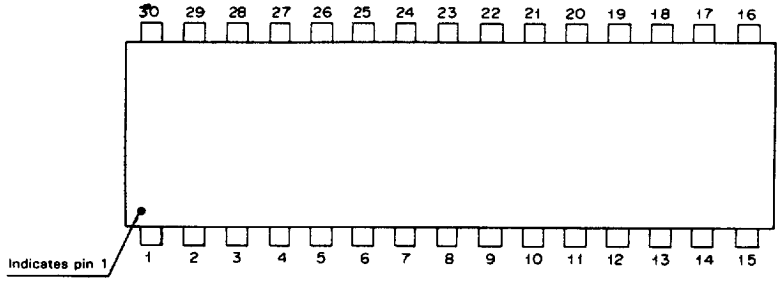
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	−20 to +75	°C

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	HDO	O	Horizontal drive pulse
2	VDO	O	Vertical drive pulse
3	SYNC	O	Composite sync. pulse
4	XBLK	O	Composite blanking pulse
5	XBFO	O	Burst•flag pulse
6	HR	I	H reset input
7	VR	I	V reset input
8	LR	I	LALT reset input
9	EXT	I	INT/EXT mode switching
10	CLKI	I	Clock input
11	CLKO	O	Clock output
12	FLD	O	Field pulse
13	LALT	O	Line alternate pulse
14	MODE	I	NTSC/PAL mode switching NTSC/PAL
15	$V_{SS}1$	—	GND
16	XWHD	O	Wide Horizontal drive pulse
17	CPO	O	Clamp pulse
18	VINT	I	Initialize input
19	COMP	O	Phase comparator output
20	$V_{DD}2$	—	Inverter +5V for filter
21	AIN	I	Inverter input for filter
22	AOUT	O	Inverter output for filter
23	$V_{SS}2$	—	Inverter GND for filter
24	FSCI	I	Clock input 4 f_{sc}
25	FSCO	O	Clock output 4 f_{sc}
26	SC1	O	Sub carrier 1
27	SC2	O	Sub carrier 2
28	BSC	O	Bursted sub carrier
29	TEST	I	Test input (Normally L)
30	$V_{DD}1$	—	+5V

Electrical Characteristics

DC characteristics

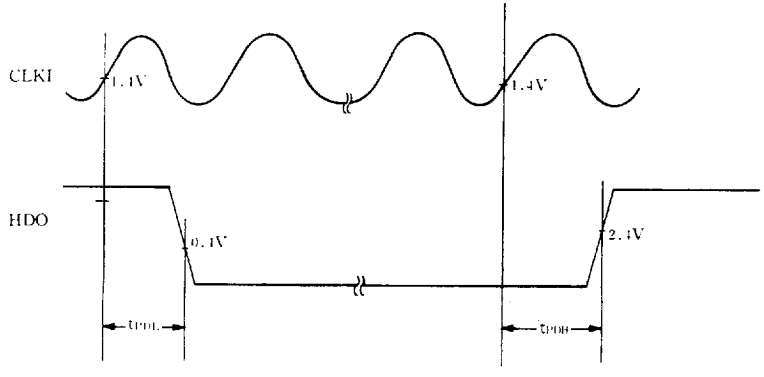
$V_{DD} = 5V \pm 10\%$ $V_{SS} = 0V$ $T_{op} = -20$ to $+75°C$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}			2.0		mA
		I_{DDS}	Static state*1	0		0.1	mA
Output voltage I*2	H level	V_{OH}	$I_{OH} = -2mA$	$V_{DD} - 0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 4mA$	V_{SS}		0.4	V
Output voltage II*3	H level	V_{OH}	$I_{OH} = -1.5mA$	2.5		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 1.5mA$	V_{SS}		2.5	V
Input voltage	H level	V_{IH}		0.7 V_{DD}			V
	Level	V_{IL}				0.3 V_{DD}	V
Input leak current		I_{LI}	$V_I = 0V$ to V_{DD}	−10		10	μA
Output leak current*4		I_{OZ}		−10		10	μA

*1. $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
*2. Output pins except "A OUT"
*3. "A OUT" pin
*4. Tri-state pin 19

AC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
H to L Propagation delay time	t_{PDL}	$V_{OL} = 0.4V$			45	ns
L to H Propagation delay time	t_{PDH}	$V_{OH} = 2.4V$			45	ns



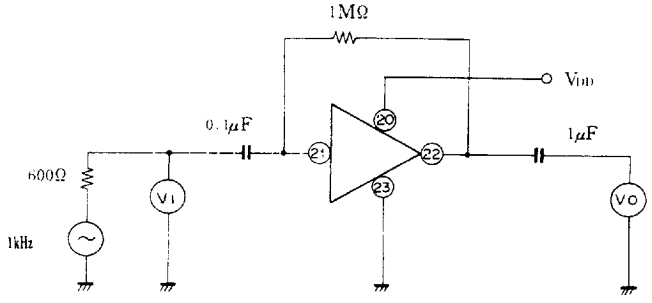
I/O capacitance

$V_{DD}V_I = 0V$, $f_M = 1MHz$

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

Filter Amplifier Characteristics

Voltage gain Gv: 25dB (Typ.)



Test circuit

Description of Function

Generation of various synchronizing signals (See the Timing Chart).

Generates various synchronizing signals from Clock.

- Clock frequency:

NTSC: 910 fH (14.31818 MHz)

PAL: 908 fH (14.1875 MHz)

4 fSC (17.734475 MHz)

PLL for PAL 4 fSC

Matches 4 fSC phase, with 908 fH as Master clock.

An active filter is used as filter.

908 fH	4 fSC	COMP
Forward	Back	L
Back	Forward	H

Generation of SC (Sub-Carrier)

Generates three kinds of sub-carrier.

SC1, SC2 and BBC. (Refer to the Timing Chart for phase.)

Mode	Sync.	Sub-carrier (SC)
NTSC	INT	910 fH/4
NTSC	EXT	No output
PAL	INT or EXT	4 fSC/4

INT: INTERNAL mode (EXT = L)

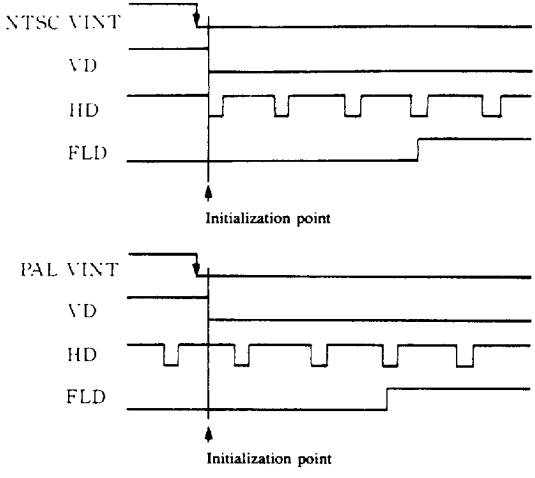
EXT: EXTERNAL mode (EXT = H)

Any unused counter is stopped in any mode.

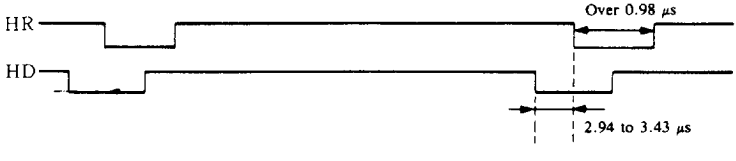
Initialize and Reset

In the INT mode, the circuit is initialized at falling edge of VINT. H reset, V reset and LALT reset are not accepted in this mode. In the EXT mode, in contrast, VINT is not accepted, while H reset, V reset and LALT reset are accepted.

- Initialize (VINT)
  Detection of VINT's falling edge causes, at the first clock, initialization at the position of falling edge of VD immediately before the ODD (1st) field to start operation. (Initialization is completed within 100 ns from the detection of falling edge.)

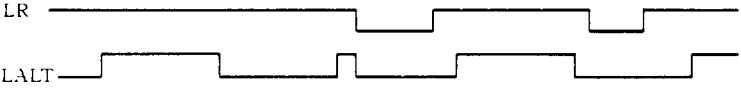


- H reset (HR)
  It is reset at the first falling edge, and not reset unless there is an offset of over 2 clocks (0.98 μs) for the next and subsequent edges. The minimum pulse duration is 0.98 μs.
  The position of reset is at 2.94 to 3.43 μs forward from HR input.



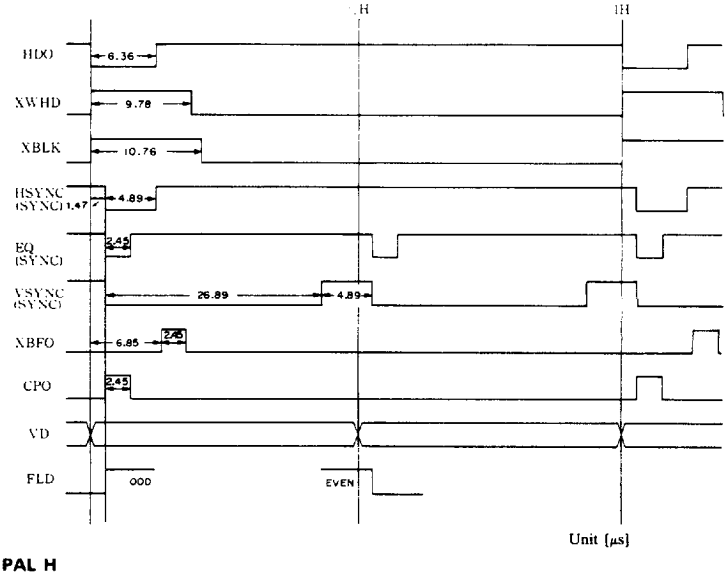
- V reset (VR)
  It is reset at a position of VD at 3.5 H forward from VR. The minimum reset pulse duration is 32 μs.

- LALT reset (LR)
  LALT is reset to the same phase as that of LR input. The minimum reset pulse duration is 32 μs.

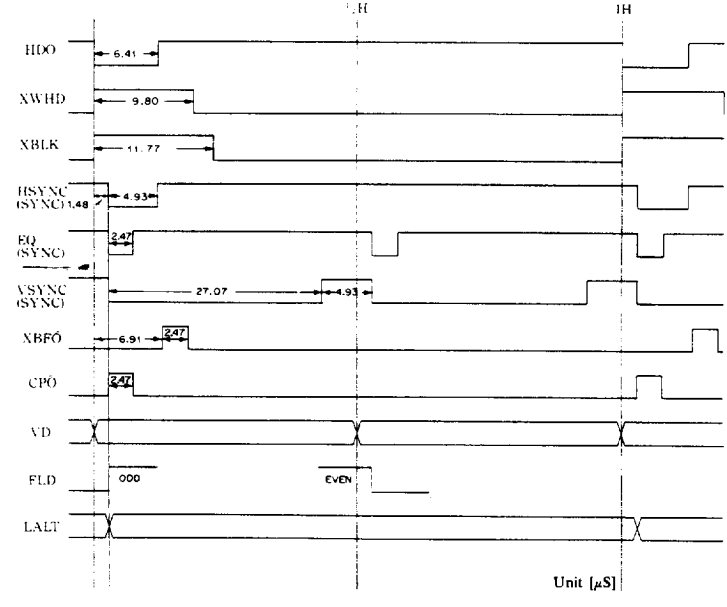


Timing Chart

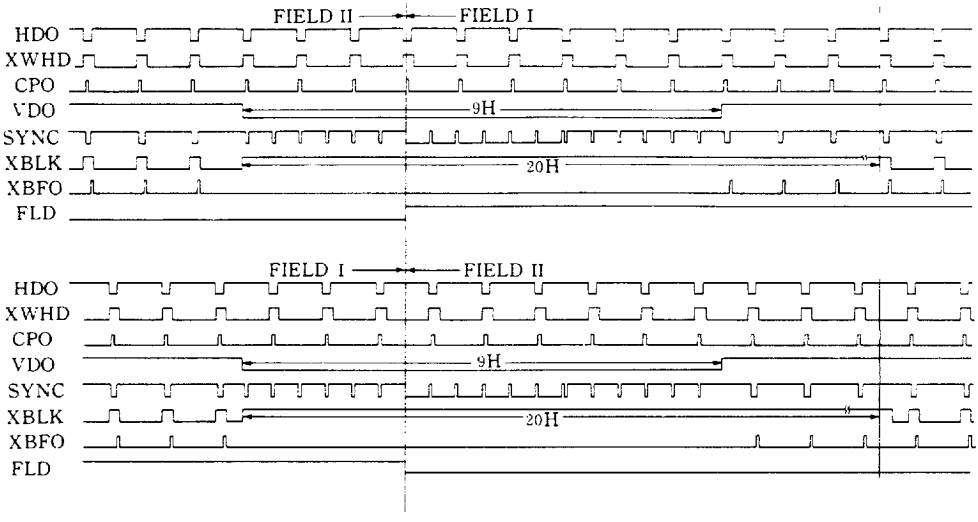
NTSC H



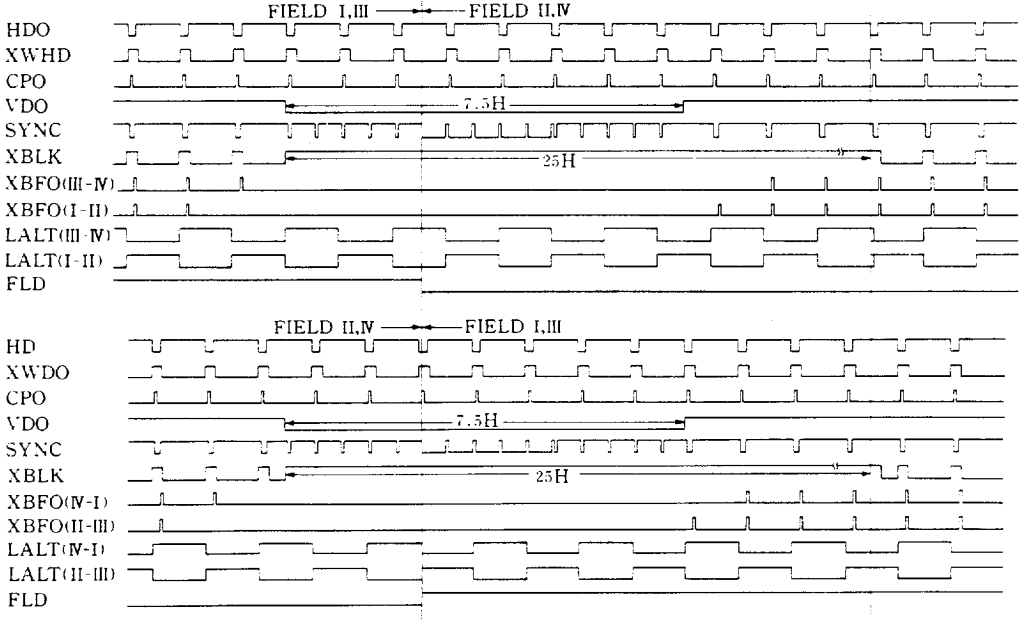
PAL H



NTSC V

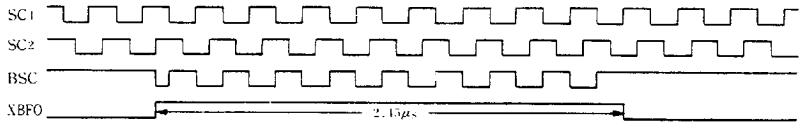

FIELD II
FIELD I
HDO
XWHD
CPO
VDO
SYNC
XBLK
XBFO
FLD
9H
20H
FIELD I
FIELD II
HDO
XWHD
CPO
VDO
SYNC
XBLK
XBFO
FLD
9H
20H

PAL V


FIELD I,III
FIELD II,IV
HDO
XWHD
CPO
VDO
SYNC
XBLK
XBFO(III-IV)
XBFO(I-II)
LALT(III-IV)
LALT(I-II)
FLD
7.5H
25H
FIELD II,IV
FIELD I,III
HD
XWDO
CPO
VDO
SYNC
XBLK
XBFO(IV-I)
XBFO(II-III)
LALT(IV-I)
LALT(II-III)
FLD
7.5H
25H

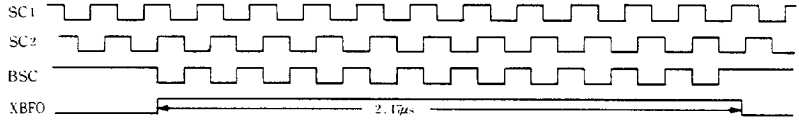
Sub Carrier

NTSC

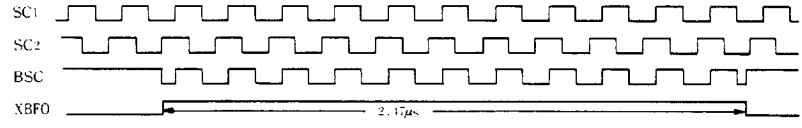


PAL

LALT=H

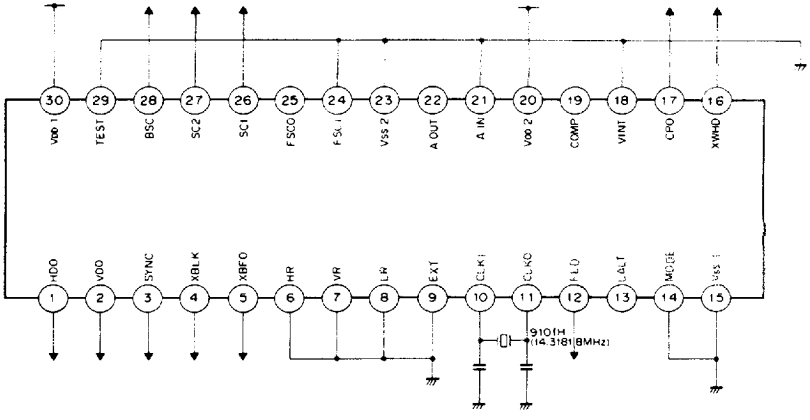


LALT=L



Application Circuit

NTSC (Internal mode)



PAL (Internal mode)