SONY®

CXD1175M/P

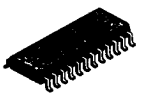
8-bit 20 MSPS Video A/D Converter (CMOS)

Evaluation Board Available — CXD1175P/CXA1106P PCB

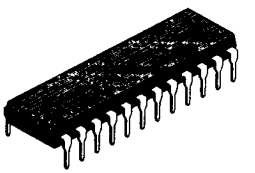
Description

CXD1175 is an 8-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 20 MSPS.

CXD1175M 24pin SOP (Plastic)



CXD1175P 24pin DIP (Plastic)



Features

- Resolution ..... 8-bit ± 1/2 LSB (DL)
- Max. sampling frequency .... 20 MSPS
- Low power consumption .... 90 mW (at 20 MSPS Typ.) (Reference current excluded)
- Built-in sampling and hold circuit.
- Built-in reference voltage self bias circuit.
- 3-state TTL compatible output.
- Power supply ..... 5V single
- Low input capacitance ..... 16 pF
- Reference impedance ..... 270Ω (Typ.)

Structure

Silicon gate CMOS monolithic IC

Applications

- TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

Absolute Maximum Ratings (Ta=25°C)

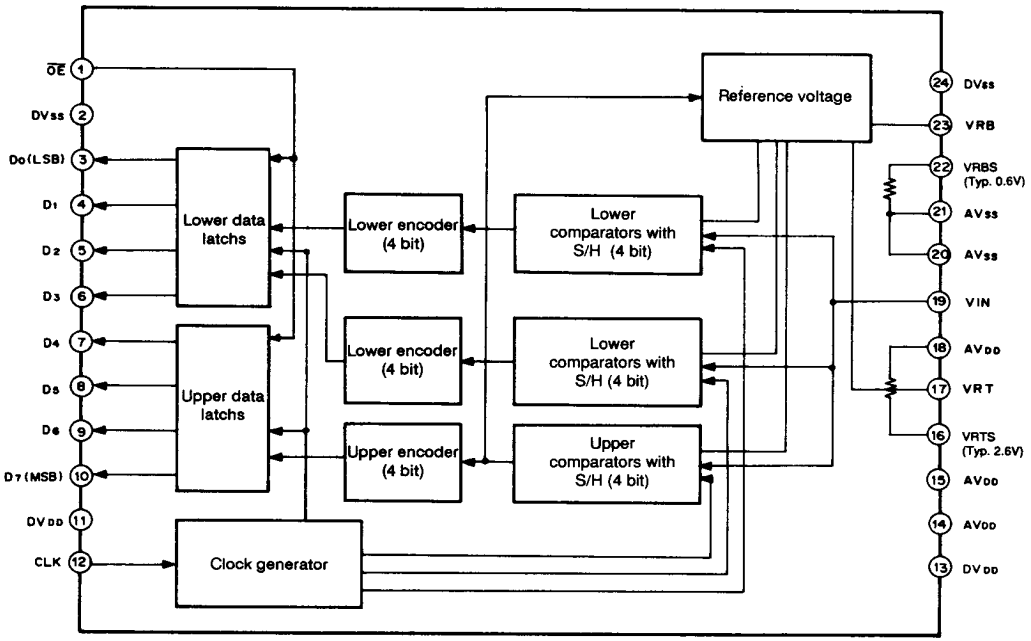
• Supply voltage	V_{DD}		7		V
• Reference voltage	V_{RT}, V_{RB}	V_{DD}	to	V_{SS}	V
• Analog input voltage	V_{IN}	V_{DD}	to	V_{SS}	V
• Digital input voltage	CLK	V_{DD}	to	V_{SS}	V
• Digital output voltage	V_{OH}, V_{OL}	V_{DD}	to	V_{SS}	V
• Storage temperature	Tstg	−55	to	+150	°C

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25		V
	DV_{DD}, DV_{SS}			
	|DGND-AGND|	0 to 100		mV
• Reference input voltage	V_{RB}, V_{RT}	$0 \leqq V_{RB} < V_{RT} \leqq 2.7$		V
	V_{RT}-V_{RB}	1.8 to AV_{DD}		V
• Analog input voltage	V_{IN}	V_{RB} to V_{RT}	(1.8Vp-p to AV_{DD}Vp-p)	
• Clock pulse width	T_{PWI}	25 (Min.)		ns
	T_{PWO}	25 (Min.)		ns
• Operating temperature	Topr	−20 to +75		°C

E89673-YA

Block Diagram and Pin Configuration

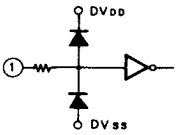
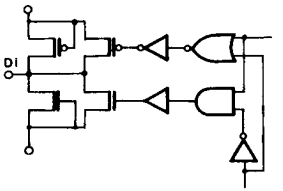
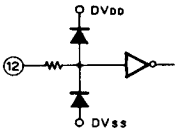
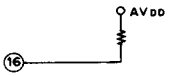
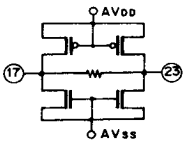
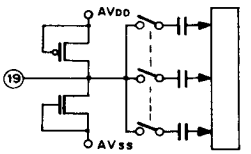
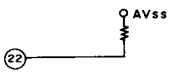


Digital Output

Compatibility between Analog input voltage and the digital output code is indicated in the chart below.

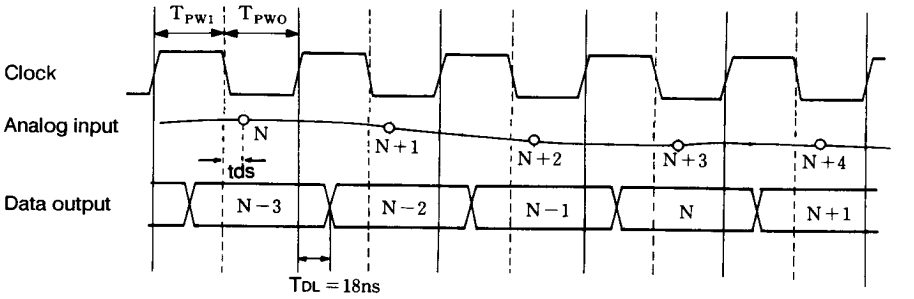
Input signal voltage	Step	Digital output code MSB							LSB
V_{RT}	0	1	1	1	1	1	1	1	1
	⋮					⋮			
	127	1	0	0	0	0	0	0	0
	128	0	1	1	1	1	1	1	1
	⋮					⋮			
V_{RB}	255	0	0	0	0	0	0	0	0

Pin Description and Equivalent Circuits

No.	Symbol	Equivalent Circuit	Description
1	$\overline{OE}$		When $\overline{OE}$ = Low, Data is output. When $\overline{OE}$ = High, D_0 to D_7 pins turn to High impedance.
2, 24	DVSS		Digital GND
3 to 10	D_0 to D_7		D_0 (LSB) to D_7 (MSB) output
11, 13	DVDD		Digital +5V
12	CLK		Clock input
16	VRTS		Shorted with VRT generates, +2.6V.
17	VRT		Reference voltage (Top)
23	VRB		Reference voltage (Bottom)
14, 15, 18	AVDD		Analog +5V
19	V_{IN}		Analog input
20, 21	AVSS		Analog GND
22	VRBS		Shorted with VRB generates +0.6V.

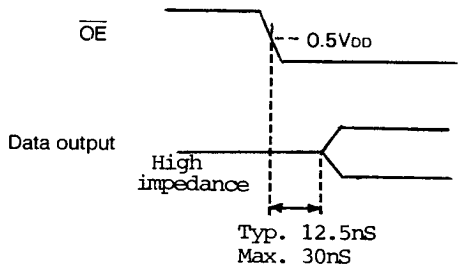
Timing Chart 1

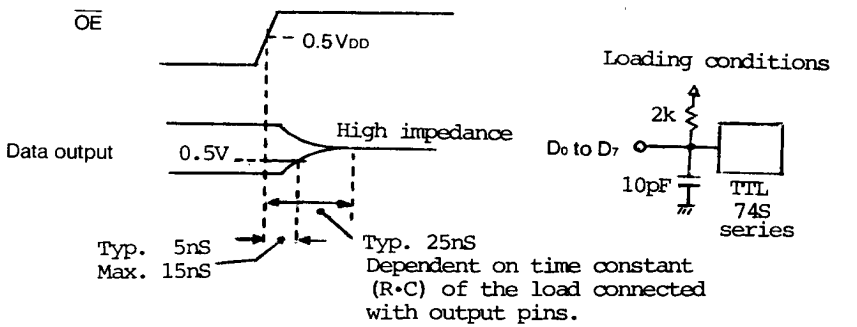
1. Without $\overline{OE}$



o: Point for analog signal sampling.

2. With $\overline{OE}$





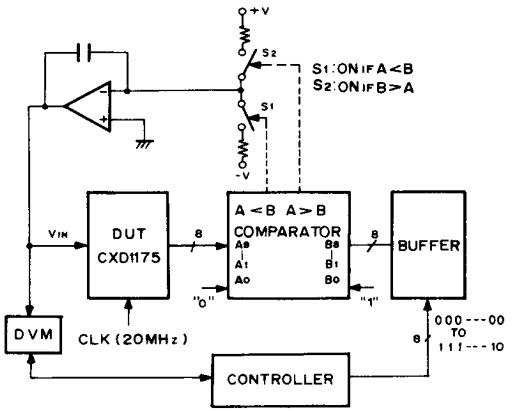
Electrical Characteristics

F_C = 20MSPS, V_{DD} = +5V, V_{RB} = 0.6V, V_{RT} = 2.6V, Ta = 25°C

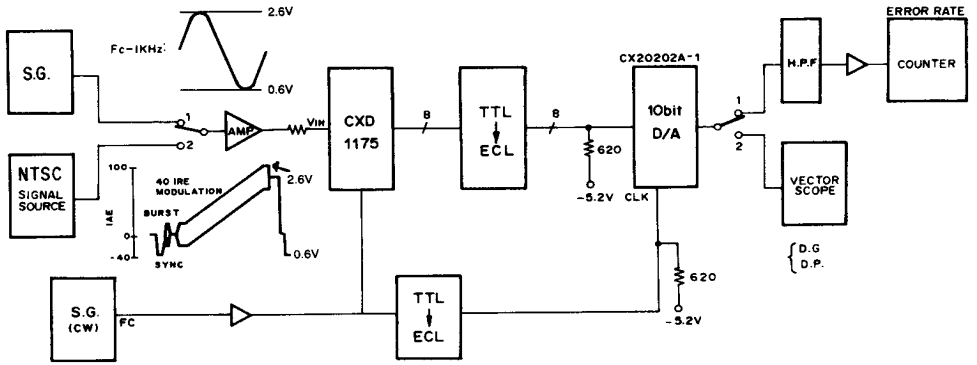
Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Maximum conversion speed	F_C	V_{IN} = 0.6V to 2.6V F_{IN} = 1 kHz ramp		20	25		MSPS
Supply current	I_{DD}	F_C = 20 MSPS NTSC ramp wave input			18	27	mA
Reference pin current	I_{REF}			5.2	7.5	10.5	mA
Analog input band (−1dB)	BW				14		MHz
Analog input capacitance	C_{IN}	V_{IN} = 1.5V + 0.07 Vrms			16		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}			190	270	350	Ω
Self bias 1	V_{RB1}	Short V_{RB} and V_{RBS}		0.57	0.6	0.65	V
	$V_{RT1} - V_{RB1}$	Short V_{RT} and V_{RTS}		1.90	2.0	2.15	
Self bias 2	V_{RT2}	VRB = AGND Short V_{RT} and V_{RTS}		2.2	2.3	2.40	V
Offset voltage	E_{OT}			−18	−43	−68	mV
	E_{OB}			0	+20	+45	
Digital input voltage	V_{IH}			4.0			V
	V_{IL}					1.0	
Digital input current	I_{IH}	V_{DD} = max.	$V_{IH} = V_{DD}$			5	µA
	I_{IL}		V_{IL} = 0V			5	
Digital output current	I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = min.	$V_{OH} = V_{DD} - 0.5V$	−1.5			mA
	I_{OL}		V_{OL} = 0.4V	4.0			
Digital output current	I_{OZH}	$\overline{OE}$= V_{DD}, V_{DD} = max.	$V_{OH} = V_{DD}$			16	µA
	I_{OZL}		V_{OL} = 0V			16	
Output data delay	T_{DL}				18	30	ns
Integral non-linearity	E_L	F_C = 20 MSPS V_{IN} = 0.6V to 2.6V			+0.7	+1.5 −1.0	LSB
Differential non-linearity	E_D	F_C = 20 MSPS V_{IN} = 0.6V to 2.6V		0	±0.3	±0.5	LSB
Differential gain error	DG	NTSC 40 IRE mod ramp, F_C = 14.3 MSPS			1.0		%
Differential phase error	DP				0.7		deg
Aperture jitter	taj				30		ps
Sampling delay	tds				4		ns

Electrical Characteristics Test Circuit

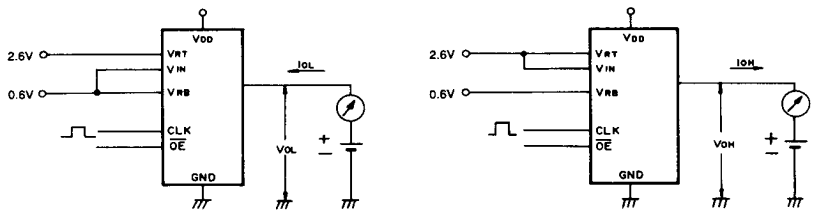
Integral non-linearity error
Differential non-linearity error
Offset voltage
} Test circuit



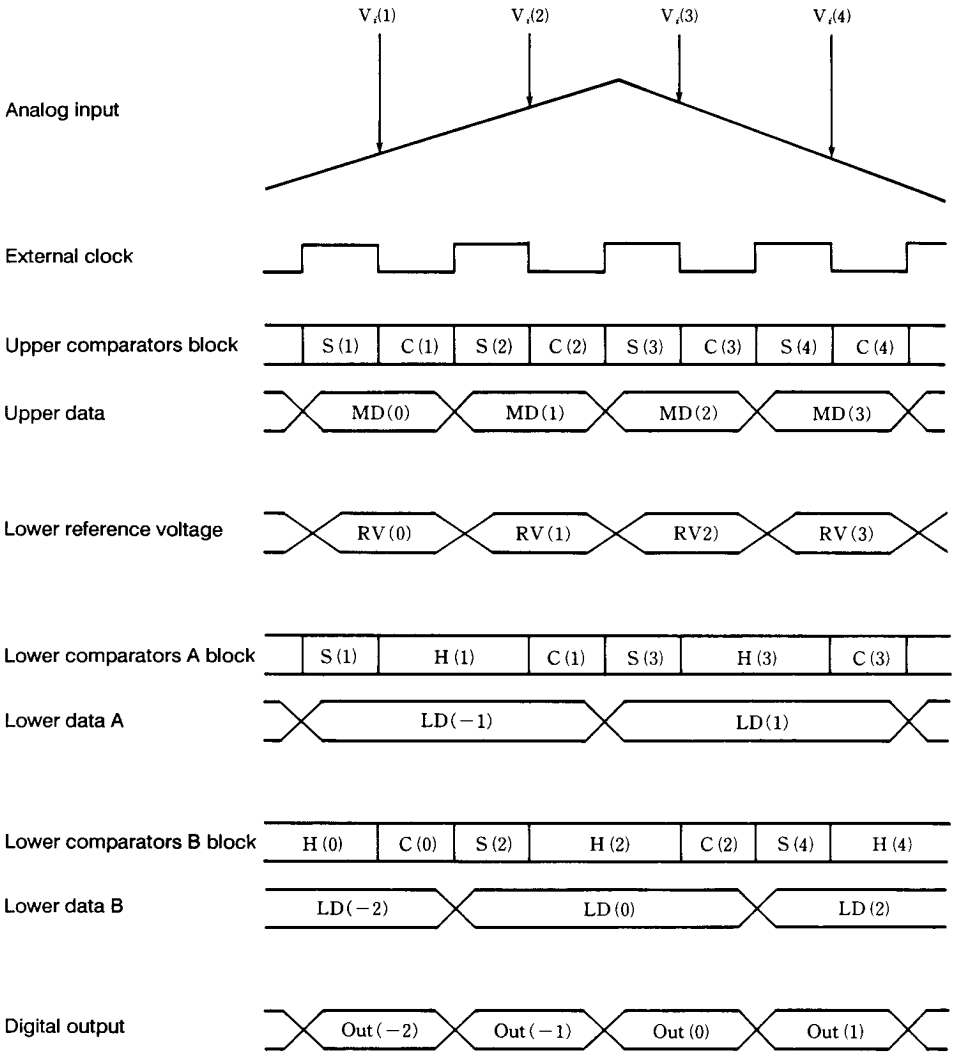
Maximum operational speed
Differential gain error
Differential phase error
} Test circuit



Digital output current test circuit



Timing Chart 2



Operation (See Block Diagram and Timing Chart)

1. CXD1175P/M is a 2-step parallel system A/D converter featuring a 4-bit upper comparators group and 2 lower comparators groups of 4-bit each. The reference voltage that is equal to the voltage between VRT-VRB/16 is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data. VRTS and VRBS pins serve for the self generation of VRT (Reference voltage top) and VRB (Reference voltage bottom).

2. This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.

3. The operation of respective parts is as indicated in the chart. For instance input voltage Vi (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.
   The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Operation Notes

1. V_{DD}, V_{SS}
   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1μF set as close as possible to the pin to bypass to the respective GND's.

2. Analog input
   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100Ω in series between the amplifier output and A/D input.

3. Clock input
   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

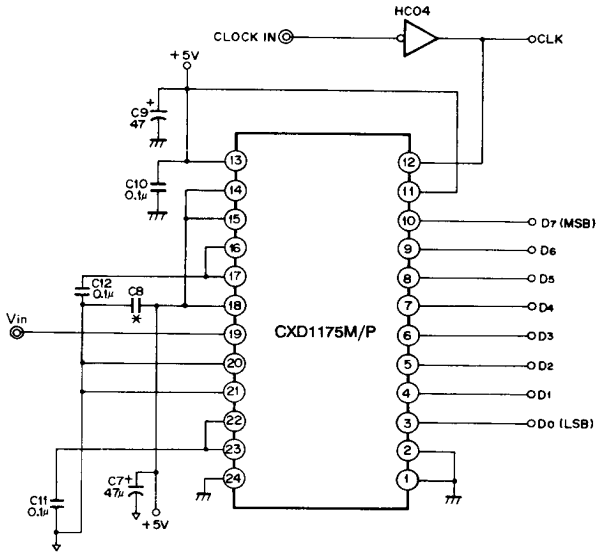
4. Reference input
   Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1μF, stable characteristics are obtained. By shorting V_{RT} and V_{RTS}, V_{RB} and V_{BRS}, the self bias function that generates V_{RT} = 2.6V and V_{RB} = 0.6V, is activated.

5. Timing
   Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

6. $\overline{OE}$ pin
   By connecting $\overline{OE}$ to GND output mode is obtained. By connecting to V_{DD} high impedance is obtained.

7. About latch up
   It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply.
   This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON.
   See "For latch up prevention" of CXD1175P/CXA1106P PCB description.

Application Circuit



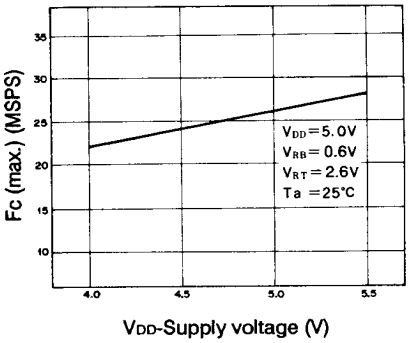
* : Ceramic Chip Condenser
0.1μF

⏚ : Analog GND

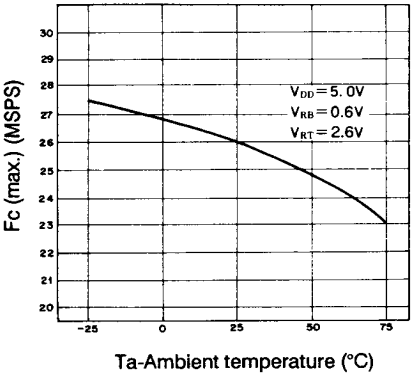
⏚ : Digital GND

Note) It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply.

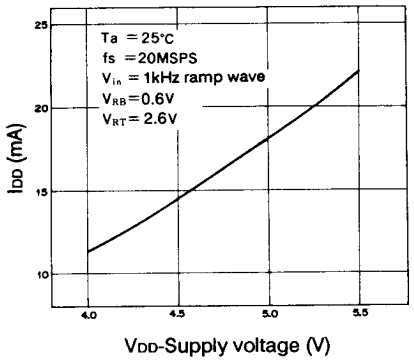
Fc (max.) vs. Supply voltage



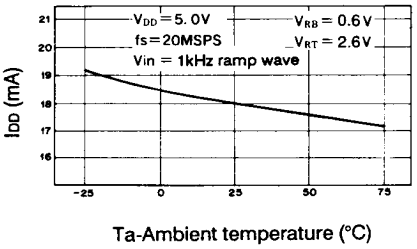
Fc (max.) vs. Ambient temperature

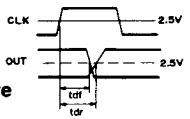


IDD vs. Supply voltage



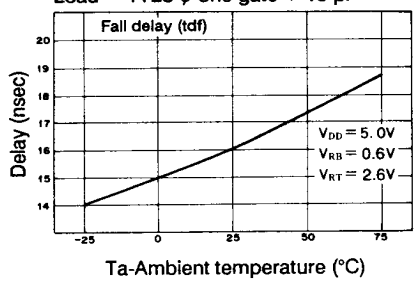
IDD vs. Ambient temperature





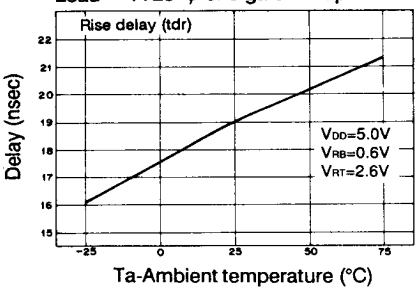
Output Delay vs. Ambient temperature

Load = TTLS ϕ one gate + 10 pF

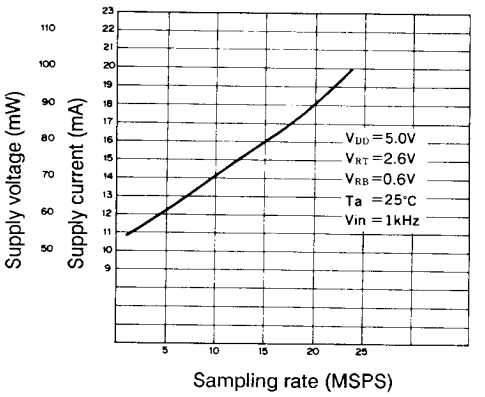


Output Delay vs. Ambient temperature

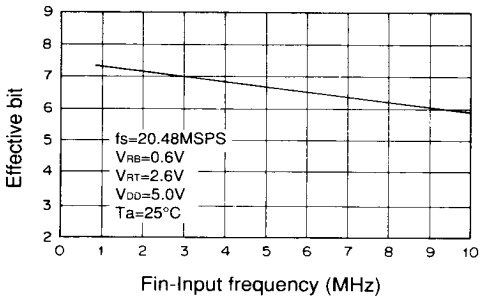
Load = TTLS ϕ one gate + 10pF



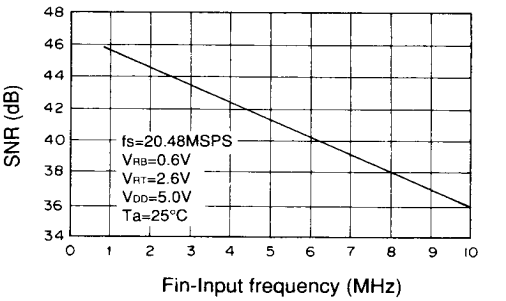
Supply current (voltage) vs. Sampling rate



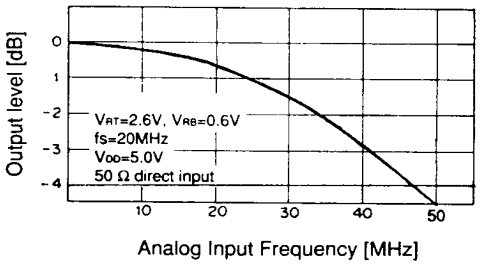
Eff bit vs. Fin



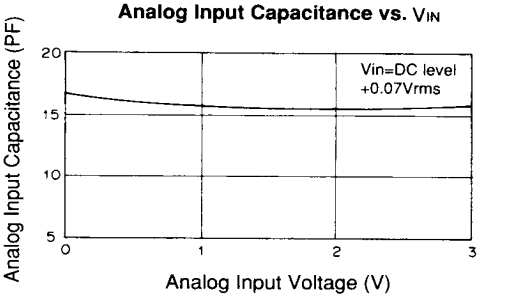
SNR vs. Fin



Output Level vs. Fin

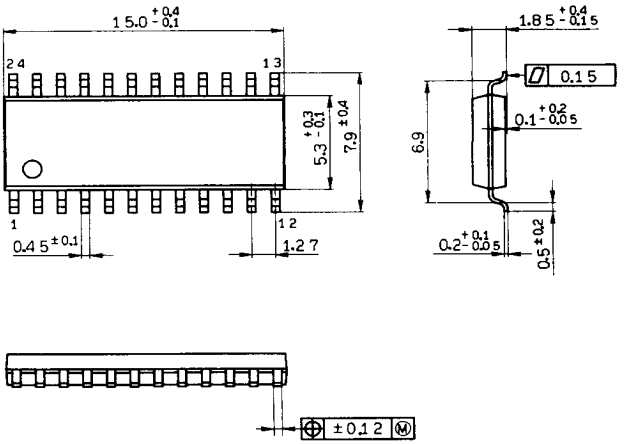


Analog Input Capacitance vs. V_{IN}



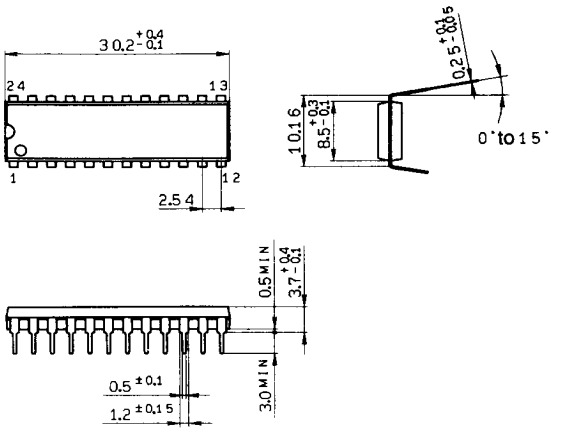
Package Outline Unit: mm

CXD1175M 24 pin SOP (Plastic) 300mil 0.3 g



SOP-24P-L01

CXD1175P 24 pin DIP (Plastic) 400mil 2.0 g



DIP-24P-01