SONY

CXD1267N

CCD Vertical Clock Driver

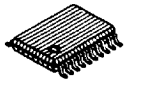
Description

The CXD1267N is a vertical clock driver for CCD image sensors. This IC is the successor of the CXD1250N with attractive features.

Features

1) Substrate voltage (Vsub) generator is built-in.
   - Variable Vsub in the range of 4.0V to 18.5V.
   - Reduction of peripheral parts saves space.
2) Only two power supplies (+15V and –8.5V) are needed.
   - V_{DD} (5V) and V_{HH} (20V) are eliminated.
3) 3.3V clock interface is acceptable.
4) 20-pin VSOP package is used.

20 pin VSOP (Plastic)



Applications

CCD cameras

Structure

CMOS

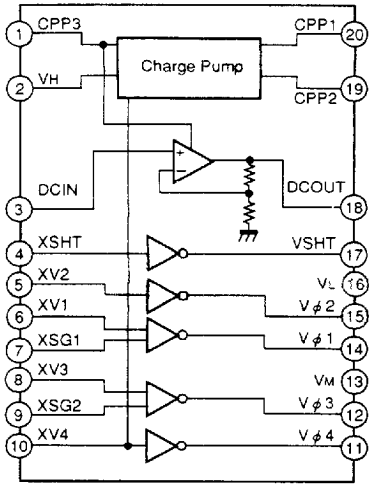
Absolute Maximum Ratings (Ta=25°C)

· Supply voltage	V_L	0 to –10	V
· Supply voltage	V_H	V_L–0.3 to 2V_L+35	V
· Supply voltage	V_M	V_L–0.3 to 3.0	V
· Input voltage	V_I	V_L–0.3 to V_H+0.3	V
· Output voltage (V2, V4)	$MV\phi$	V_L–0.3 to V_M+0.3	V
· Output voltage (V1, V3)	$HV\phi$	V_L–0.3 to V_H+0.3	V
· Output voltage (VSHT)	$HHV\phi$	V_L–0.3 to V_H+0.3	V
· Operational amplifier output current	I_{OUT}	±5	mA
· Operating temperature	Topr	–25 to +85	°C
· Storage temperature	Tstg	–40 to +125	°C

Recommended Operating Conditions

· Supply voltage	V_H	14.5 to 15.5	V
· Supply voltage	V_M	0	V
· Supply voltage	V_L	–7.5 to –9.0	V
· Input voltage (except for pin 3)	V_I	0 to 6.0	V
· Operational amplifier input voltage	V_{IOP}	1.0 to 4.5	V
· Operating temperature	Topr	–20 to +75	°C

Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	I/O	Description
1	CPP3	O	Charge pump
2	V_H	—	Power supply (15V)
3	DCIN	I	Operational amplifier input
4	XSHT	I	Output control (VSHT)
5	XV2	I	Output control (Vϕ2)
6	XV1	I	Output control (Vϕ1)
7	XSG1	I	Output control (Vϕ1)
8	XV3	I	Output control (Vϕ3)
9	XSG2	I	Output control (Vϕ3)
10	XV4	I	Output control (Vϕ4)
11	Vϕ4	O	High-voltage output (2 levels: V_M, V_L)
12	Vϕ3	O	High-voltage output (3 levels: V_H, V_M, V_L)
13	V_M	—	GND
14	Vϕ1	O	High-voltage output (3 levels: V_H, V_M, V_L)
15	Vϕ2	O	High-voltage output (2 levels: V_M, V_L)
16	V_L	—	Power supply (–8.5 V)
17	VSHT	O	High-voltage output (2 levels: V_H, V_L)
18	DCOUT	O	Operational amplifier output
19	CPP2	—	Charge pump
20	CPP1	—	Charge pump

Truth Table

Input				Output		
XV1 3	XSG1, 2	XV2, 4	XSHT	Vϕ1, 3	Vϕ2, 4	VSHT
L	L	X	X	V_H	X	X
H	L	X	X	Z	X	X
L	H	X	X	V_M	X	X
H	H	X	X	V_L	X	X
X	X	L	X	X	V_M	X
X	X	H	X	X	V_L	X
X	X	X	L	X	X	V_H
X	X	X	H	X	X	V_L

X: Don't care
Z: High impedance

Electrical Characteristics

DC Characteristics

(Unless otherwise specified, Ta=25°C, V_H=15V, V_M=GND, V_L=–8.5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		2.3	—	—	V
Low level input voltage	V_{IL}		—	—	1.3	V
High level output voltage	V_{OH}	I_O=–20 μA	14.9	15.0	—	V
Middle level output voltage	V_{OM1}	I_O=20 μA	—	0.0	0.1	V
Middle level output voltage	V_{OM2}	I_O=–20 μA	–0.1	0.0	—	V
Low level output voltage	V_{OL}	I_O=20 μA	—	–8.5	–8.4	V
Charge pump output voltage	V_{CPP3}	–1≦I_{CPP3}≦0mA I_{OUT}=0mA, Ta=–20 to 75°C V_{IOP}=4.5V	20	—	—	V
Input current	I_I	V_I=V_L to 5V	–1.0	0.0	1.0	μA
Operating supply current	I_H	*1	—	2.0	3.5	mA
Operating supply current	I_M	*1	—	4.5	5.0	mA
Operating supply current	I_L	*1	–8.5	–6.5	—	mA
Output current	I_{OL}	Vϕ1 to 4=–8.0V	25	—	—	mA
Output current	I_{OM1}	Vϕ1 to 4=–0.5V	—	—	–10	mA
Output current	I_{OM2}	Vϕ1, 3=0.5V	9	—	—	mA
Output current	I_{OH}	Vϕ1, 3=14.5V	—	—	–12	mA
Output current	I_{OSL}	VSHT=–8.0V	12	—	—	mA
Output current	I_{OSH}	VSHT=14.5V	—	—	–7	mA
Operational amplifier gain	G	I_{OUT}=–200/+100 μA	—	×4.40	—	
Gain error	ΔG	Ta=–20 to 75°C *2 I_{OUT}=–200/+100 μA V_{IOP}=1.0 to 4.5V	–3	—	3	%

*1 See Measurement Circuit. Shutter speed: 1/10000.
*2 See Operational Amplifier Gain Characteristic.
Note) Current directions: + indicates the direction flowing to IC; – indicates the direction flowing from IC

Switching Characteristics

(V_H=15V, V_M=GND, V_L=−8.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLM}	Load free*1	10	40	70	ns
Propagation delay time	T_{PMH}	Load free*1	10	30	70	ns
Propagation delay time	T_{PLH}	Load free*1	10	40	100	ns
Propagation delay time	T_{PML}	Load free*1	10	100	200	ns
Propagation delay time	T_{PHM}	Load free*1	10	100	180	ns
Propagation delay time	T_{PHL}	Load free*1	10	60	100	ns
Rise time	T_{TLM}	$V_L \rightarrow V_M$*1	400	700	930	ns
Rise time	T_{TMH}	$V_M \rightarrow V_H$*1	400	650	930	ns
Rise time	T_{TLH}	$V_L \rightarrow V_H$*1	10	50	100	ns
Fall time	T_{TML}	$V_M \rightarrow V_L$*1	200	300	500	ns
Fall time	T_{THM}	$V_H \rightarrow V_M$*1	400	600	820	ns
Fall time	T_{THL}	$V_H \rightarrow V_L$*1	10	50	100	ns
Charge pump boosting time	T_C	*2	—	—	10	ms
Output noise voltage	V_{CLH}	*3	—	—	0.5	V
Output noise voltage	V_{CLL}	*3	—	—	0.5	V
Output noise voltage	V_{CMH}	*3	—	—	0.5	V
Output noise voltage	V_{CML}	*3	—	—	0.5	V

*1 See Response of Voltage Pulse.

*2 CP1=0.1 μF, CP2=0.1 μF, V_{CPP3}=20V; boosting time after all power supplies rose.

*3 See Noise on a Waveform.

Note) Each item is evaluated by Measurement Circuit.

Notes on Operation (See Application Circuit.)

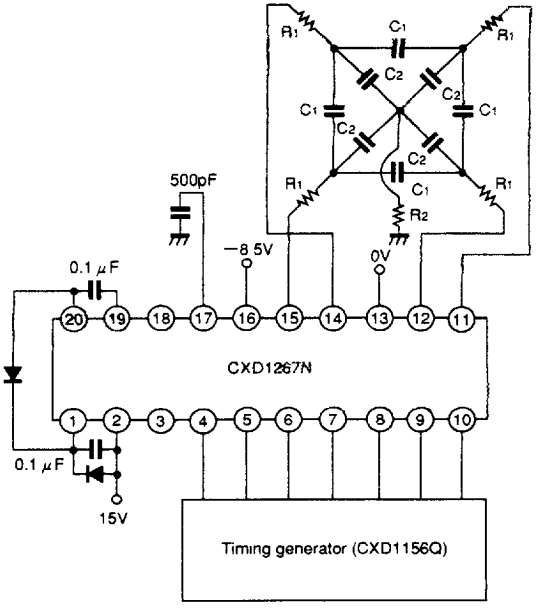
1. Be sure to protect against static electricity because this IC is MOS structure.

2. A bypass capacitor is connected between each power supply (V_H, V_L) and GND.

3. To prevent latch-up, use a capacitor of 0.1 μF (CP1, CP2) for charge pump.
   Insert a silicon diode (D2) between CPP3 and CPP1.

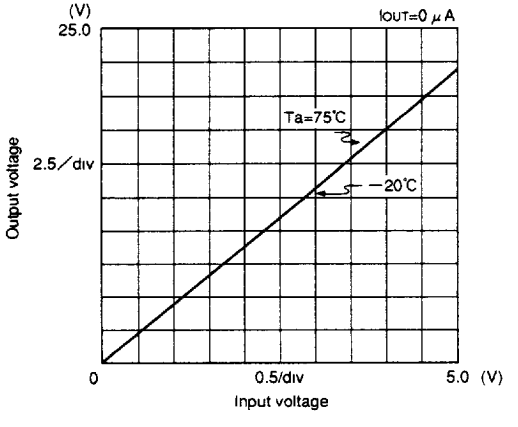
4. In order to protect CCD image sensor, pre-clamp is requested prior to clamp by DCOUT.

Measurement Circuit

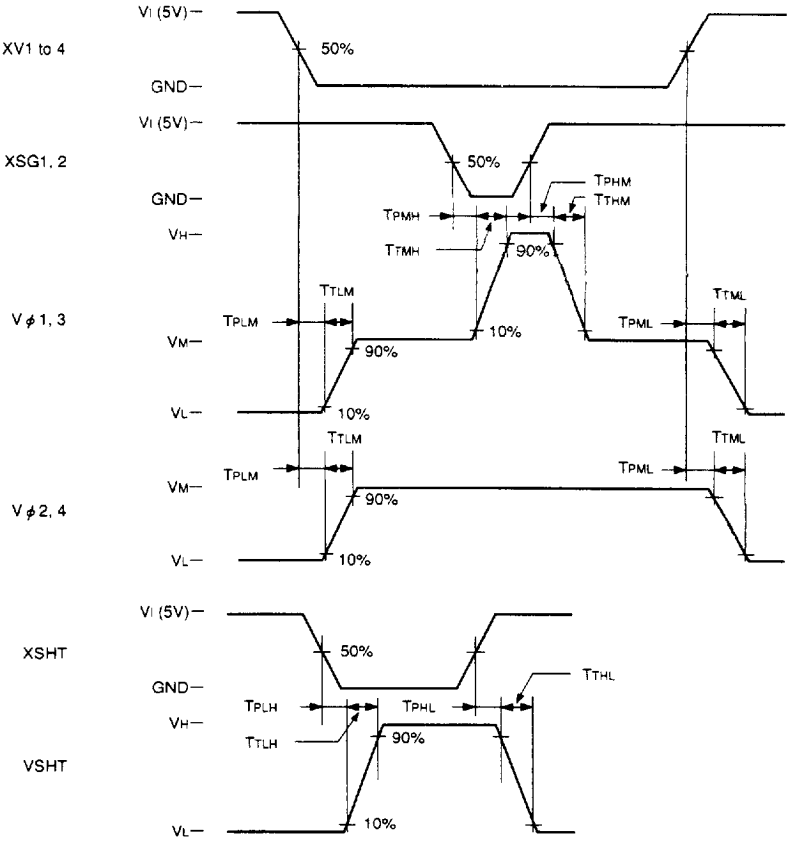


R1; 27Ω
R2; 5Ω
C1, 1500pF
C2; 3300pF

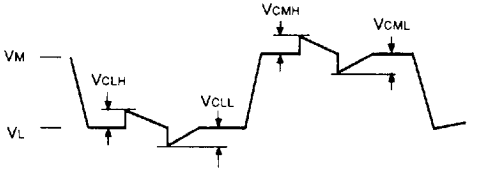
Operational Amplifier Gain Characteristics



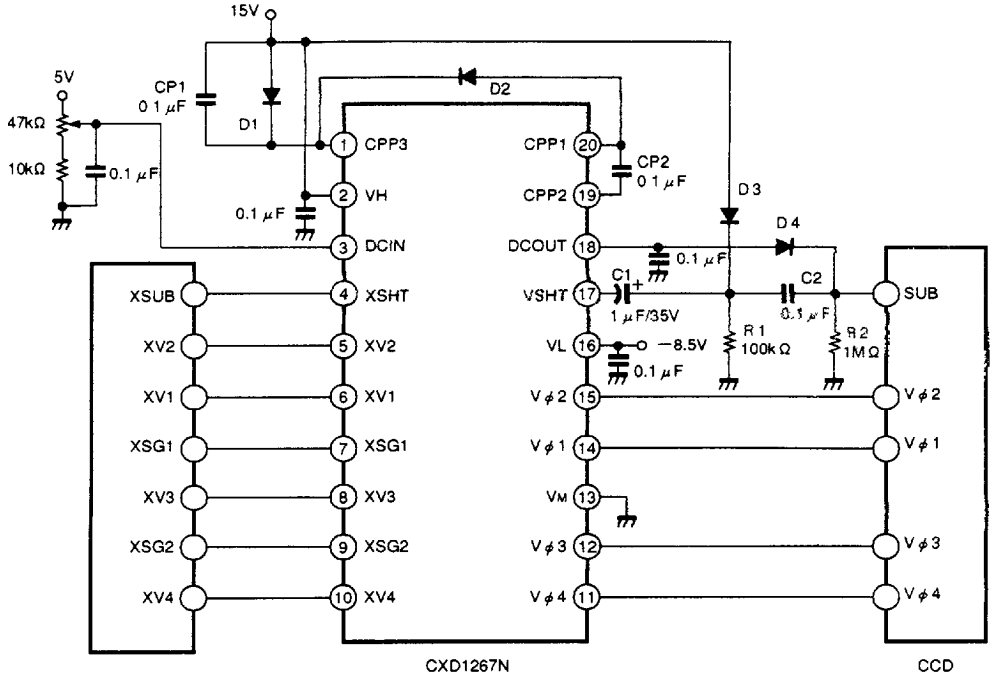
Response of Voltage Pulse



Noise on a Waveform



Application Circuit

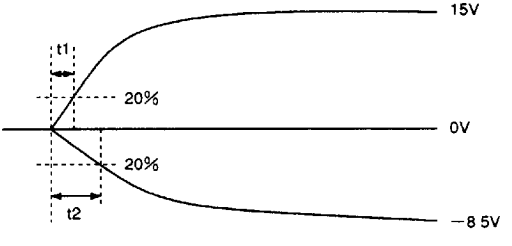


* A peripheral circuit can be simplified by CCD image sensor.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same

Note with power-on sequence

To protect CCD image sensor, rise two power supplies as follows.

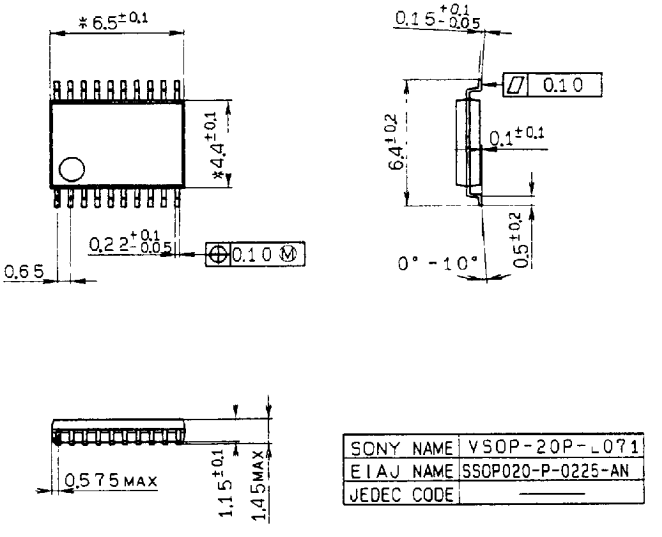


t2≧t1≧10ms

Package Outline

Unit: mm

20pin VSOP (Plastic) 225mil 0.086g



SONY NAME	VSOP-20P-L071
EIAJ NAME	SSOP020-P-0225-AN
JEDEC CODE	———

Note) Dimensions marked with * do not include resin residue.