SONY

CXD1272Q/R

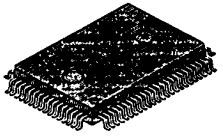
Cellular Phone Filter LSI with On-Chip Compandor *Preliminary*

Description

The CXD1272Q/R is a filter LSI for cellular phones. Successor to the CXD1271Q/R, this device features an on-chip compandor a new function fulfilling users' requests for a more versatile version of the CXD1271Q/R. Furthermore, addition of an attenuator for digital control provides for easy adjustment.

When used in conjunction with the control signal processor CXD1270Q/R IC, a modem can be implemented.

CXD1272Q
80 pin QFP (Plastic)



CXD1272R
80 pin VQFP (Plastic)

Features

- On-chip high-performance compandor in CMOS.
- Ultra-low current consumption:
  Operating current – 6mA; Power standby – 1mA
  (For standard 5V operation.)
- Power saver function provided.
- 4-bit attenuation controller facilitates gain adjustment over required range.
- Supports 4 standards
  AMPS, DOC, TACS, and N-TACS.
- Adoption of SCF technology provides stable characteristics
- On-chip 8-level, 3dB step electronic volume.

Functions

- Compandor
- Filtering of received data
- PLL lock detector for received SAT
- Filtering and addition performed on transmitted data
- Audio signal filtering for received/transmitted signals
- Gain controlled through serial data input
- Volume controller (Dual system)

Absolute Maximum Ratings

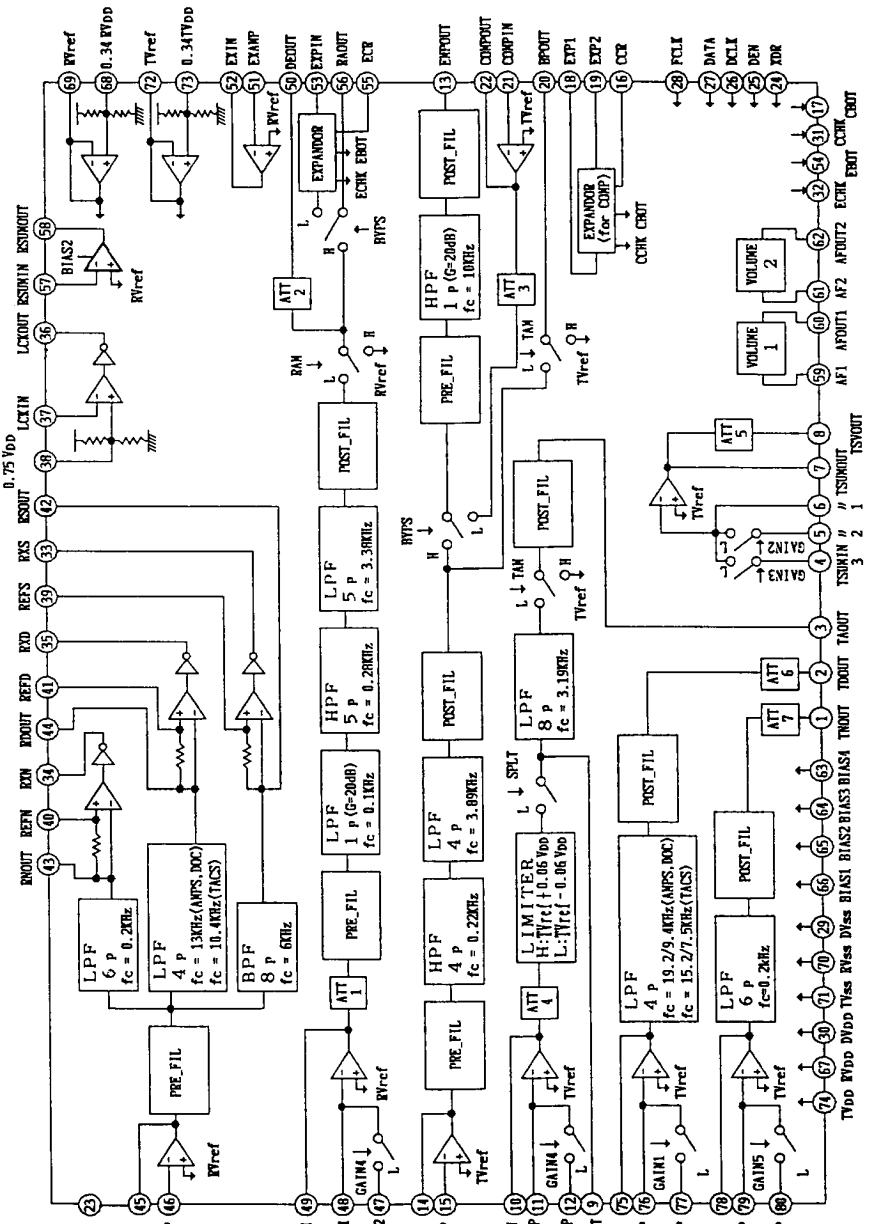
• Supply voltage	V_{DD}	–0.3 to 7.0	V
• Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
• Output voltage	V_{OUT}	–0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	–34 to +85	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	–34 to +85	°C

PE91Z32 – ST

Block Diagram



Pin Description

Pin No. QFP	Pin No. VQFP	Symbol	I/O	Description
3	1	TNOUT	O	Filter output for TX (N-TACS standard)
4	2	TDOUT	O	Filter output for TX Wide Band, ST, and SAT
5	3	TAOUT	O	TX Audio splutter filter output.
6	4	TSUMIN3	I	TX summing amplifier input. Gain is controlled by gain control "GAIN3"
7	5	TSUMIN2	I	TX summing amplifier input. Gain is controlled by gain control "GAIN2"
8	6	TSUMIN1	I	TX summing amplifier input. Used by TSUMIN2 and TSUMIN3 as well as for output data (TDOUT and TNOUT), and audio addition (TAOUT).
9	7	TSUMOUT	O	TX system summing amplifier output.
10	8	TSVOUT	O	Attenuated output for TX system summing amplifier. Controlled by control data "A5C3 to A5C0".
11	9	LIMOUT	I/O	TX audio limiter output. Also used as input for independent measurement of TX splutter filter characteristics of the latter stage.
12	10	LIMIN	O	Gain controller output used for input to limiter.
13	11	LIMAMP1	I	Limiter input 1.
14	12	LIMAMP2	I	Limiter input 2. Gain is controlled by gain control "GAIN4".
15	13	EMPOUT	O	Emphasis output for TX audio.
16	14	TAIN	O	Gain control amplifier output for TX audio input.
17	15	TAAMP	I	Gain control amplifier input from TX audio input.
18	16	CCR	O	Output for audio level detection circuit in the pin compressor Forms the low-pass filter by connecting a 1 µF capacitor between this pin and TVss.
19	17	CBOT	O	Reference voltage output from compressor.
20	18	EXP1	I	Expander input of the compressor structure
21	19	EXP2	O	Expander output of the compressor structure
22	20	BPOUT	I	Input to the internal compressor.
23	21	COMPIN	I	Operational amplifier input of the compressor structure
24	22	COMPOUT	O	Output from internal compressor.
25	23	—	—	—
26	24	XDR	I	Control data reset. Active at Low.
27	25	DEN	I	Load signal input for inputting serial data to data buffer. Active at High.
28	26	DCLK	I	Clock signal input for serial data input.
29	27	DATA	I	8-bit serial data input.
30	28	FCLK	I	Clock input for filter. 4.8MHz required.
31	29	DVss	—	Exclusive GND for digital circuits.
32	30	DV_{DD}	—	Exclusive power supply for digital circuits.

Pin No.		Symbol	I/O	Description
QFP	VQFP			
33	31	CCHK	O	Monitor for compressor offset adjustment.
34	32	ECHK	O	Monitor for expander offset adjustment.
35	33	RXS	O	Comparator output for RX SAT.
36	34	RXN	O	Comparator output for RX data (N-TACS standard)
37	35	RXD	O	Comparator output for RX Wide Band Data
38	36	LCKOUT	O	Output for PLL lock detection-use comparator of RX SAT
39	37	LCKIN	I	Input for PLL lock detection-use comparator of RX SAT
40	38	0.75VDD	I	Reference voltage input for PLL lock detection-use comparator of RX SAT. Bias at 0.75 times supply voltage. For normal operation, a 1 µF capacitor is externally connected between this pin and RVss.
41	39	REFS	I	Comparator reference voltage input for RX SAT. The offset bias effected by bandpass filter of the former stage can be eliminated by connecting a 0.1 µF capacitor between this pin and RVss
42	40	REFN	I	Comparator reference voltage input for RX data (N-TACS standard). The offset bias effected by low-pass filter of the former stage can be eliminated by connecting a 1 µF capacitor between this pin and RVss.
43	41	REFD	I	Comparator reference voltage input for RX Wide Band Data. The offset bias effected by low-pass filter of the former stage can be eliminated by connecting a 1 µF capacitor between this pin and RVss.
44	42	RSOUT	O	Filter output for RX SAT.
45	43	RNOUT	O	Filter output for N-TACS RX data (N-TACS standard).
46	44	RDOUT	O	Filter output for RX Wide Band Data. Used as a pre-filter for RX audio data.
47	45	RDIN	O	Gain controller amplifier output for RX Wide Band Data and SAT input.
48	46	RDAMP	I	Gain controller amplifier input for RX Wide Band Data and SAT input.
49	47	RAAMP2	I	Input 2 for RX audio data. Gain is controlled by gain control "Gain4".
50	48	RAAMP1	I	Input 1 for RX audio data.
51	49	RAIN	O	Gain control amplifier for RX audio data input.
52	50	DEOUT	O	RX audio filter output.
53	51	EXAMP	I	Gain control amplifier input for expander input.
54	52	EXIN	O	Gain control amplifier output for expander input.
55	53	EXPIN	I	Expander input.
56	54	EBOT	O	Expander reference voltage output.
57	55	ECR	O	Output for audio level detection circuit in the expander. Forms a low-pass filter by connecting a 1 µF capacitor between this pin and RVss. pin.
58	56	RAOUT	O	Filter output for RX audio data. (BYPS: High) Internal expander output. (BYPS: Low)
59	57	RSUMIN	I	Summing amplifier input for RX system. This signal used by DTMF and audio adder.
60	58	RSUMOUT	O	Summing amplifier output for RX system.
61	59	AF1	I	Volume 1 input.

Pin No. QFP	Pin No. VQFP	Symbol	I/O	Description
62	60	AFOUT1	O	Volume 1 output. Controlled by control data "V1C2 to V1C0".
63	61	AF2	I	Volume 2 input.
64	62	AFOUT2	O	Volume 2 output. Controlled by control data "V2C2 to V2C0".
65	63	BIAS4	I	Determines internal operational amplifier bias current of the compandor.
66	64	BIAS3	I	Determines internal operational amplifier bias current of the compandor.
67	65	BIAS2	I	Determines RX summing amplifier bias current.
68	66	BIAS1	I	Determines internal operation amplifier bias current.
69	67	RV_{DD}	—	Exclusive power supply for RX system.
70	68	$0.34RV_{DD}$	I	Reference voltage input for RX processing system operational amplifier. Bias at 0.34 times supply voltage. For normal operation, a 1 µF capacitor is connected between this pin and the RVss pin.
71	69	RVref	O	Reference voltage output for RX processing system operational amplifier. Bias at 0.34 times supply voltage. For normal operation, a 1 µF capacitor is connected between this pin and RVss.
72	70	RVss	—	Exclusive GND for RX system.
73	71	TVss	—	Exclusive GND for TX system.
74	72	TVref	O	Reference voltage output for TX processing system operational amplifier. Bias at 0.34 times supply voltage. For normal operation, a 1 µF capacitor is connected between this pin and TVss.
75	73	$0.34TV_{DD}$	I	Reference voltage input for TX processing system operational amplifier. Bias at 0.34 times supply voltage. For normal operation, a 1 µF capacitor is connected between this pin and RVss.
76	74	TV_{DD}	—	Exclusive power supply for TX system.
77	75	TDIN	O	Summing amplifier output for inputting RX Wide Band Data, ST, and SAT data.
78	76	TDAMP1	I	Input for TX SAT.
79	77	TDAMP2	I	Input for TX Wide Band Data and ST. Gain is controlled by gain control "GAIN1".
80	78	TNIN	O	Gain control amplifier output for inputting TX data (N-TACS standard).
1	79	TNAMP1	I	Input 1 for TX data (N-TACS standard).
2	80	TNAMP2	I	Input 2 for TX data (N-TACS standard).

Electrical Characteristics

(V_{DD}=5V ± 10%, Ta=–34 to +85°C)

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Power supply current 1 (N-TACS specification)	I_{DD1}	RV_{DD} TV_{DD} DV_{DD} Total	STD="L" STN="L" V1ST=V2ST="L" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	6	—	mA
Power supply current 2 (Specification other than N-TACS)	I_{DD2}	RV_{DD} TV_{DD} DV_{DD} Total	STD="L" STN="H" V1ST=V2ST="L" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	5.8	—	mA
Power supply current 3 (In standby status, excluding volume)	I_{STB1}	RV_{DD} TV_{DD} DV_{DD} Total	STD="H" STN="H" V1ST=V2ST="L" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	0.7	1.2	mA
Power supply current 4 (All in standby status)	I_{STB2}	RV_{DD} TV_{DD} DV_{DD} Total	STD="H" STN="H" V1ST=V2ST="H" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	0.6	1.0	mA
Digital input voltage "L"	V_{IL}	FCLK, DATA, DCLK, DEN, XDR	—	—	—	0.3V_{DD}	V
Digital input voltage "H"	V_{IH}	FCLK, DATA, DCLK, DEN, XDR	—	0.7V_{DD}	—	—	V
Digital input current "L"	I_{IL}	FCLK, DATA, DCLK, DEN, XDR	V_{IN}=GND	–10	—	10	µA
Digital input current "H"	I_{IH1}	FCLK, DATA, DCLK, DEN, XDR	V_{IN}=V_{DD}	–10	—	10	µA
Digital output voltage "L"	V_{OL}	RXD, RXN, RXS, LCKOUT	I_{OL}=0.4mA	—	—	0.8	V
Digital output voltage "H"	V_{OH}	RXD, RXN, RXS, LCKOUT	I_{OH}=–0.4mA	V_{DD}–1	—	—	V
Analog input voltage range	V_{LA}	RDAMP, RAAMP1, RAAMP2, TAAMP, TNAMP1, TNAMP2 TDAMP1, TDAMP2, RSUMIN, TSUMIN1, TSUMIN2, TSUMIN3 AF1, AF2	BIAS1=500kΩ	—	—	1	Vp-p
Analog input resistance	R_I	AF1, AF2	Input=–0.34V_{DD}	70	130	190	kΩ
Analog switch ON resistance	R_{SW}	TDAMP2, TSUMIN2, TSUMIN3, EXPOUT, RAOUT, RAAMP2, LIMAMP2, TNAMP2	Input=–0.34V_{DD}	—	0.6	1.5	kΩ

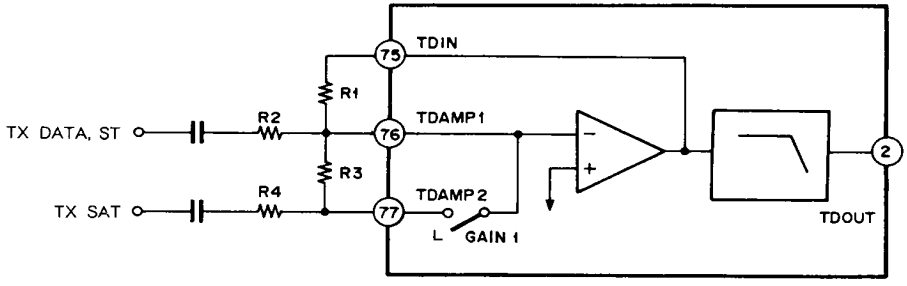
Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Analog output load resistance 1	R_{L1}	RSUMOUT	Output pin=–0.34V_{DD} BIAS2 resistance=100kΩ	2	—	—	kΩ
Analog output load resistance 2	R_{L2}	EXPIN, RAOUT, COMPIN, TAOUT, TDOUT, AFOUT1, EMPIN, TSUMOUT, TSVOUT, AFOUT2, TNOUT	Output pin=–0.34V_{DD} BIAS1 resistance=500kΩ	10	—	—	kΩ
Analog output load resistance 3	R_{L3}	RDIN, TAIN, TDIN, TNIN, RAIN	Output pin=–0.34V_{DD} BIAS1 resistance=500kΩ	100	—	—	kΩ
Analog output voltage range 1	V_{OA1}	RSUMOUT	BIAS2 resistance=100kΩ Load resistance=2kΩ	—	—	0.4	Vp-p
Analog output voltage range 2	V_{OA2}	RAOUT, EMPOUT, TSVOUT TSUMOUT, TAOUT, TDOUT, RDOUT, TNOUT, AFOUT1, AFOUT2	BIAS1 resistance=500kΩ Load resistance=10kΩ	—	—	0.4	Vp-p
Limiter voltage "L"	V_{LL}	LIMOUT	SPLT="L"	0.34V_{DD} –0.066 V_{DD}	0.34V_{DD} –0.06 V_{DD}	0.34V_{DD} –0.054 V_{DD}	V
Limiter voltage "H"	V_{LH}	LIMOUT	SPLT="L"	0.34V_{DD} +0.054 V_{DD}	0.34V_{DD} +0.06 V_{DD}	0.34V_{DD} +0.066 V_{DD}	V
Electronic volume step	V_{STEP}	AF1 – AFOUT1 AF2 – AFOUT2	—	2.5	3	3.5	dB
Attenuator step	A_{STEP}	—	—	0.2	0.4	0.6	dB
RX DATA filter gain 1 (AMPS)	G_{RD1}	RDAMP – RDOUT	Input: –18dBV 13kHz AT="H"	–5	–3	–1	dB
RX DATA filter gain 2 (TACS)	G_{RD2}	RDAMP – RDOUT	Input: –18dBV 10.4kHz AT="L"	–4	–3	–2	dB
RX DATA filter gain (N-TACS)	G_{RN}	RDAMP – RNOUT	Input: –18dBV 0.2kHz	–4	–3	–2	dB
RX SAT filter gain	G_{SAT}	RDAMP – RSOUT	Input: –18dBV 6kHz	–1	0	1	dB
TX DATA filter gain 1 (AMPS)	G_{TD1}	TDAMP1 – TDOUT	Input: –18dBV 19.2kHz AT="H", DS="H"	–5	–3	–1	dB
TX DATA filter gain 2 (AMPS)	G_{TD2}	TDAMP1 – TDOUT	Input: –18dBV 9.4kHz AT="H", DS="L"	–4	–3	–2	dB
TX DATA filter gain 3 (TACS)	G_{TD3}	TDAMP1 – TDOUT	Input: –18dBV 15.2kHz AT="L", DS="H"	–5	–3	–1	dB
TX DATA filter gain 4 (TACS)	G_{TD4}	TDAMP1 – TDOUT	Input: –18dBV 7.5kHz AT="L", DS="L"	–4	–3	–2	dB
TX DATA filter gain (N-TACS)	G_{TN}	TNAMP – TNOUT	Input: –18dBV 0.2kHz	–4	–3	–2	dB

Item		Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
RX audio filter gain		G_{RA}	RAAMP1 – RAOUT	Input: –16dBV 1kHz RAM="L", BYPS="H" ATT1=0dB	–1	–0.3	1	dB
RX audio muting volume		G_{RAM}	RAAMP1 – RAOUT	Input: –16dBV 1kHz RAM="H", BYPS="H" ATT1=0dB	50	—	—	dB
RX audio S/N ratio		SN_R	RAAMP1 – RAOUT	Input: –16dBV 1kHz RAM="L", BYPS="H" ATT1=0dB Band: 50Hz to 30kHz	50	—	—	dB
RX audio distortion		THD_R	RAAMP1 – RAOUT	Input: –16dBV 1kHz RAM="L", BYPS="H" ATT1=0dB Band: 50Hz to 30kHz	—	—	–50	dB
TX audio gain		G_{TA}	TAAMP – TAOUT	Input: –16dBV 1kHz TAM="L", BYPS="H" SPLT="L" ATT4=0dB	–1	–0.3	1	dB
TX audio muting volume		G_{TAM}	TAAMP – TAOUT	Input: –16dBV 1kHz TAM="H", BYPS="H" SPLT="L" ATT4=0dB	50	—	—	dB
TX audio S/N ratio		SN_T	TAAMP – TAOUT	Input: –16dBV 1kHz TAM="L", BYPS="H" SPLT="L" ATT4=0dB Band: 50Hz to 30kHz	45	—	—	dB
TX audio distortion factor		THD_T	TAAMP – TAOUT	Input: –16dBV 1kHz TAM="L", BYPS="H" SPLT="L" ATT4=0dB Band: 50Hz to 30kHz	—	—	–45	dB
Compressor	Input reference level		COMPIN–COMPOUT		—	0	—	dBV
	Output level		COMPIN–COMPOUT	Input: –20dBV Input: –70dBV	—	–10 –35	—	dBV
	Rise time		COMPIN–COMPOUT	12dB step input	—	3.0	—	ms
	Fall time		COMPIN–COMPOUT	12dB step input	—	13.5	—	ms
Expander	Input reference level		EXPIN – RAOUT		—	0	—	dBV
	Output level		EXPIN – RAOUT	Input: –10dBV Input: –35dBV	—	–20 –70	—	dBV
	Rise time		EXPIN – RAOUT	6dB step input	—	13.5	—	ms
	Fall time		EXPIN – RAOUT	6dB step input	—	13.5	—	ms

Note) 0dBV=1Vrms

Notes on Operation

1. Summing Amplifier Gain Adjustment for TX Data



Note) Pin numbers are for VQFP package.

In the above circuit, R1 and R2 adjust attenuation factor for TX DATA and ST, and R1, R3, and R4 adjust attenuation factor for TX SAT. An attenuation factor of –20dB is recommended.

R3 is also used to compensate TX output level differential between DATA and ST.

For ST transmission, GAIN1 is set at "L" to raise the gain, and for DATA transmission, GAIN1 is set at "H" to lower the gain.

2. Standard Setting and TX Data Mode

To accommodate each standard setting and TX data mode, the cut-off frequencies for data filters are controlled. This control is performed by control data "AT" and "DS".

TX data / Standard	WBD	ST, SAT
AMPS, DOC	AT=H DS=H	AT=H DS=L
TACS, N-TACS	AT=L DS=H	AT=L DS=L

3. Standby Control

Data "STD", "STN", "V1ST", and "V2ST" independently perform standby control.

Control data	Control block	"H"	"L"
STD	All data processing section other than VOLUME1, VOLUME2, and N-TACS	Activates only blocks up to RDAMP-RXD and the RVref generation circuit	Active
STN	N-TACS data processing block (fc=0.2kHz, 6th-order LPF)	Standby	Active
V1ST	VOLUME1	Standby	Active
V2ST	VOLUME2	Standby	Active

Note) Setting STD="H" and STN="L" is strictly prohibited.

4. Attenuation and Volume Control

For ports where fine adjustment of the audio signal is necessary, a 4-bit attenuation controller (ATT1–ATT7) is provided which conducts level setting using serially input data.

Also, for controlling volume for speakers and ringing, etc, a dual system, 3-bit electronic volume controller is included on-chip.

* ATT1 to 7

C3	C2	C1	C0	GAIN
1	1	1	1	–2.8
1	1	1	0	–2.4
1	1	0	1	–2.0
1	1	0	0	–1.6
1	0	1	1	–1.2
1	0	1	0	–0.8
1	0	0	1	–0.4
1	0	0	0	0
0	1	1	1	0.4
0	1	1	0	0.8
0	1	0	1	1.2
0	1	0	0	1.6
0	0	1	1	2.0
0	0	1	0	2.4
0	0	0	1	2.8
0	0	0	0	3.2

dB

* VOLUME1, 2

C2	C1	C0	GAIN
1	1	1	–21
1	1	0	–18
1	0	1	–15
1	0	0	–12
0	1	1	–9
0	1	0	–6
0	0	1	–3
0	0	0	0

dB

5. Serial Data Format (8-bit serial)

7 6 5 4 3 2 1 0 →

7	6	5	4	3	2	1	0	
0	0	0	0	AT 0	DS 1	STN 1	STD 1	
0	0	0	1	RAM 1	TAM 1	BYPS 0	SPLT 0	
0	0	1	0	GAIN1 0	GAIN2 0	GAIN3 0		
0	0	1	1	EA3 0	EA2 0	EA1 0	EA0 0	
0	1	0	0	EA5 1	EA4 0	CA5 1	CA4 0	
0	1	0	1	CA3 0	CA2 0	CA1 0	CA0 0	
0	1	1	0	V1C2 1	V1C1 1	V1C0 1	V1ST 1	VOLUME1
0	1	1	1	V2C2 1	V2C1 1	V2C0 1	V2ST 1	VOLUME2
1	0	0	0	A1C3 1	A1C2 0	A1C1 0	A1C0 0	ATT1
1	0	0	1	A2C3 1	A2C2 0	A2C1 0	A2C0 0	ATT2
1	0	1	0	A3C3 1	A3C2 0	A3C1 0	A3C0 0	ATT3
1	0	1	1	A4C3 1	A4C2 0	A4C1 0	A4C0 0	ATT4
1	1	0	0	A5C3 1	A5C2 0	A5C1 0	A5C0 0	ATT5
1	1	0	1	A6C3 1	A6C2 0	A6C1 0	A6C0 0	ATT6
1	1	1	0	A7C3 1	A7C2 0	A7C1 0	A7C0 0	ATT7
1	1	1	1			GAIN4 0	GAIN5 0	

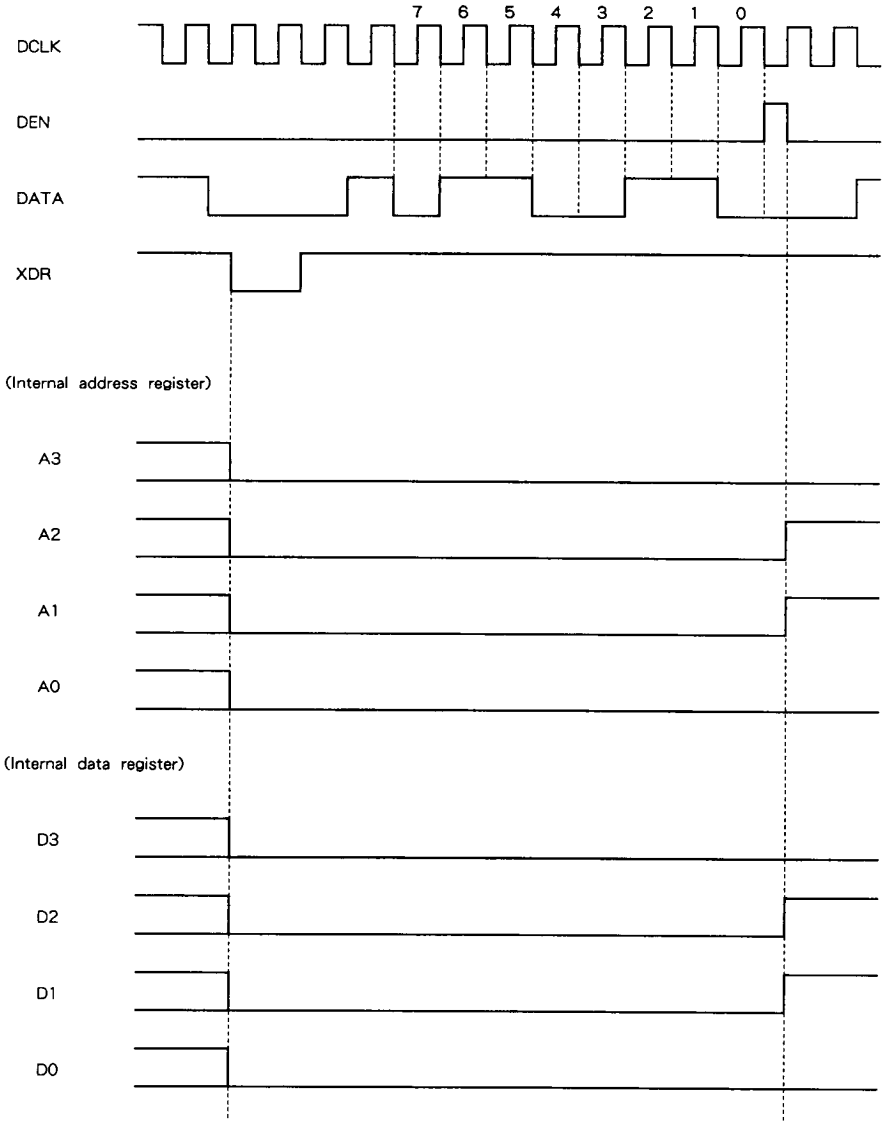
Address Data

Note: The numbers on the left half of the table are the status of each data at the time of data reset (XDR=L).

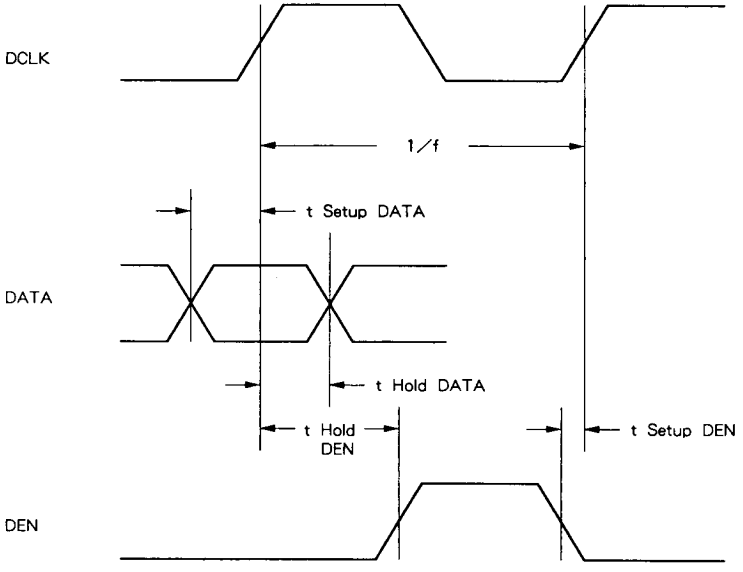
Data Description

AT : Cellular standard switchover. (For AMPS and DOC - "H", for TACS and N-TACS - "L".)
DS : TX data switchover. (For Wide Band Data – "H", for ST data – "L".)
STD : Standby controls for processing blocks other than at N-TACS data processing and volume blocks. Power save activated at "H". (However, RX blocks operate as usual.)
STN : Standby control for N-TACS data processing block. In standby for "H".
V1ST : VOLUME1 standby control. Standby at "H".
V2ST : VOLUME2 standby control. Standby at "H".
SPLT, BYPS, GAIN1, GAIN2, GAIN3, GAIN4, and GAIN5 : Refer to block diagram.
EA5 to EA0 : Expander adjustment.
CA5 to CA0 : Compressor adjustment.
The remaining data controls VOLUME1, VOLUME2, and ATT1 to ATT7.

6. Serial Data Timing Chart

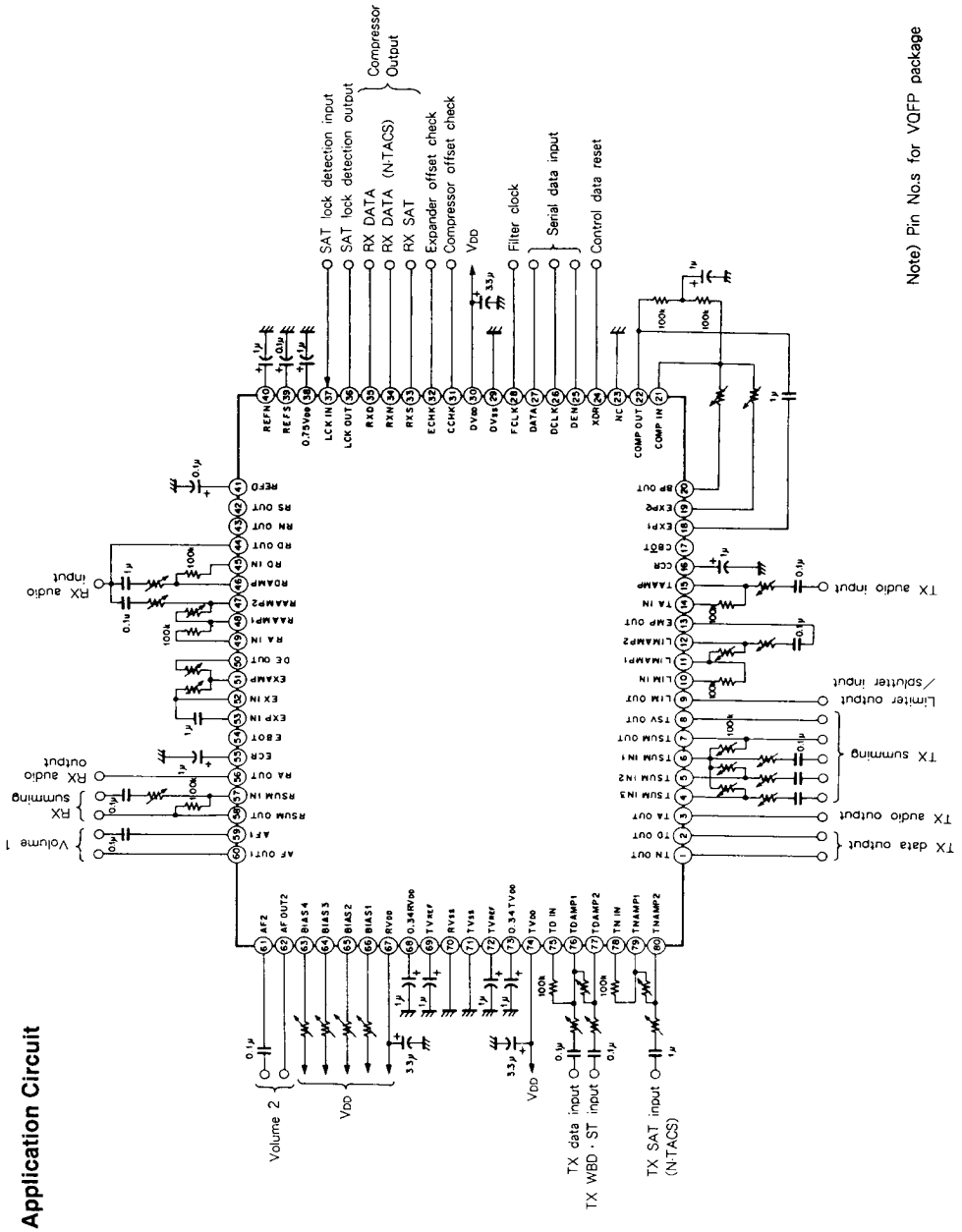


7. Serial Data Switching Characteristics



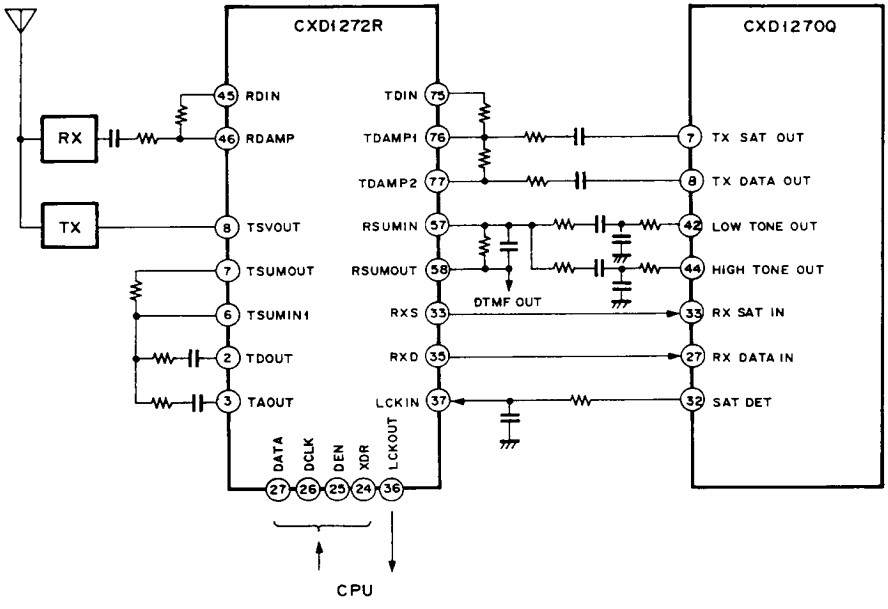
Item	Symbol	Min.	Typ.	Max.	Unit
DATA Set up Time	t Setup DATA	500	—	—	ns
DATA Hold Time	t Hold DATA	500	—	—	ns
DEN Set up Time	t Setup DEN	100	—	—	ns
DEN Hold Time	t Hold DEN	500	—	—	ns
DCLK frequency	f	—	—	1.2	MHz

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Connection Example of CXD1272R and CXD1270Q

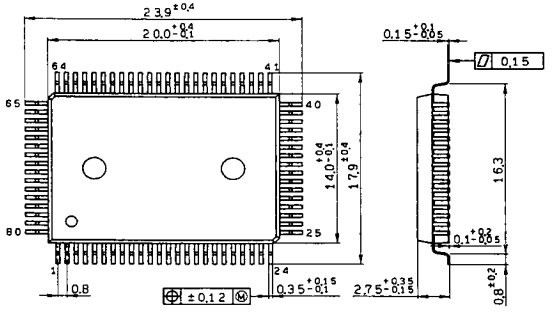


Package Outline

Unit : mm

CXD1272Q

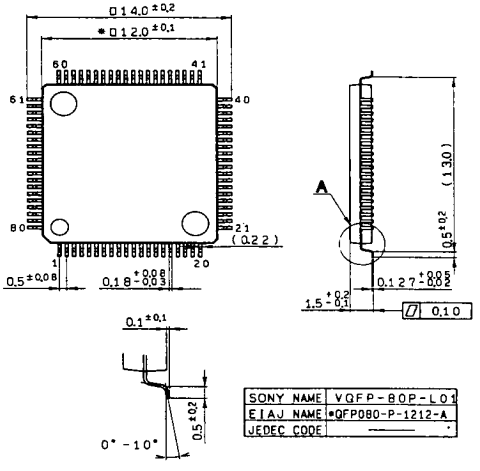
80pin QFP (Plastic) 1.6g



SONY NAME	QFP-80P-L01
EIAJ NAME	*QFP080-P-1420-A
JEDEC CODE	———

CXD1272R

80pin VQFP (Plastic) 0.5g



SONY NAME	VQFP-80P-L01
EIAJ NAME	*QFP080-P-1212-A
JEDEC CODE	———

Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.