SONY **CXD2411R**

Timing Generator for Color LCD Panels

Description

The CXD2411R is a timing signal generator for color LCD panel drivers.

Features

- Generates the LCX005BK and LCX009 drive pulse
- Supports right/left inverse display
- Supports 16:9 wide display (LCX009)
- Supports line inversion and field inversion
- AC drive for LCD panel during no signal (NTSC/PAL)
- Generates timing signal of external sample-and-hold circuit
- AFC circuit supporting static and dynamic fluctuations

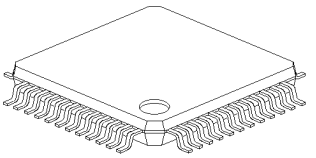
Applications

- Color LCD View Finder
- Single-panel and three-panel projectors

Structure

Silicon gate CMOS IC

48 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta = +25°C)

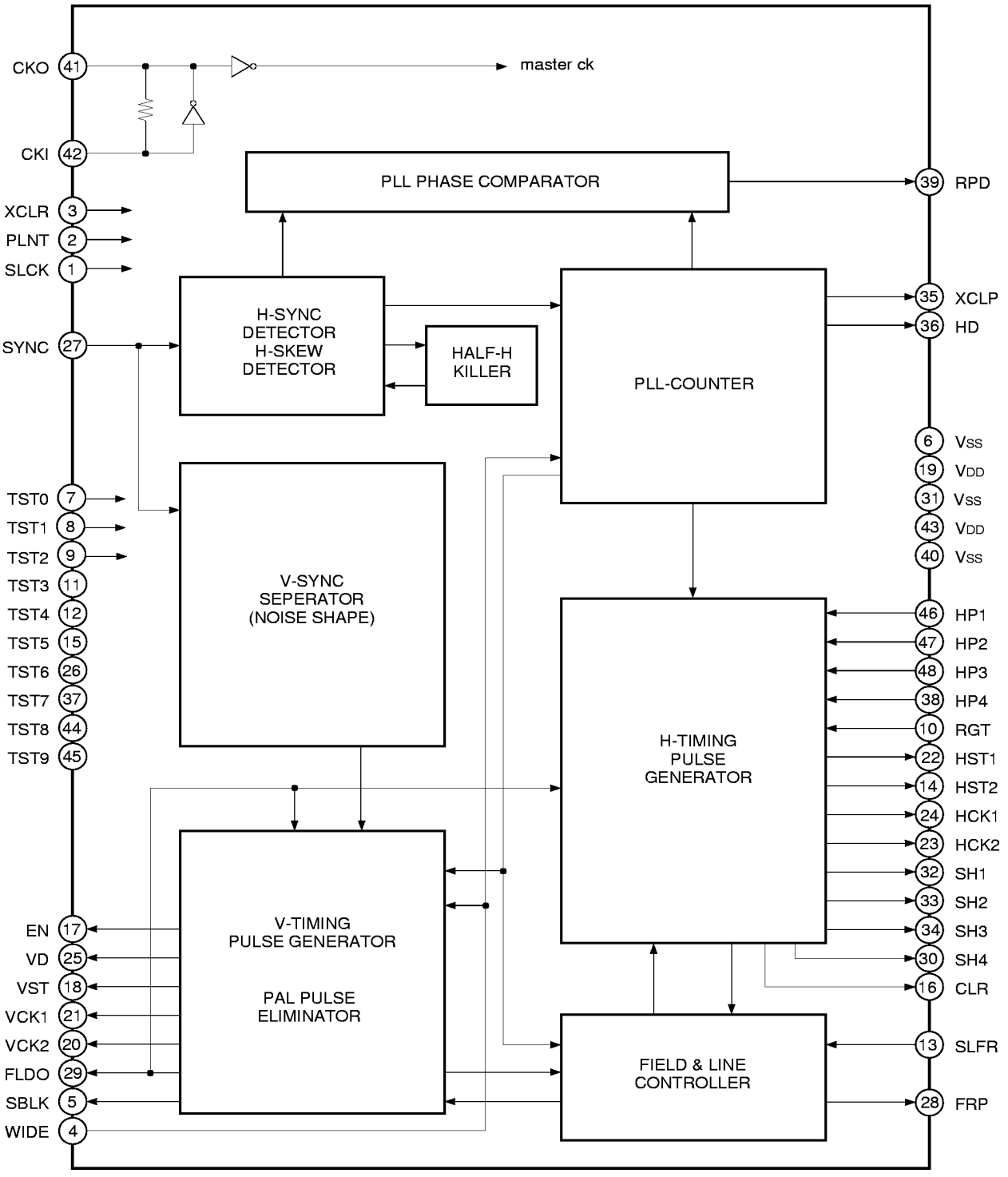
• Supply voltage	V_{DD}	V_{SS}–0.5 to +7.0	V
• Input voltage	V_I	V_{SS}–0.5 to V_{DD} +0.5	V
• Output voltage	V_O	V_{SS}–0.5 to V_{DD} +0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Strage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 5.5	V
• Operating temperature	Topr	–20 to +75	°C

E94629–ST

Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description	Input Pin for Open Status
1	SLCK	I	Switches between LCX005BK (H) and LCX009 (L)	L
2	PLNT	I	Switches between PAL (H) and NTSC (L)	L
3	XCLR	I	Cleared at 0V	H
4	WIDE	I	Switches between 16:9 display (H) and 4:3 display (L)	L
5	SBLK	O	Black signal pulse output (during WIDE MODE) (positive polarity)	—
6	V_{SS}	—	GND	
7	TST0	I	Test	L
8	TST1	I	Test	L
9	TST2	I	Test	L
10	RGT	I	Switches between Normal scan (H) and Reverse scan (L)	H
11	TST3	—	Not connected	—
12	TST4	—	Not connected	—
13	SLFR	I	Switches between field inversion (H) and line inversion (L)	L
14	HST2	O	H start pulse 2 (positive polarity)	—
15	TST5	—	Not connected	—
16	CLR	O	CLR pulse output (positive polarity)	—
17	EN	O	EN pulse output (negative polarity)	—
18	VST	O	V start pulse (positive polarity)	—
19	V_{DD}	—	Power supply	—
20	VCK2	O	V clock pulse 2	—
21	VCK1	O	V clock pulse 1	—
22	HST1	O	H start pulse 1 (positive polarity)	—
23	HCK2	O	H clock pulse 2	—
24	HCK1	O	H clock pulse 1	—
25	VD	O	VD pulse output (positive polarity)	—
26	TST6	—	Not connected	—
27	SYNC	I	Composite sync input (positive polarity)	—
28	FRP	O	AC drive timing pulse output	—
29	FLDO	O	Field identification signal output	—
30	SH4	O	Sample-and-hold pulse (positive polarity)	—
31	V_{SS}	—	GND	—
32	SH1	O	Sample-and-hold pulse (positive polarity)	—
33	SH2	O	Sample-and-hold pulse (positive polarity)	—
34	SH3	O	Sample-and-hold pulse (positive polarity)	—

Pin No.	Symbol	I/O	Description	Input Pin for Open Status
35	XCLP	O	Burst position clamp pulse output (negative polarity)	—
36	HD	O	HD pulse output (positive polarity)	—
37	TST7	—	Not connected	—
38	HP4	I	Switches for the horizontal display position	H
39	RPD	O	Phase comparator output	—
40	V_{SS}	—	GND	—
41	CKO	O	Oscillation cell (output)	—
42	CKI	I	Oscillation cell (input)	—
43	V_{DD}	—	Power supply	—
44	TST8	—	Not connected	—
45	TST9	—	Not connected	—
46	HP1	I	Switches for the horizontal display position	L
47	HP2	I	Switches for the horizontal display position	L
48	HP3	I	Switches for the horizontal display position	L

(H: Pull up, L: Pull down)

Electrical Characteristics

1. DC Characteristics

(Temperature = +25°C, V_{SS} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		3.0		5.5	V
Input voltage	V_{IH}	TTL input cell (5V±10%)	2.2			V
Input voltage	V_{IH}	TTL input cell (3.3V±10%)	1.8			V
Input voltage	V_{IL}	TTL input cell			0.8	V
Input voltage	V_{IH}	CMOS input cell	0.7V_{DD}			V
Input voltage	V_{IL}	CMOS input cell			0.3V_{DD}	V
Output voltage	V_{OH}	I_{OH} = –4mA (HCKn, VCKn)	V_{DD}–0.8			V
Output voltage	V_{OL}	I_{OL} = 8mA (HCKn, VCKn)			0.4	V
Output voltage	V_{OH}	I_{OH} = –3mA (CKO, CKI)	V_{DD}/2			V
Output voltage	V_{OL}	I_{OL} = 3mA (CKO, CKI)			V_{DD}/2	V
Output voltage	V_{OH}	I_{OH} = –2mA (other than the above)	V_{DD}–0.8			V
Output voltage	V_{OL}	I_{OL} = 4mA (other than the above)			0.4	V
Input leak current	I_L	Normal input pin	–10		10	µA
Input leak current	I_{IL}	Pull up resistor connected	–12	–100	–240	µA
Input leak current	I_{IH}	Pull down resistor connected	12	100	240	µA
Output leak current	I_{LZ}	RPDn, FPDn (at high impedance state)	–40		40	µA
Current consumption	I_{DD}			25		mA

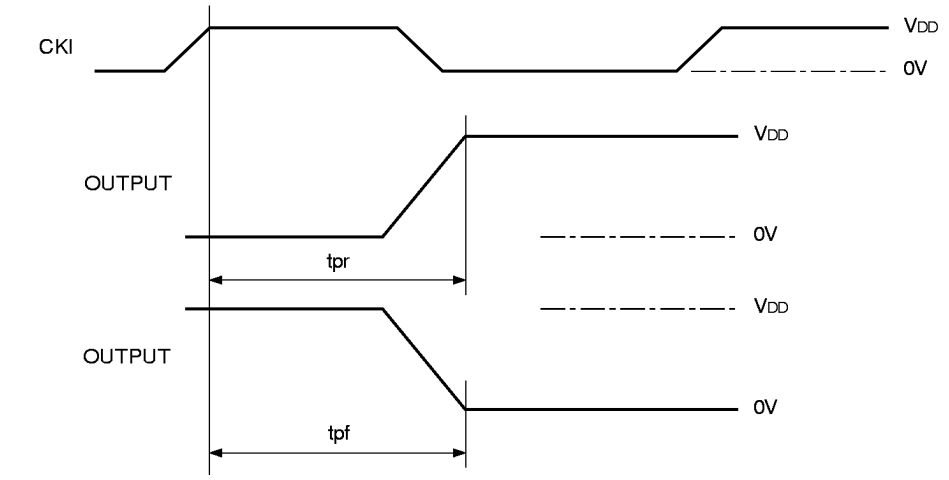
2. AC Characteristics

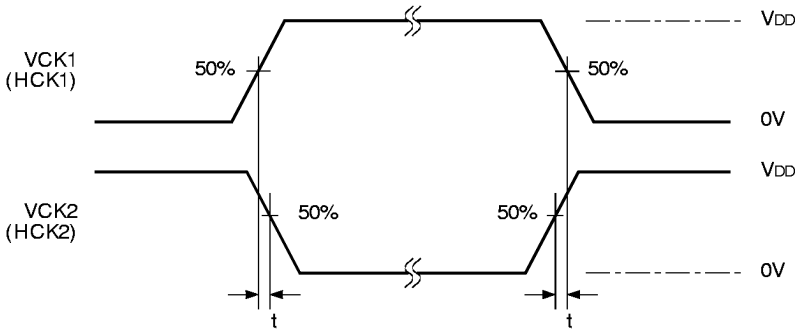
(V_{DD} = 3.0 to 5.5V)

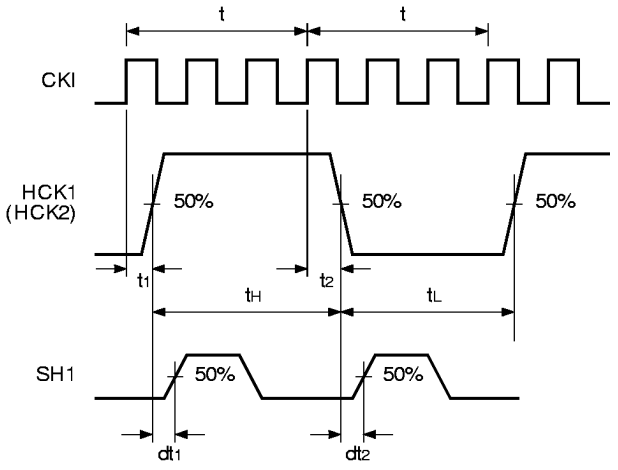
Item	Applicable Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock input cycle	CKI			60			ns
Cross-point time difference	HCK1 , HCK2	Δt	CL = 30pF			10	ns
Cross-point time difference	VCK1 , VCK2	Δt	CL = 30pF			10	ns
Output rise delay	HCKn , VCKn	tpr	CL = 30pF			30	ns
Output fall delay	HCKn , VCKn	tpf	CL = 30pF			25	ns
Output rise delay	Other than HCKn and VCKn	tpr	CL = 30pF			40	ns
Output fall delay	Other than HCKn and VCKn	tpf	CL = 30pF			22	ns
HCK1, SH1 delay time difference	HCK1 , SH1	dt1	CL = 30pF	60		85	ns
HCK1, SH1 delay time difference	HCK1 , SH1	dt2	CL = 30pF	60		95	ns
HCK2, SH1 delay time difference	HCK2 , SH1	dt1	CL = 30pF	60		85	ns
HCK2, SH1 delay time difference	HCK2 , SH1	dt2	CL = 30pF	60		95	ns
HCK1 Duty	HCK1	tH/tH + tL	CL = 30pF	46		52	%
HCK2 Duty	HCK2	tH/tH + tL	CL = 30pF	46		52	%

Note) n = 1, 2

Timing Definition







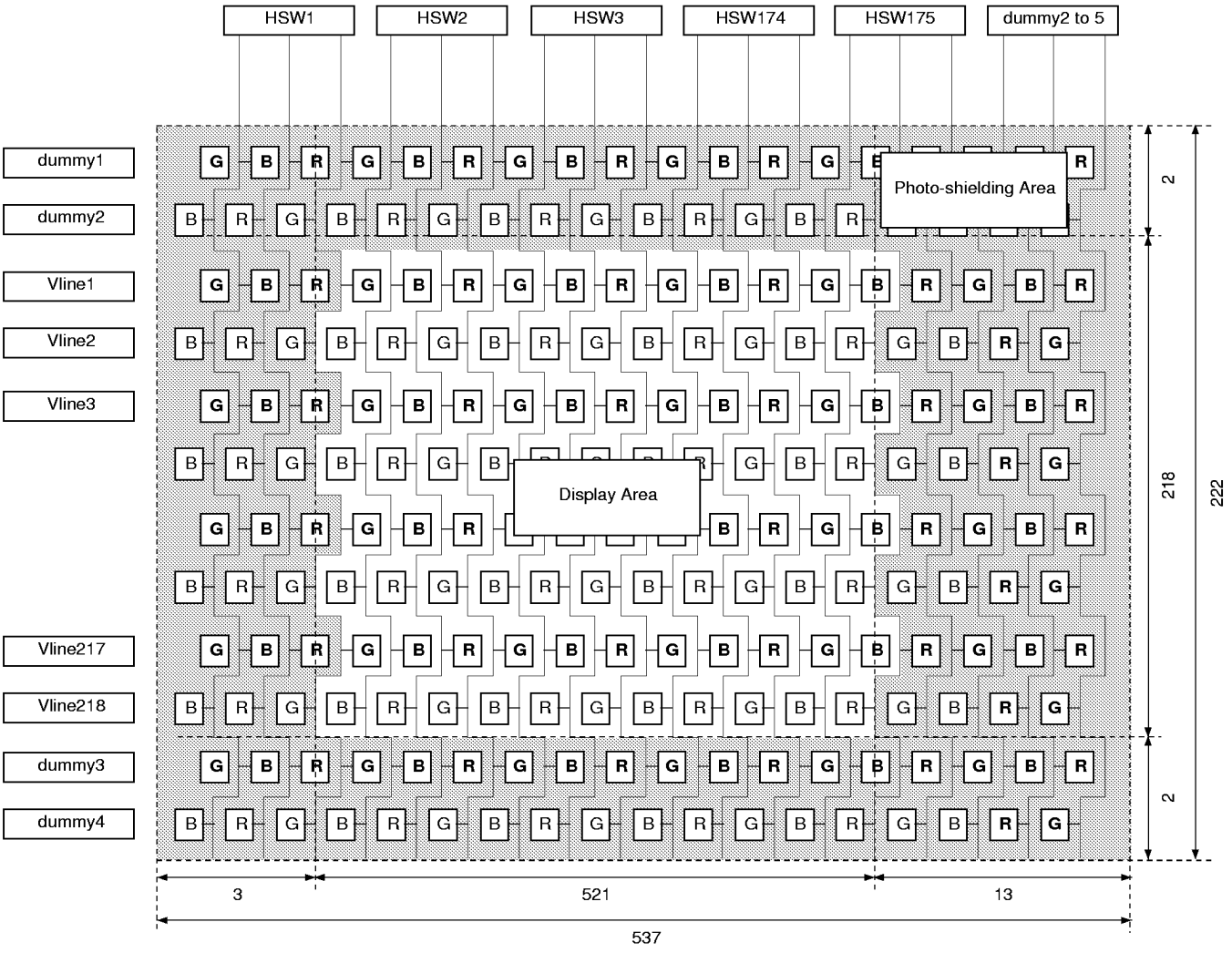
$t_H - t_L = 2\,(t - t_1)$

$\left(\begin{array}{l} t_H = t - t_1 + t_2 \\ t_L = t - t_2 + t_1 \\ t_H - t_L = 2\,(t_2 - t_1) \end{array}\right)$

LCX005BK/BKB and LCX009AK/AKB Color Coding Diagram

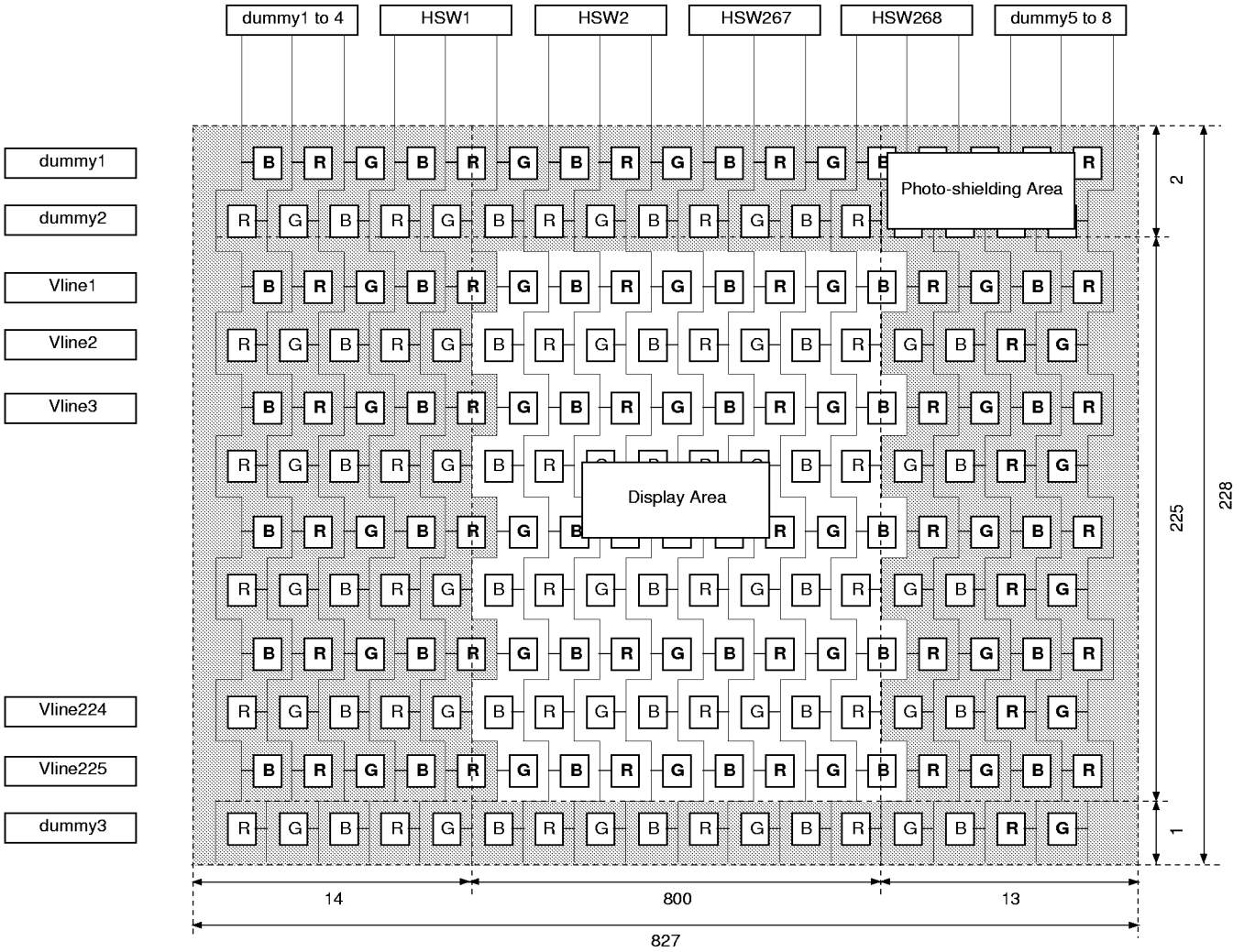
The delta arrangement is used for the color coding in the LCD panels with which this IC is compatible. Note that the shaded region within the diagram is not displayed.

LCX005BK Pixel Arrangement



Basic Specifications	
Total horizontal dots:	537H
Horizontal display dots:	521H
Total vertical dots:	222H
Vertical display dots:	218H
Total dots:	119,214H
Display dots:	113,578H

LCX009AK Pixel Arrangement



Basic Specifications	
Total horizontal dots:	827H
Horizontal display dots:	800H
Total vertical dots:	228H
Vertical display dots:	225H
Total dots:	188,556H
Display dots:	180,000H

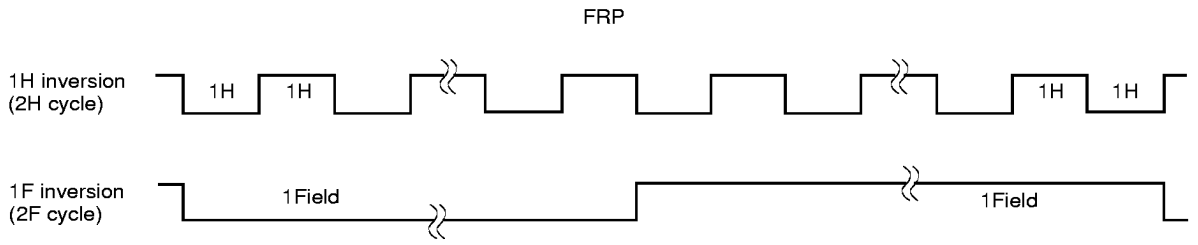
Description of the Mode Selection Switch (SLCK, PLNT, WIDE)

SLCK	PLNT	WIDE	MODE
H	L	L	LCX005BK/NTSC/NORMAL
H	L	H	—
H	H	L	LCX005BK/PAL/NORMAL
H	H	H	—
L	L	L	LCX009/NTSC/NORMAL
L	L	H	LCX009/NTSC/WIDE
L	H	L	LCX009/PAL/NORMAL
L	H	H	LCX009/PAL/WIDE

* NORMAL (4:3 display), WIDE (16:9 display)
WIDE is supported in LCX009 mode only.

SLFR

SLFR is the selector switch for the AC drive timing pulse (FRP). This switch selects field inversion when H and line inversion when L. Normally, line inversion (L) is used. The transition point is one clock cycle after the transition point of the VCK1 and VCK2 pulses.



* FRP polarity is not specified.

HP1, 2, 3, 4

These are selector switches for the horizontal display position. The HST timing can be set at 2fh intervals in 16 different ways by using the four HST position bits. In addition, the picture center is aligned at internal preset: 1000 (NTSC and PAL modes in the LCX005BK/009). However, actually, because there is a difference between the video signal and drive pulse delays, the picture center may not be in the right position. In this case, adjust with these switches.

The HST timing (from SYNC termination to the rising edge of HST) for even lines is shown below.

LCX005BK (NTSC, PAL)

HP4	HP3	HP2	HP1	HST1 (NTSC/PAL)	HST2 (NTSC/PAL)
0	0	0	0	72fh (6.51/6.56µs)	74.5fh (6.74/6.79µs)
0	0	0	1	70fh	72.5fh
0	0	1	0	68fh	70.5fh
0	0	1	1	66fh	68.5fh
0	1	0	0	64fh	66.5fh
0	1	0	1	62fh	64.5fh
0	1	1	0	60fh	62.5fh
0	1	1	1	58fh	60.5fh
1	0	0	0	56fh (5.06/5.11µs)	58.5fh (5.29/5.33µs)
1	0	0	1	54fh	56.5fh
1	0	1	0	52fh	54.5fh
1	0	1	1	50fh	52.5fh
1	1	0	0	48fh	50.5fh
1	1	0	1	46fh	48.5fh
1	1	1	0	44fh	46.5fh
1	1	1	1	42fh (3.80/3.83µs)	44.5fh (4.02/4.06µs)

* The HST1 and 2 timing for odd lines is delayed or advanced 1.5fh from the above timings.
(Refer to the Timing Charts for details.)

LCX009 (NTSC, PAL)

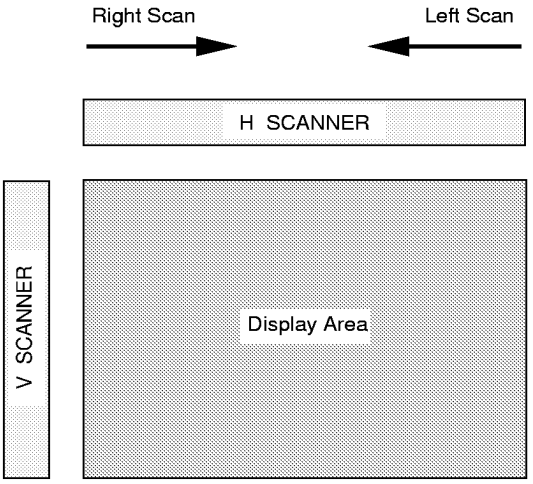
HP4	HP3	HP2	HP1	HST1 (NTSC/PAL)	HST2 (NTSC/PAL)
0	0	0	0	91fh (5.51/5.55µs)	93.5fh (5.66/5.70µs)
0	0	0	1	89fh	91.5fh
0	0	1	0	87fh	89.5fh
0	0	1	1	85fh	87.5fh
0	1	0	0	83fh	85.5fh
0	1	0	1	81fh	83.5fh
0	1	1	0	79fh	81.5fh
0	1	1	1	77fh	79.5fh
1	0	0	0	75fh (4.54/4.57µs)	77.5fh (4.69/4.72µs)
1	0	0	1	73fh	75.5fh
1	0	1	0	71fh	73.5fh
1	0	1	1	69fh	71.5fh
1	1	0	0	67fh	69.5fh
1	1	0	1	65fh	67.5fh
1	1	1	0	63fh	65.5fh
1	1	1	1	61fh (3.69/3.72µs)	63.5fh (3.84/3.87µs)

* The HST1 and 2 timing for odd lines is delayed or advanced 1.5fh from the above timings.
(Refer to the Timing Charts for details.)

Right/Left Inversion

The LCD panel is arranged in a delta pattern, where identical signal lines are 1.5-dot offset for juxtaposed lines. For this reason, a 1.5-bit offset is attached to the horizontal start pulse (HST) of the LCD between lines. HCK and SH are also 1.5-bit offset in a similar manner.

When the panel is driven with left scan, this offset relationship becomes inverted for even and odd lines. Moreover, since the dot arrangement is asymmetrical, the HST position is also changed. CXD2411R deals with this inversion as follows.



(1) When using single-panel LCDs

When the right/left inversed-identification pin (RGT) goes L, the relationship between odd and even lines in the HCK system output switches. In this case, use HST1 for the horizontal direction start pulse.

When RGT is H:

Right scan (Normal scan) mode is on. The right scan drive pulse is output by the timing generator and is supplied to the panel.

When RGT is L:

Left scan (Reverse scan) mode is on. The left scan drive pulse is output by the timing generator and is supplied to the panel.

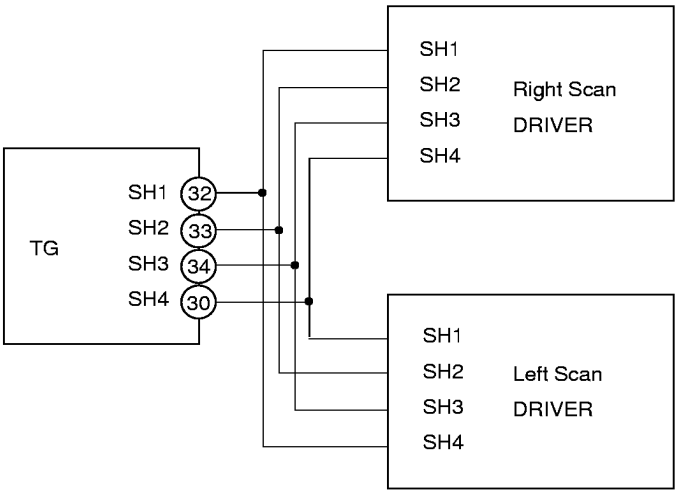
(2) When using three-panel LCDs

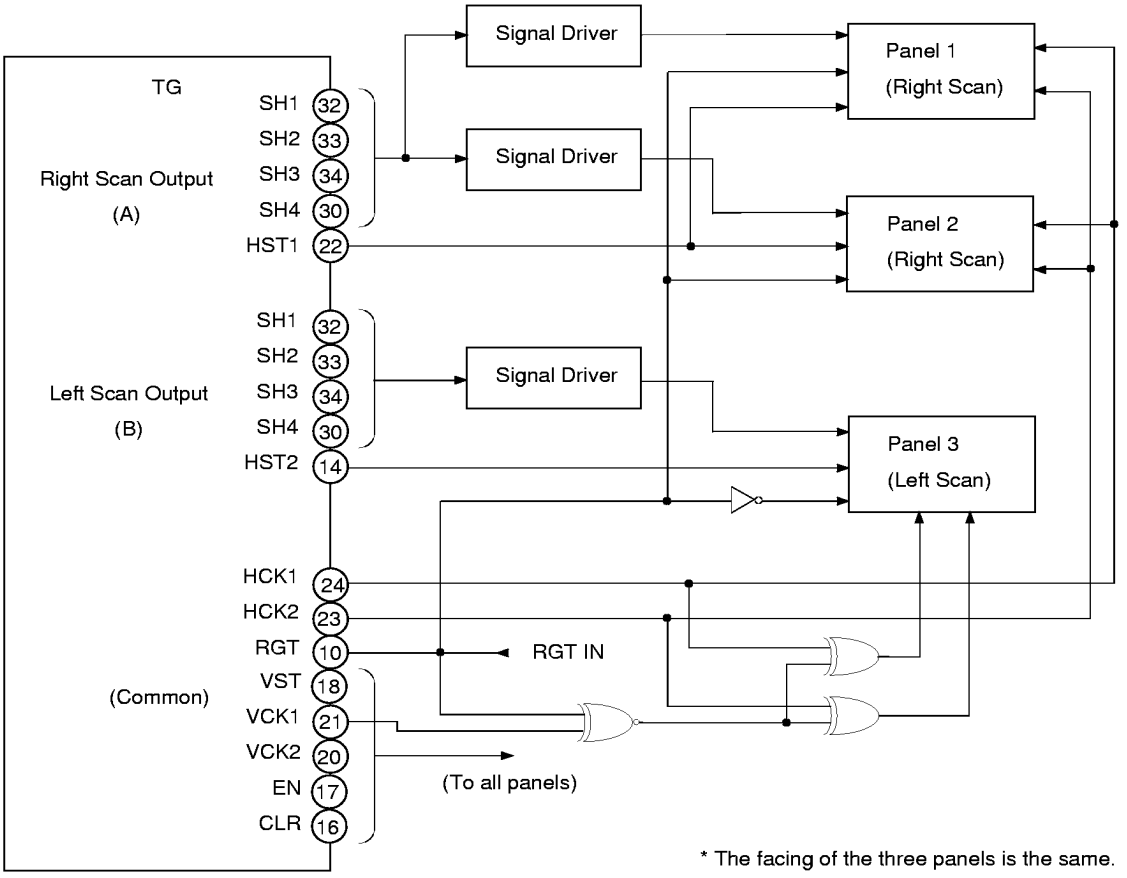
In order to be able to simultaneously drive three panels, with a mixture of right/left inversion on and off, output two pulses regarding HST pulse: HST1 for right scan and HST2 for left scan.

External measures are also taken for HCK1, 2 for left scan and RGT output to the panel. (See the circuit on the next page.)

Regarding SH, the wires to the SH1 and SH4 drivers are switched.

Application Circuit (Driving a Three-panel LCD)



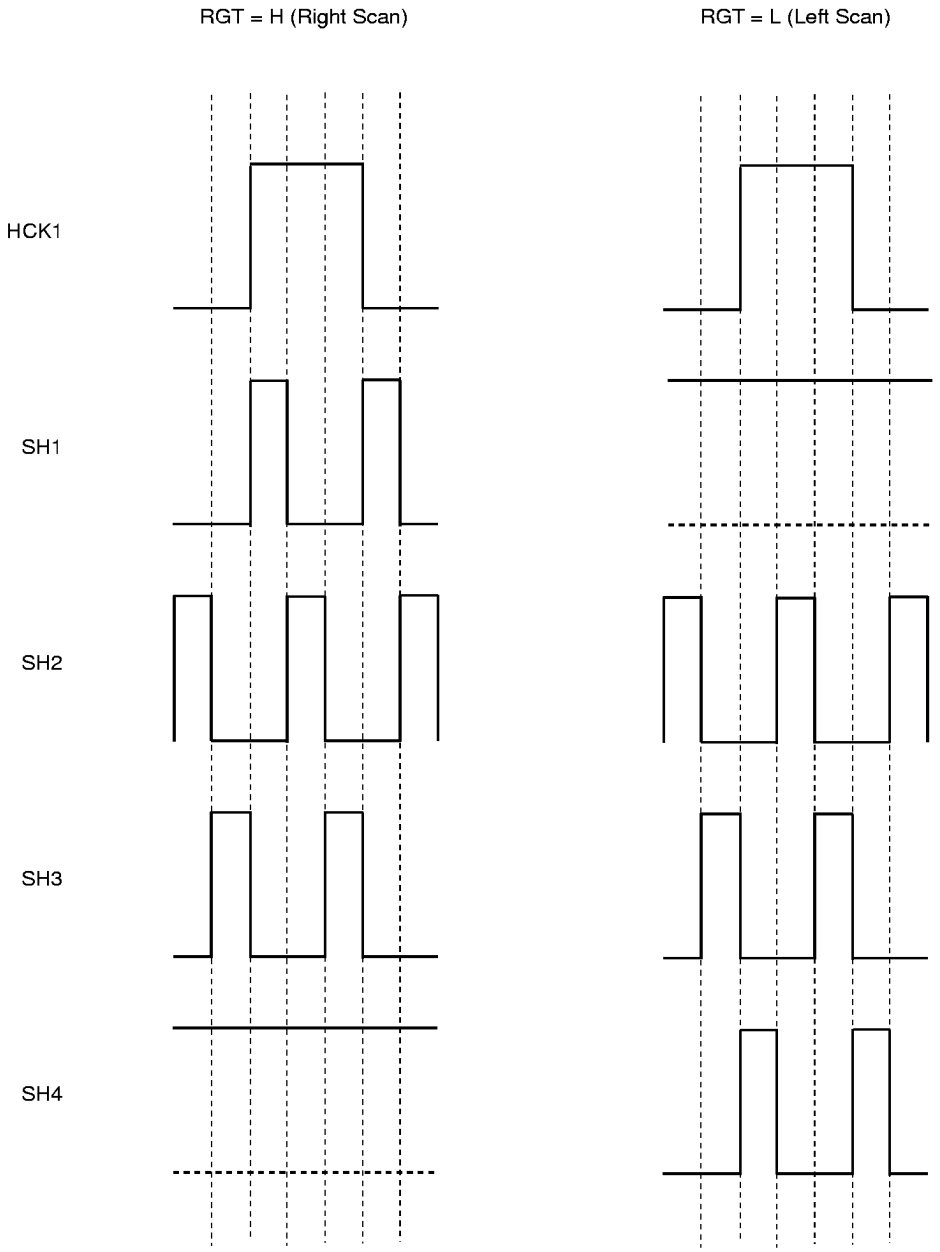


* The facing of the three panels is the same.

SH Pulse and HCK Phase Relationship

The phase relationship between the SH pulse and HCK changes when the unit is switched between right scan (Normal scan) and left scan (Reverse scan).

In the present timing, SH3 is the re-sampling pulse.



WIDE Mode

Setting the WIDE pin (Pin 4) to H shifts the unit to WIDE mode (supported only in the LCX009). In this mode, the aspect ratio is converted through pulse eliminator processing, allowing 16:9 quasi-WIDE display.

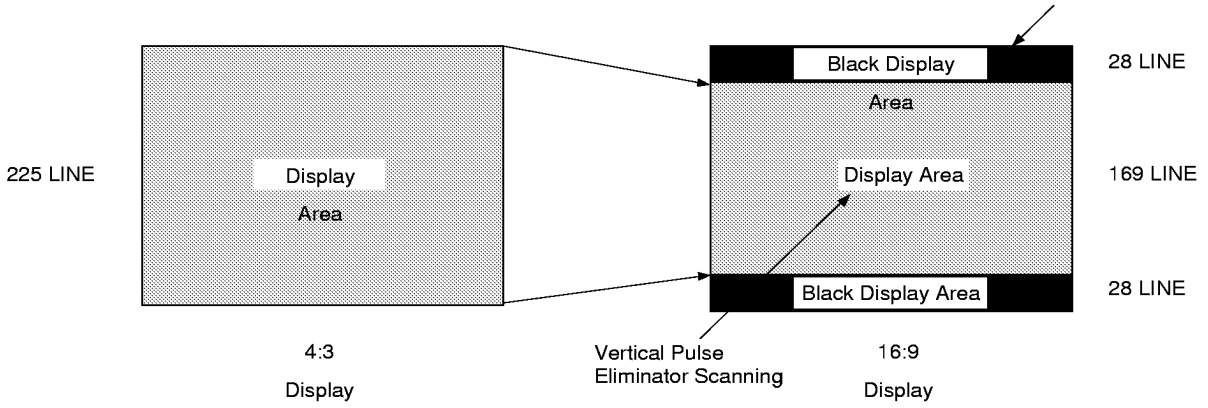
During WIDE mode, 1/4 and 1/2, 1/4 vertical pulse eliminator scanning of 1/4 for NTSC and 1/2 and 1/4 for PAL, are performed, and the video signal is compressed to achieve a 16:9 aspect ratio. In addition, in areas outside the display area, black is displayed by performing direction high-speed scanning.

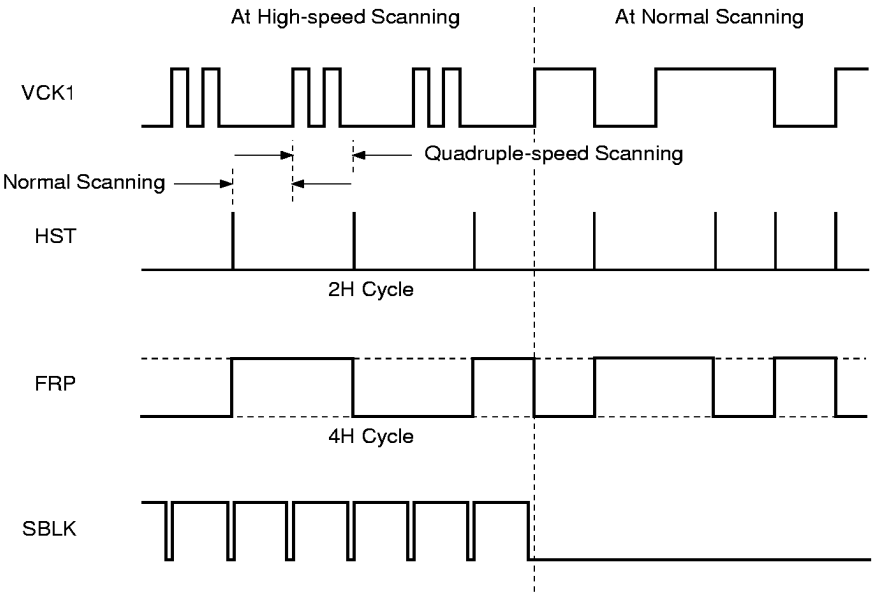
The timing during high-speed scanning is a 2H cycle pulse consisting of normal drive (1H) and quadruple-speed drive (1H) and black signals are written in 28 lines of the upper and lower side of this display area. During this time, FRP is changed to a 4H cycle, HST to a 2H cycle, and EN and CLR are not output.

In addition, the SBLK output, which is the black signal generation timing pulse; becomes H.

(For example, black display in the panel is permitted by connecting the black signal output SBLK to the external RGB input pin of the CXA1785R/AR.)

Refer to the attached sheets for detailed timing.

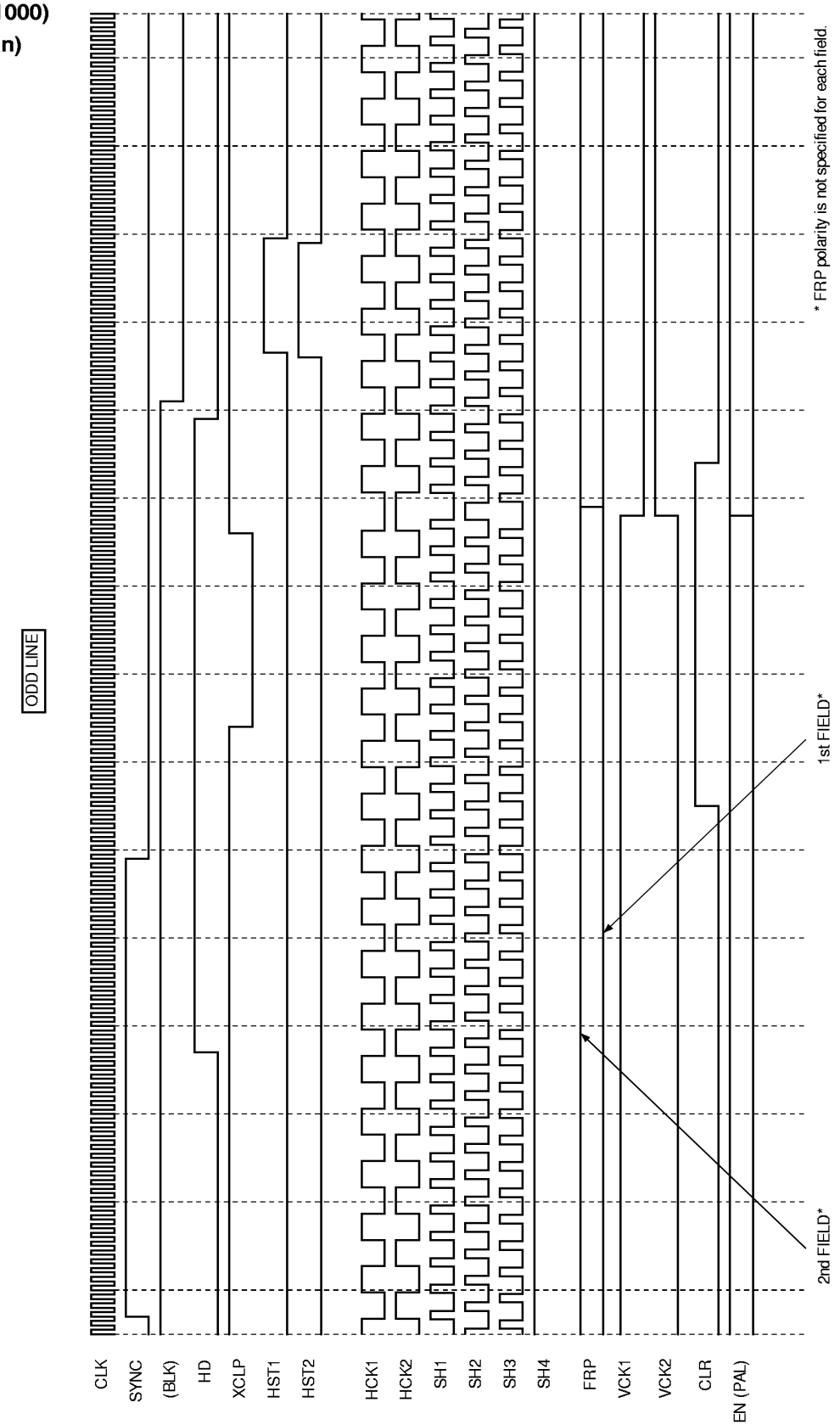




LCX005BK Horizontal Direction Timing Chart

NTSC, PAL (HPOS-1000)

RGT: H (Normal scan)

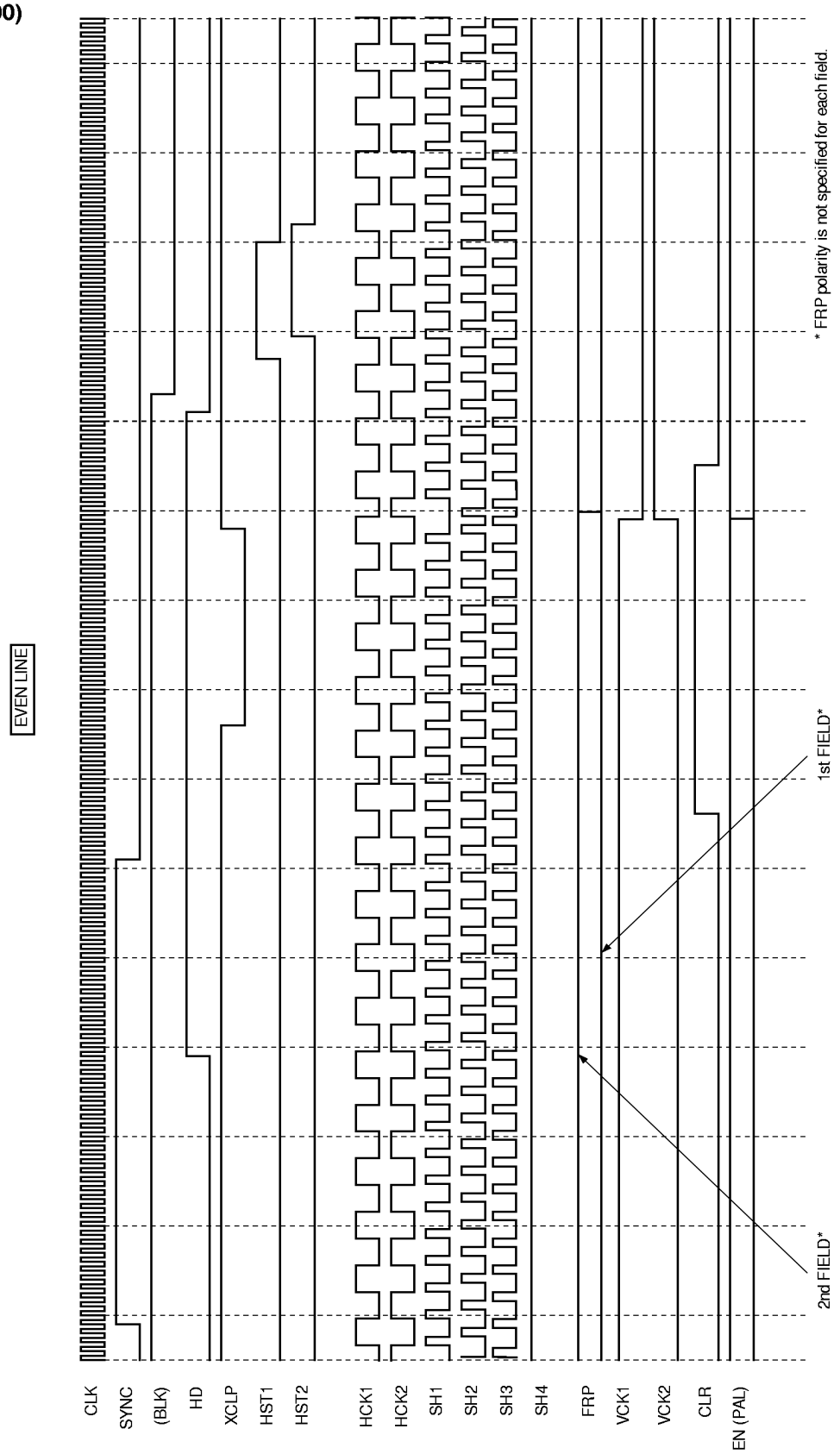


Note) Signals for the timing interval from input SYNC which change with HST according to horizontal start position settings (HP1 to HP4): HCK1, HCK2, SH1, SH2, SH3, FRP, VCK1, VCK2, CLR, EN
Constant signals regardless of the horizontal start position settings (HP1 to HP4): SYNC, HD, XCLP
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.

LCX005BK Horizontal Direction Timing Chart

NTSC, PAL (HPOS-1000)

RGT: H (Normal scan)

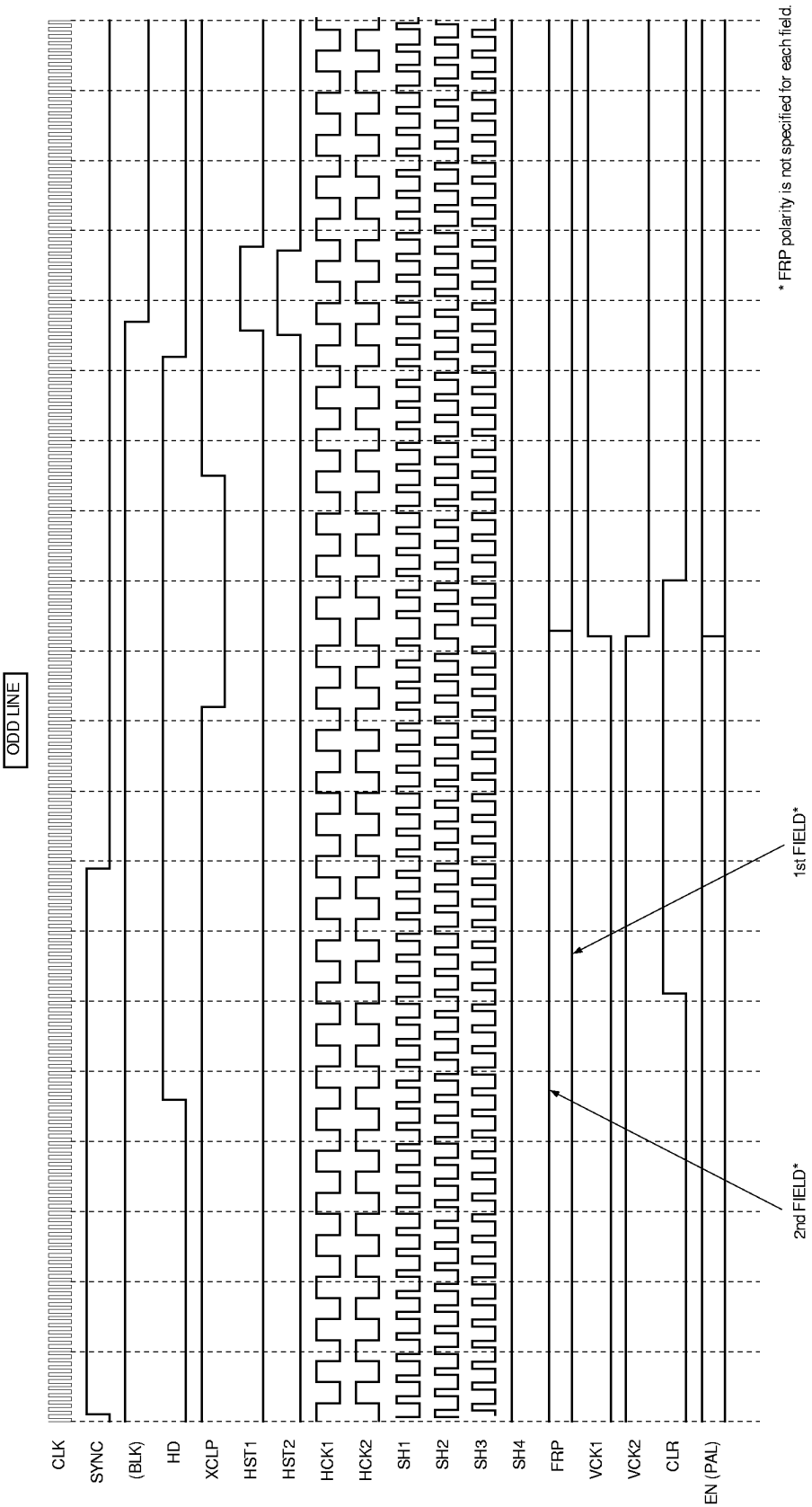


Note) Signals for the timing interval from input SYNC which change with HST according to horizontal start position settings (HP1 to HP4): HCK1, HCK2, SH1, SH2, SH3, FRP, VCK1, VCK2, CLR, EN
Constant signals regardless of the horizontal start position settings (HP1 to HP4): SYNC, HD, XCLP
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.

LCX009 Horizontal Direction Timing Chart

NTSC, PAL (HPOS-1000)

RGT: H (Normal scan)

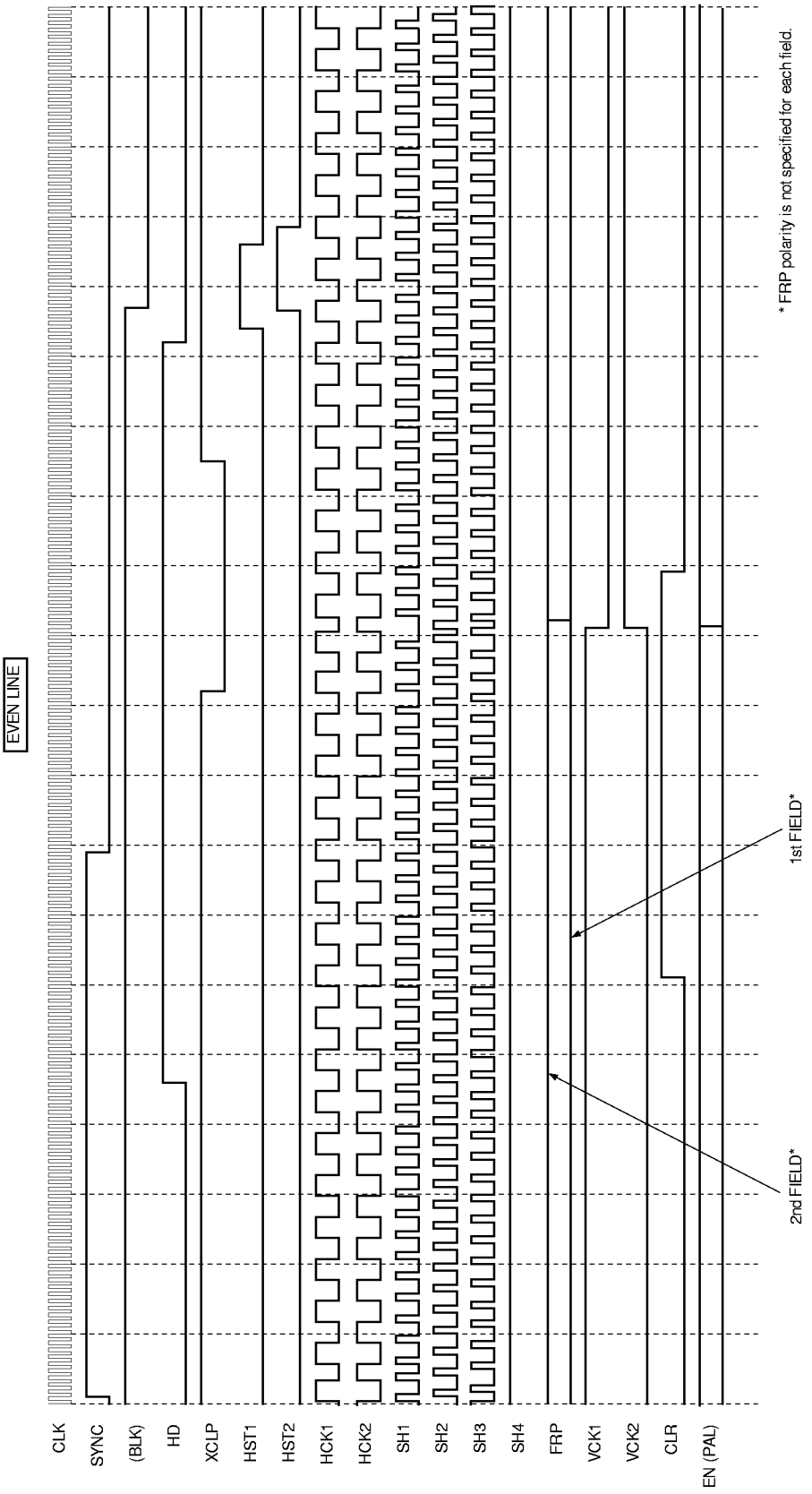


Note) Signals for the timing interval from input SYNC which change with HST according to horizontal start position settings (HP1 to HP4): HCK1, HCK2, SH1, SH2, SH3, SH4, FRP, VCK1, VCK2, CLR, EN
Constant signals regardless of the horizontal start position settings (HP1 to HP4): SYNC, HD, XCLP
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.

LCX009 Horizontal Direction Timing Chart

NTSC, PAL (HPOS-1000)

RGT: H (Normal scan)

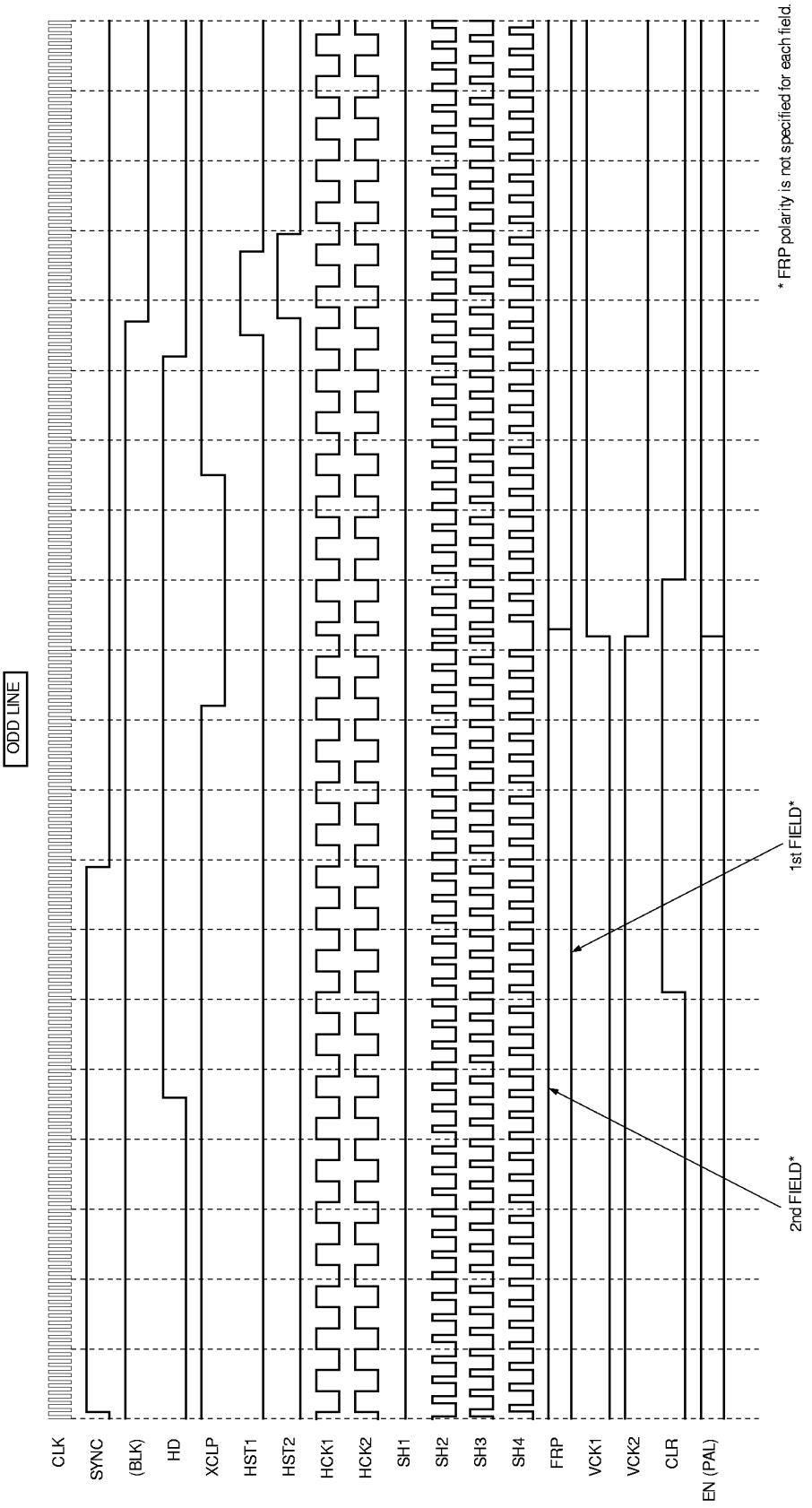


Note) Signals for the timing interval from input SYNC which change with HST according to horizontal start position settings (HP1 to HP4): HCK1, HCK2, SH1, SH2, SH3, SH4, FRP, VCK1, VCK2, CLR, EN
Constant signals regardless of the horizontal start position settings (HP1 to HP4): SYNC, HD, XCLP
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.

LCX005BK Horizontal Direction Timing Chart

NTSC, PAL (HPOS-1000)

RGT: L (Reverse scan)

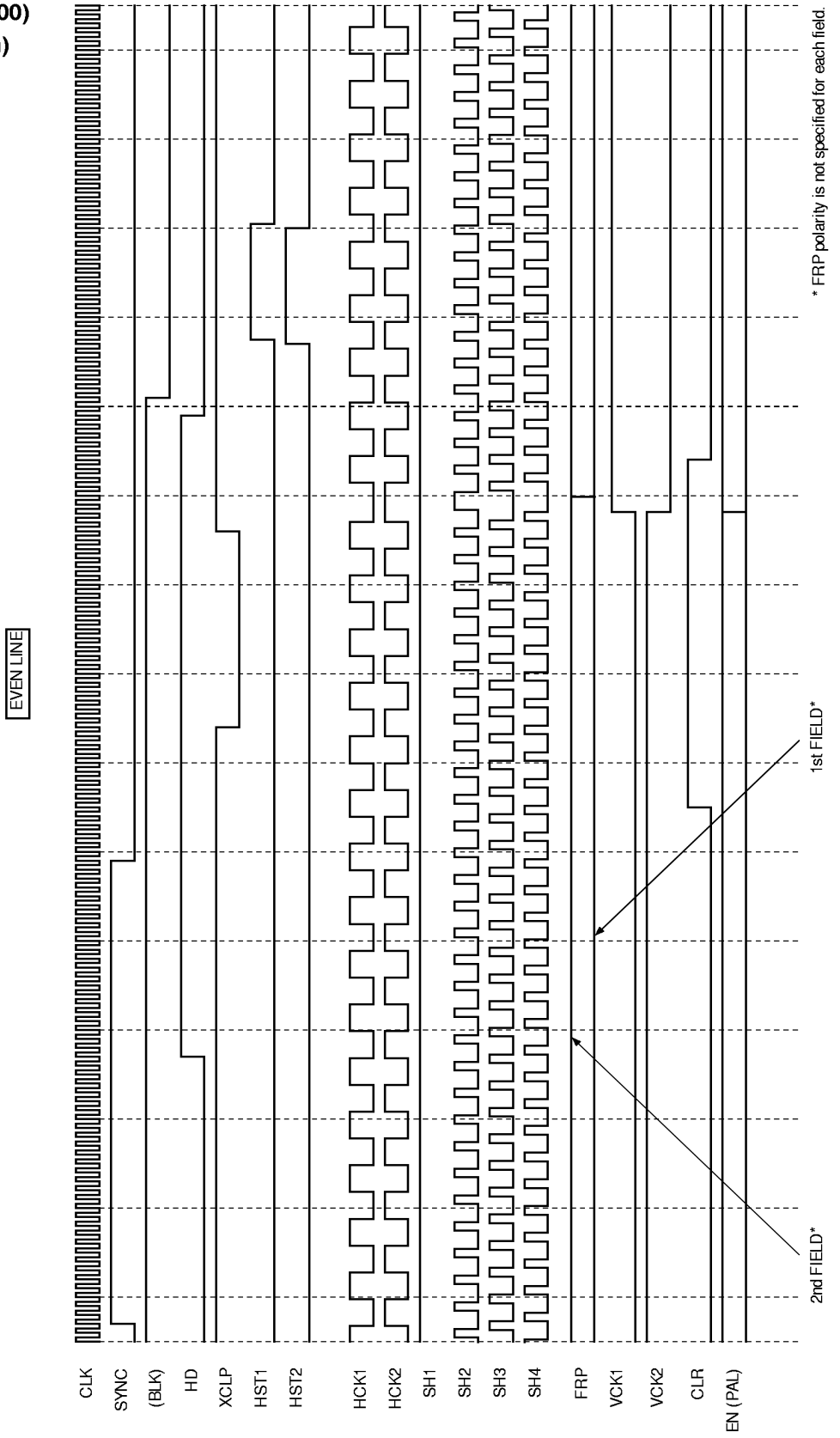


Note) Signals for the timing interval from input SYNC which change with HST according to horizontal start position settings (HP1 to HP4): HCK1, HCK2, SH1, SH2, SH3, SH4, FRP, VCK1, VCK2, CLR, EN
Constant signals regardless of the horizontal start position settings (HP1 to HP4): SYNC, HD, XCLP
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.

LCX005BK Horizontal Timing Chart

NTSC, PAL (HPOS-1000)

RGT: L (Reverse scan)

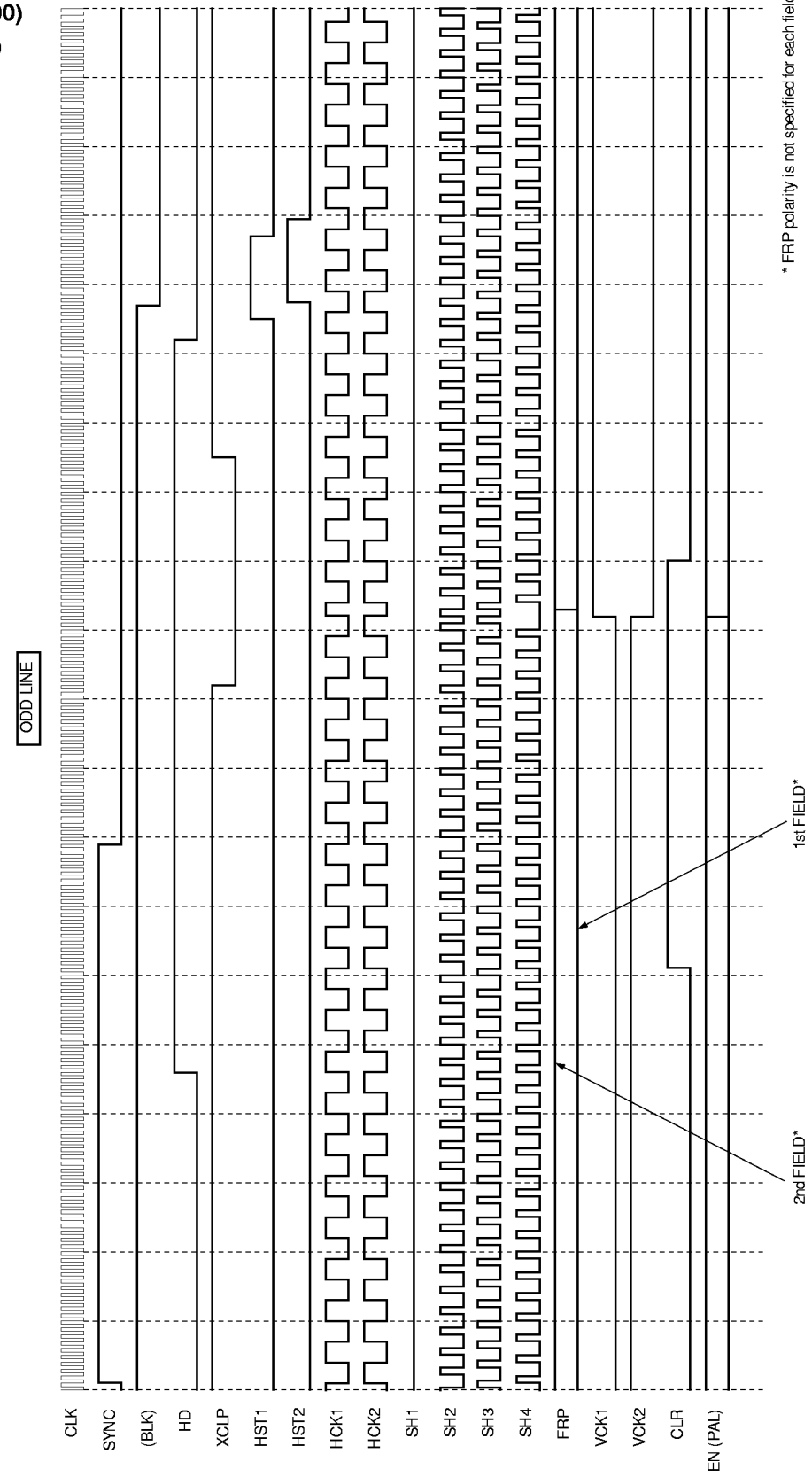


Note) Signals for the timing interval from input SYNC which change with HST according to horizontal start position settings (HP1 to HP4): HCK1, HCK2, SH1, SH2, SH3, FRP, VCK1, VCK2, CLR, EN
Constant signals regardless of the horizontal start position settings (HP1 to HP4): SYNC, HD, XCLP
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.

LCX009 Horizontal Direction Timing Chart

NTSC, PAL (HPOS-1000)

RGT: L (Reverse scan)

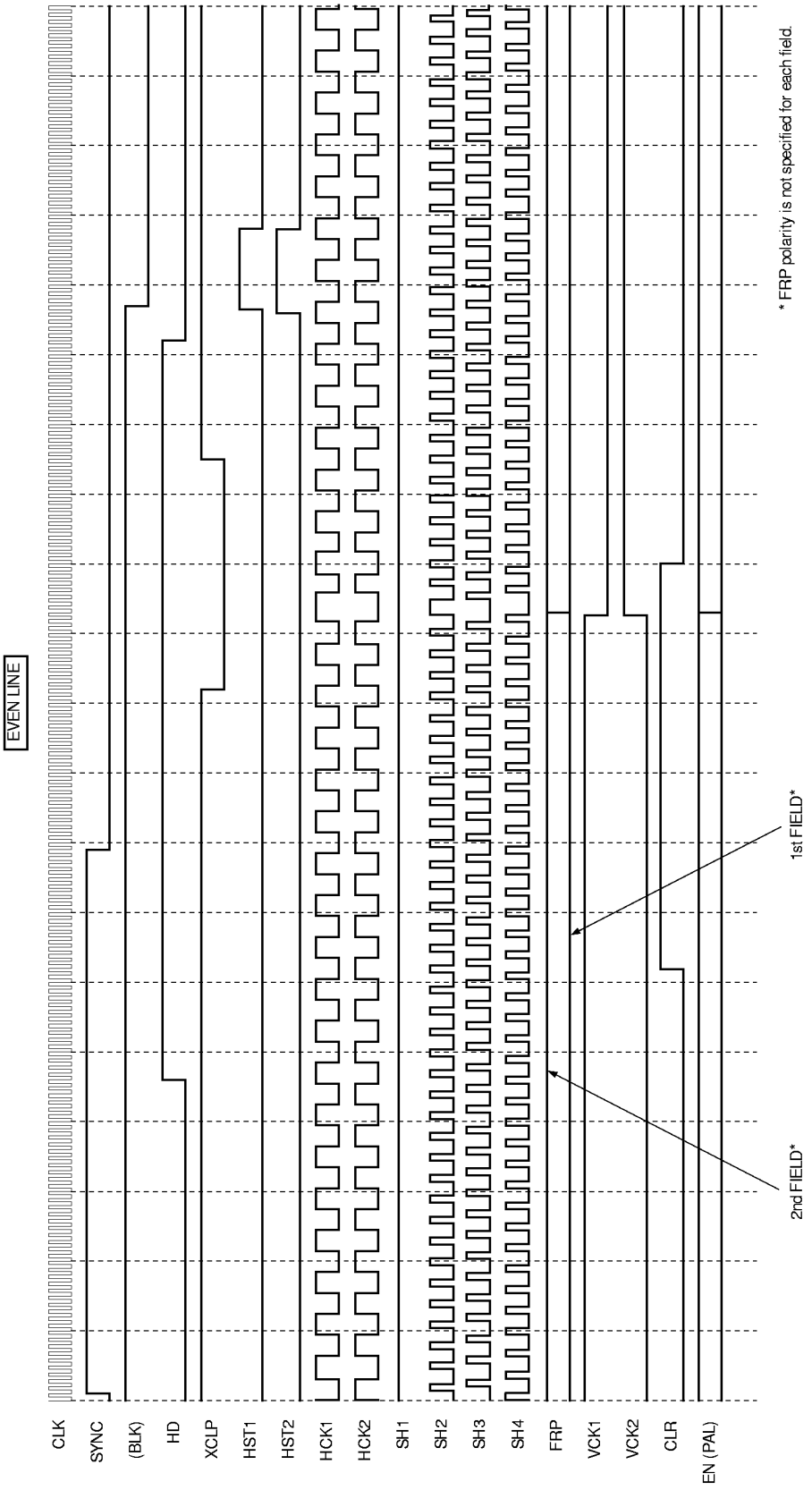


Note) Signals for the timing interval from input SYNC which change with HST according to horizontal start position settings (HP1 to HP4): HCK1, HCK2, SH1, SH2, SH3, SH4, FRP, VCK1, VCK2, CLR, EN
Constant signals regardless of the horizontal start position settings (HP1 to HP4): SYNC, HD, XCLP
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.

LCX009 Horizontal Direction Timing Chart

NTSC, PAL (HPOS-1000)

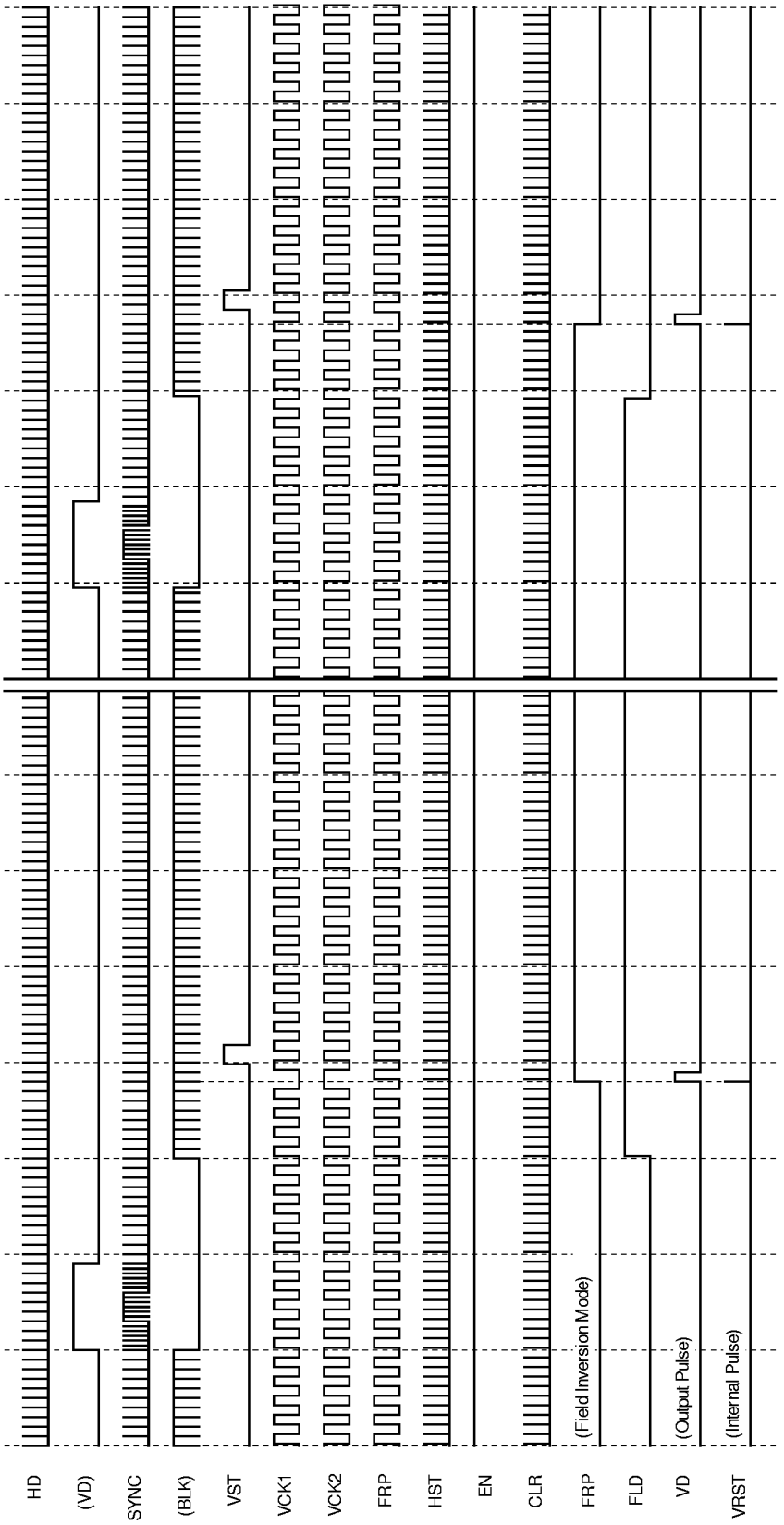
RGT: L (Reverse scan)



Note) Signals for the timing interval from input SYNC which change with HST according to horizontal start position settings (HP1 to HP4): HCK1, HCK2, SH1, SH2, SH3, SH4, FRP, VCK1, VCK2, CLR, EN
Constant signals regardless of the horizontal start position settings (HP1 to HP4): SYNC, HD, XCLP
The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.

LCX005BK Vertical Direction Output Pulse

NTSC Vertical Direction Timing Chart

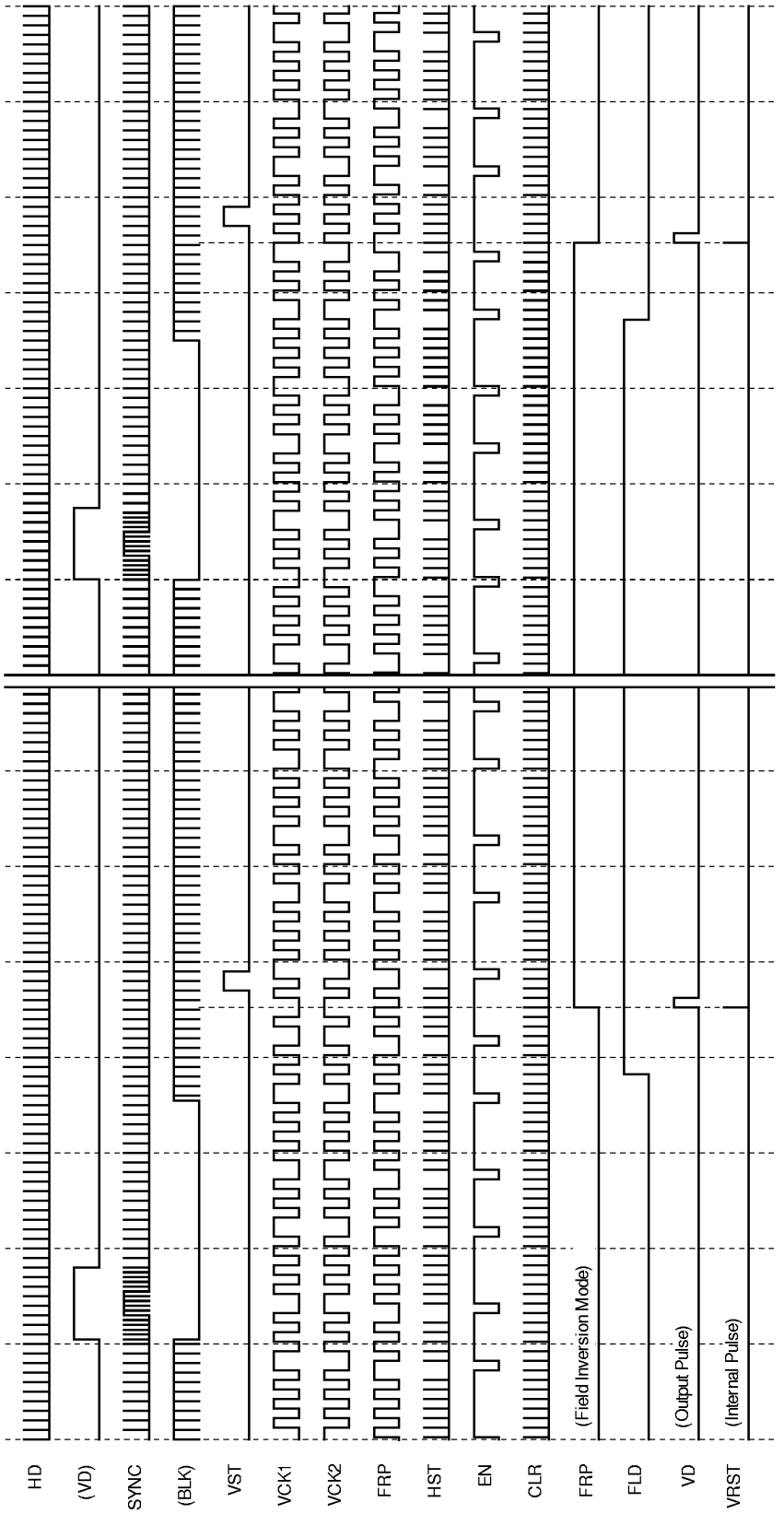


* FRP polarity is not specified for each field.

Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

LCX005BK Vertical Direction Output Pulse

PAL Vertical Direction Timing Chart

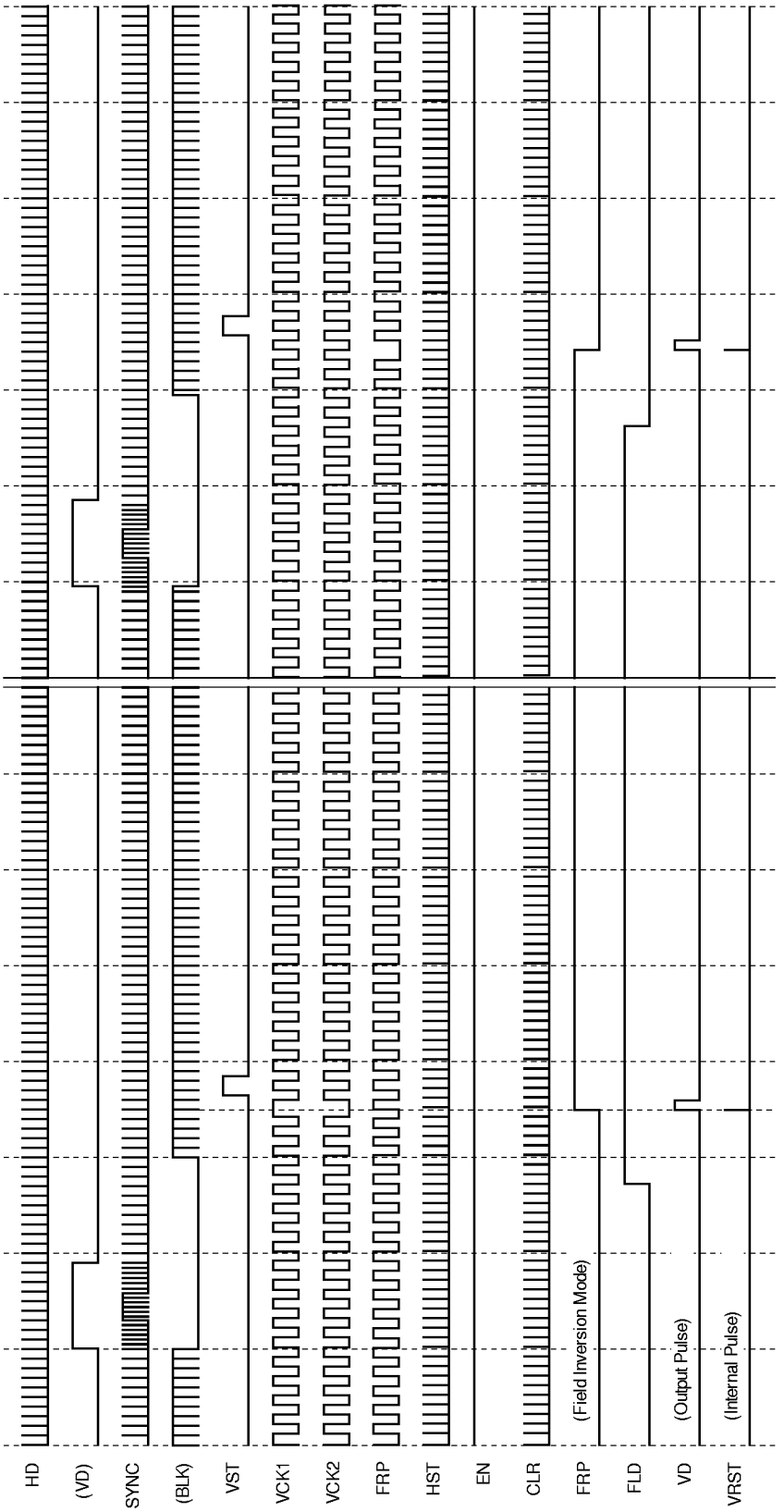


* FRP polarity is not specified for each field.

Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

LCX009 Vertical Direction Output Pulse

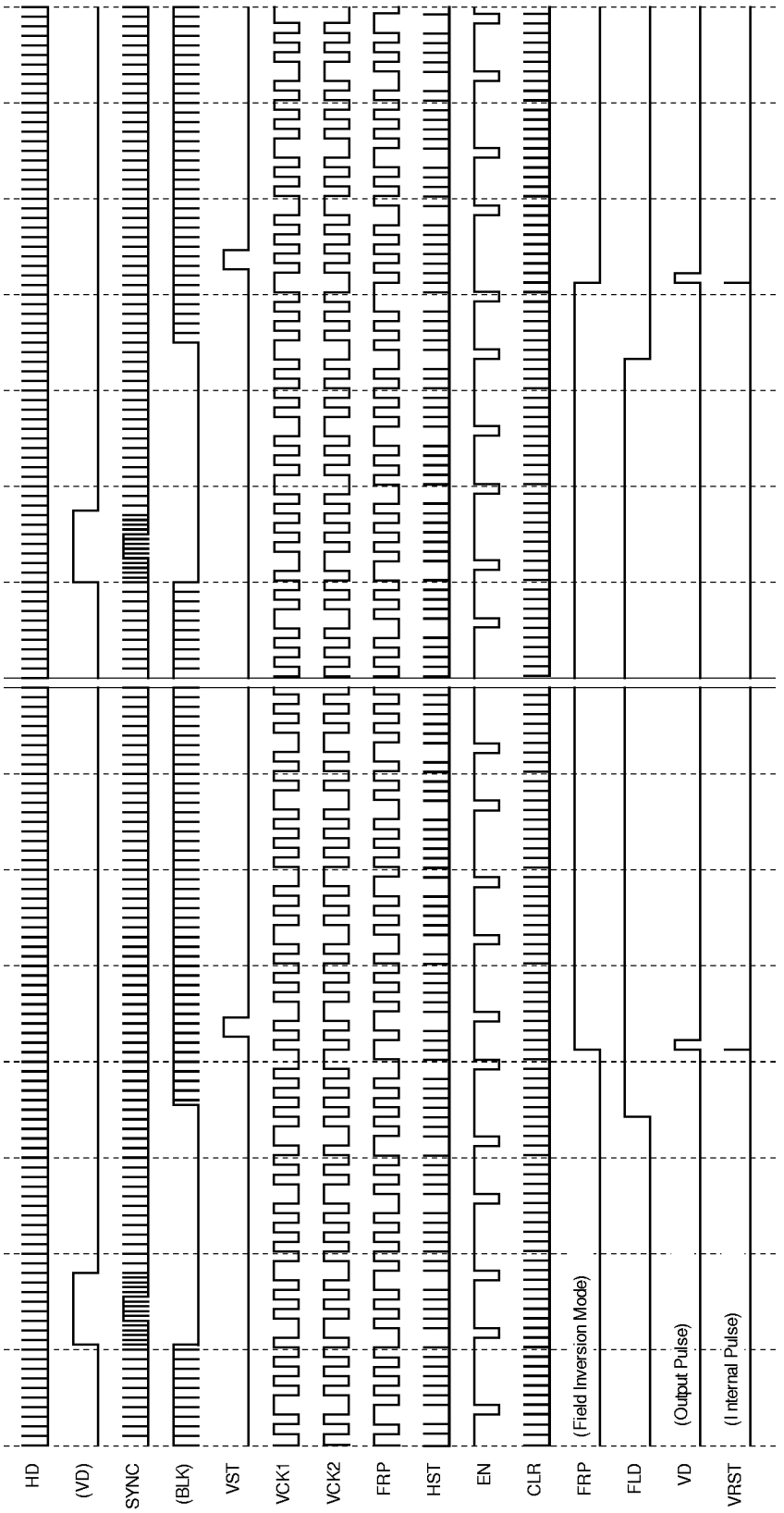
NTSC Vertical Direction Timing Chart



Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

LCX009 Vertical Direction Output Pulse

PAL Vertical Direction Timing Chart

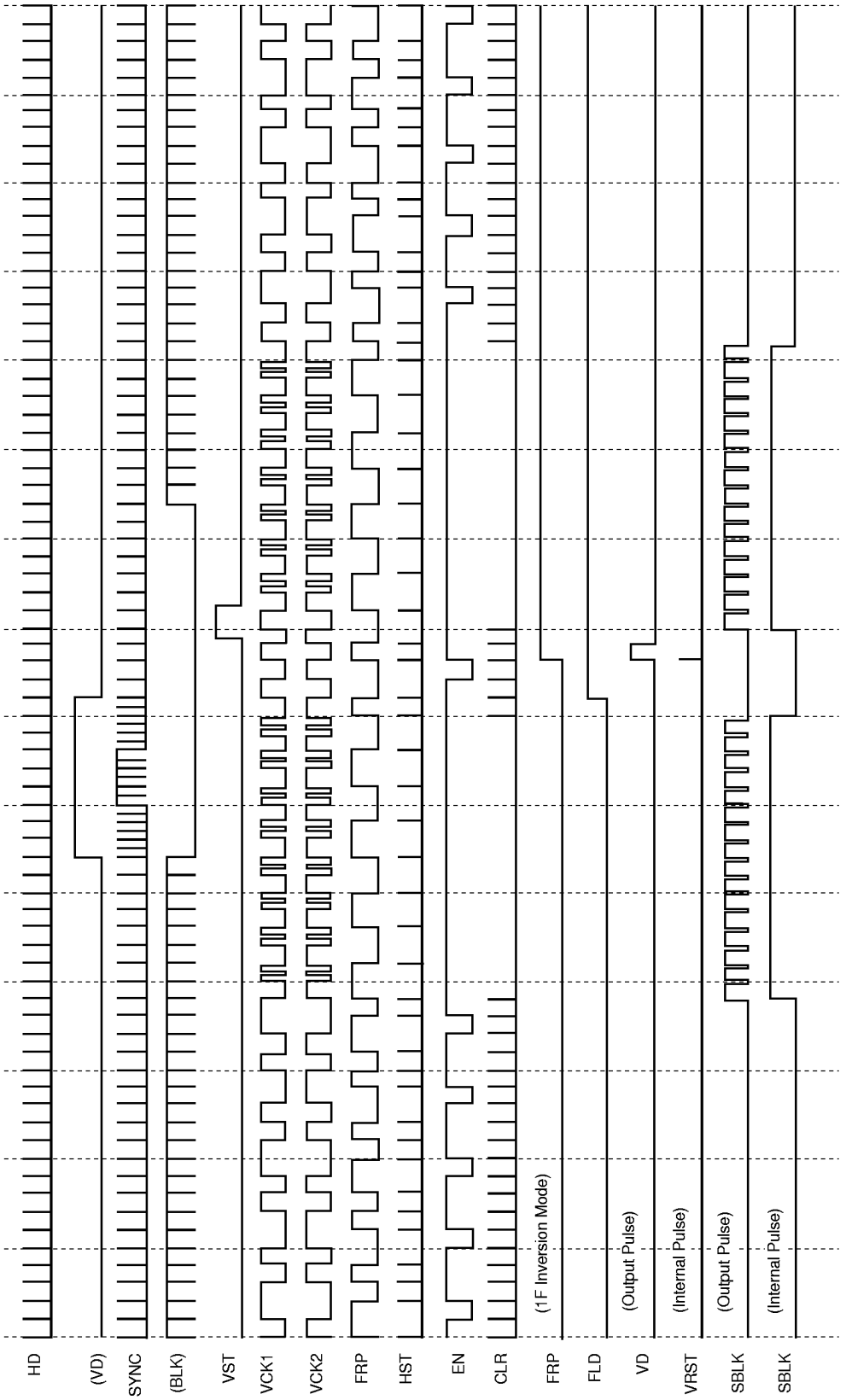


* FRP polarity is not specified for each field.

Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

LCX009 Vertical Direction Output Pulse

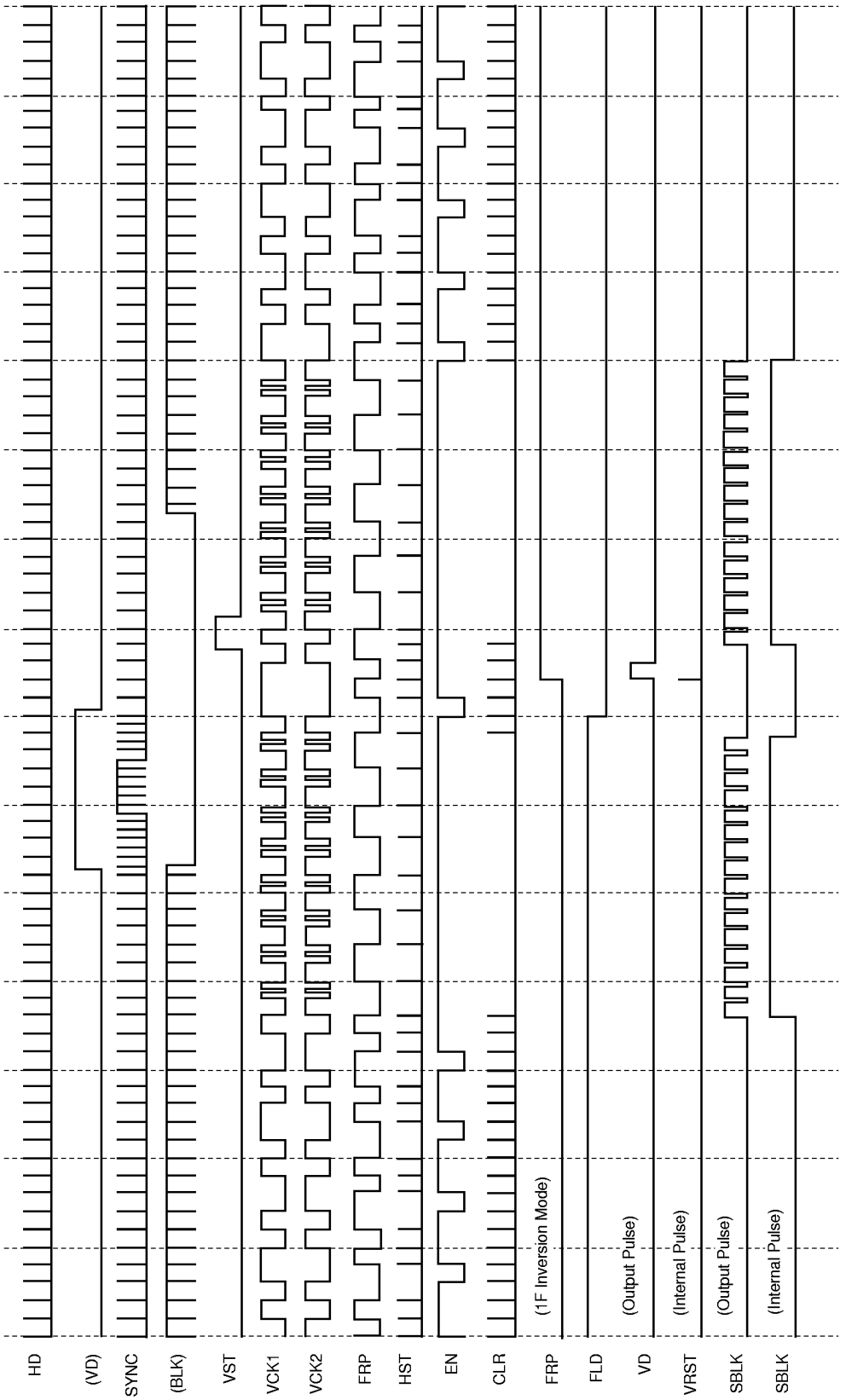
NTSC WIDE Vertical Direction Timing Chart



Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

LCX009 Vertical Direction Output Pulse

NTSC WIDE Vertical Direction Timing Chart

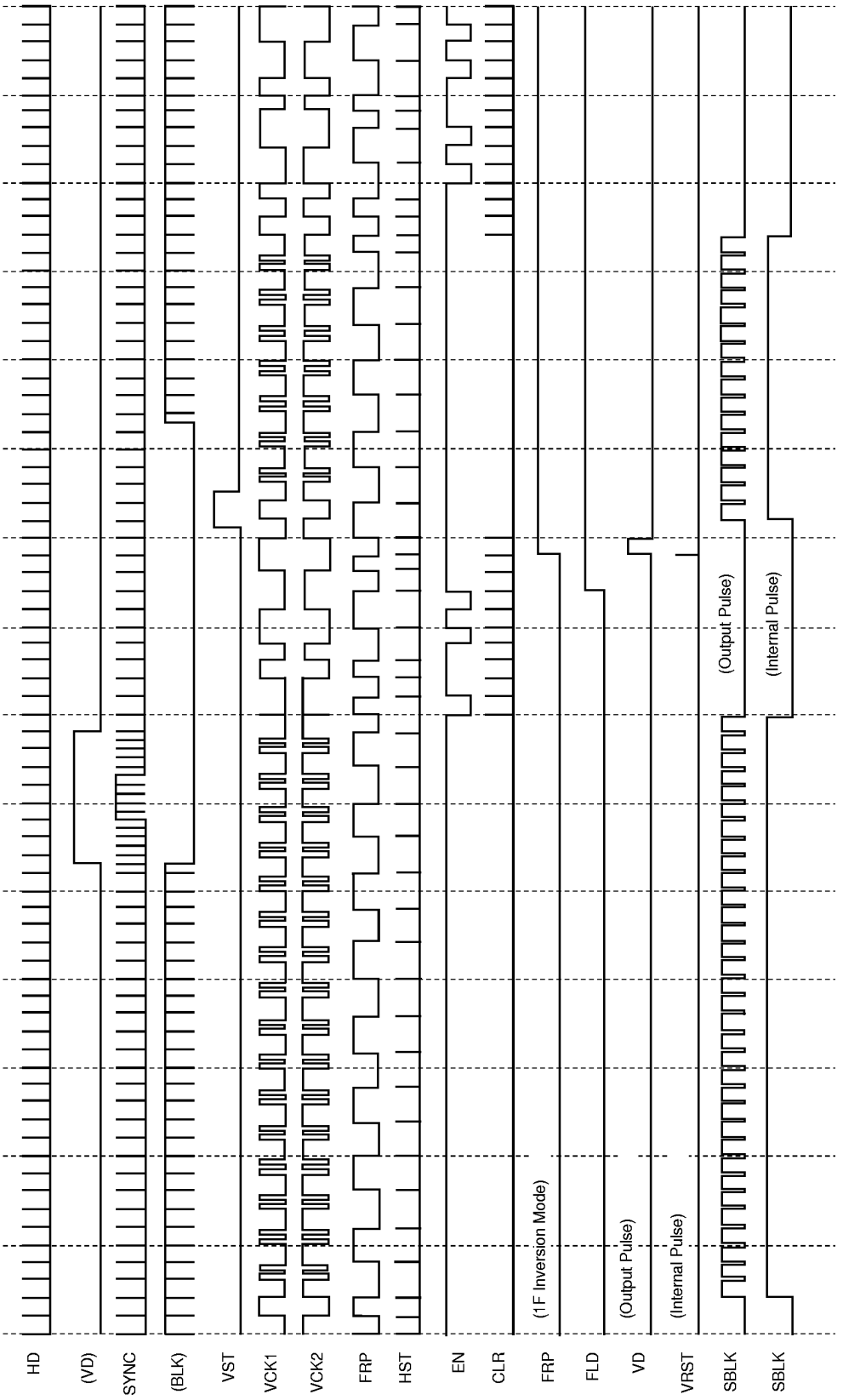


* FRP polarity is not specified for each field.

Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

LCX009 Vertical Direction Output Pulse

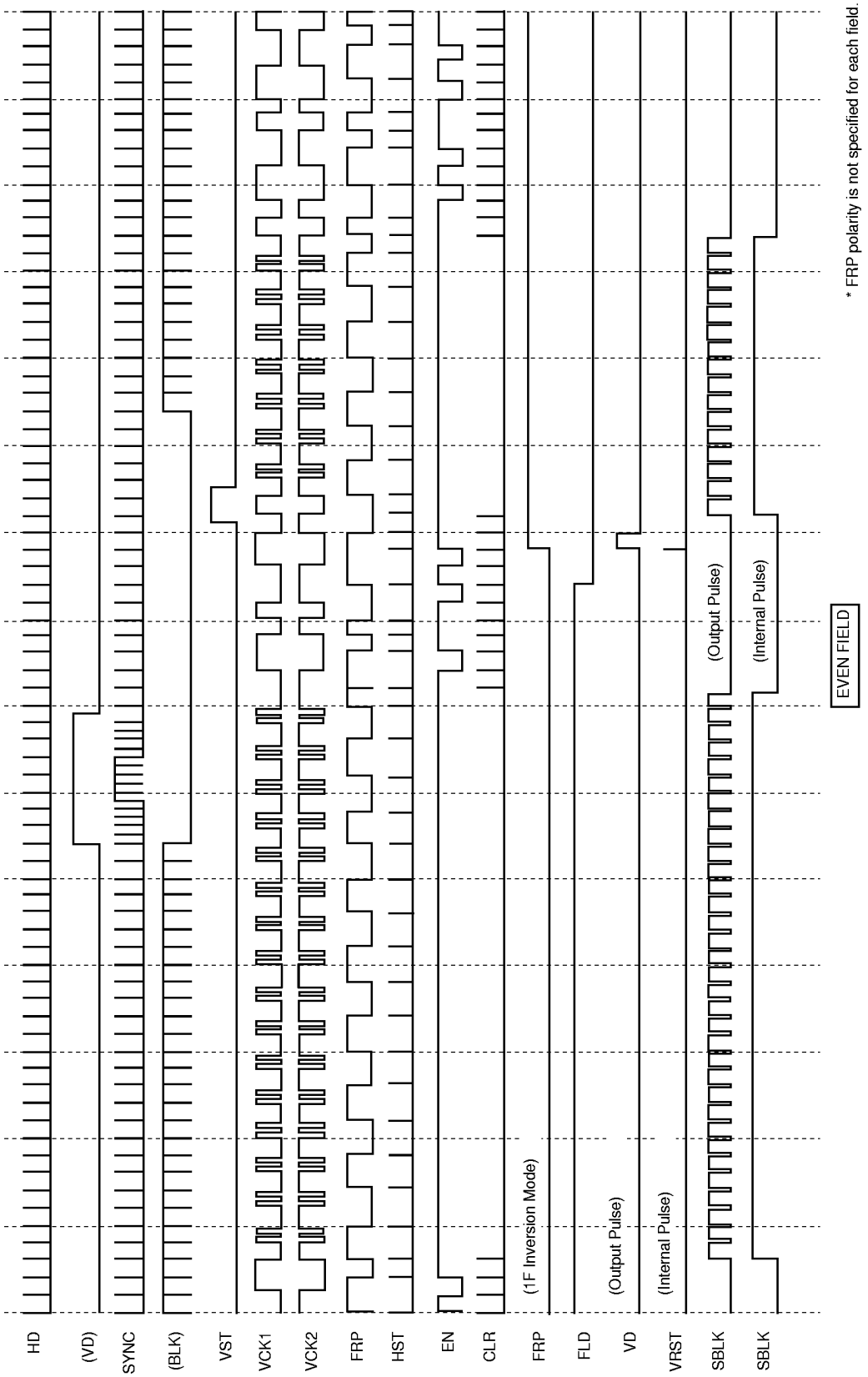
PAL WIDE Vertical Direction Timing Chart



Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

LCX009 Vertical Direction Output Pulse

PAL WIDE Vertical Direction Timing Chart



Note) The second and fourth rows of the timing chart "VD" and "BLK" are pulses indicated as a reference and are not pulses output from pins.

AC Driving for No Signal

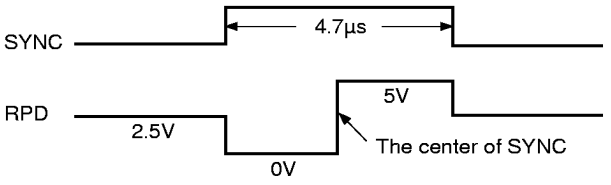
HST1, HST2, HCK1, HCK2, FRP, VCK1, VCK2, XCLP, HD, VD, and VST are made to run free so that the LCD panel is AC driven even when there is no composite sync from the SYNC pin.

During this time, the PLL counter is made to run free because the HSYNC separation circuit stops. In addition, the auxiliary V counter is used to create the reference pulse for generating VD and VST because the VSYNC separation circuit is also stopped.

The period of the V counter is designed to be 269H for NTSC and 321H for PAL. When there is no VSYNC during 303H (NTSC) or 360H (PAL), the free running state is assumed.

The RPD is kept at high impedance when there is no signal.

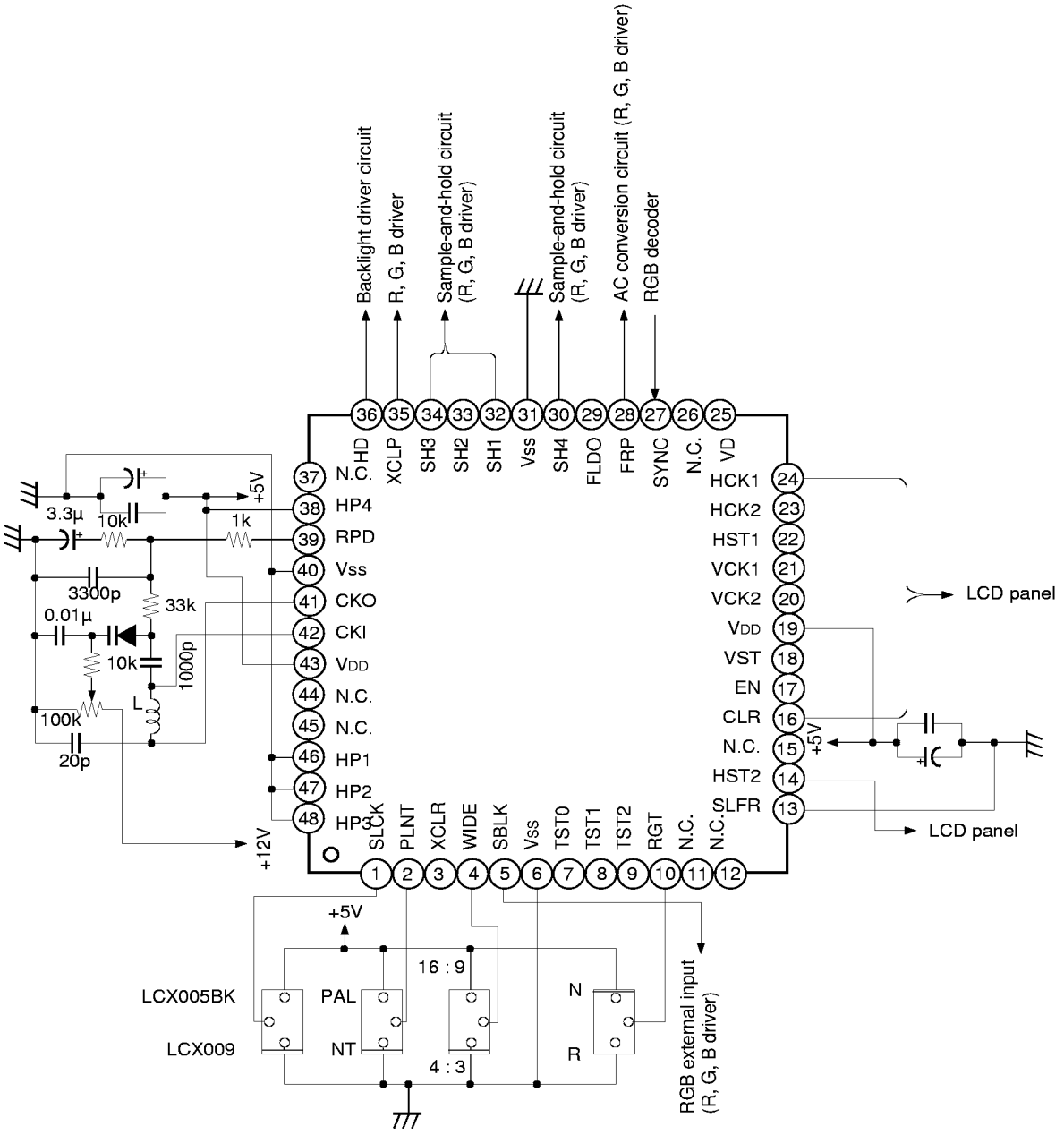
AFC Circuit (702/1050fh Generation)



A fully synchronized AFC circuit is built in. PLL error detection signal is generated at the following timing.

The phase comparison output of the entire bottom of SYNC and the internal H counter becomes RPD. RPD output is converted to DC error with the lag-lead filter, and then it changes the vari-cap capacitance and the oscillating frequency is stabilized at 702fh in LCX005BK/1050fh in LCX009.

Application Circuit



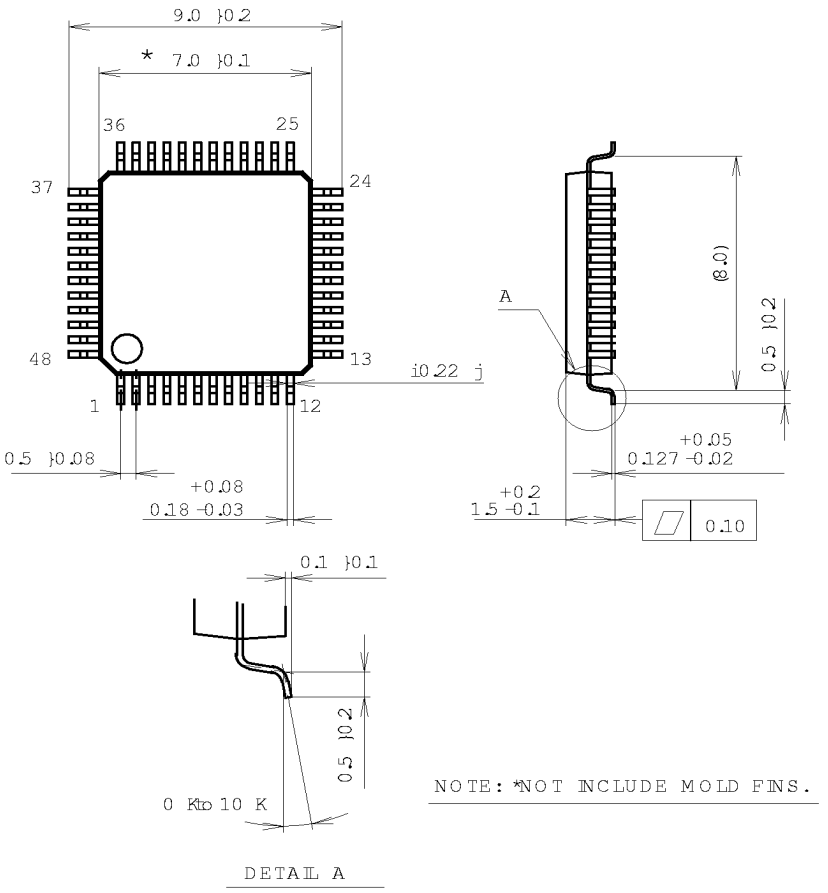
Reference examples of L value: when using LCX009 4.7µH
when using LCX005BK 10µH

Recommended varicap: 1T369 (SONY)

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

48PIN LQFP (PLASTIC)



DETAIL A

NOTE: *NOT INCLUDE MOLD FINS.

SONY CODE	LQFP-48P-L01
EIAJ CODE	*QFP048-P-0707-A
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2 g