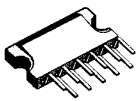
DUAL INJECTION DRIVER

ADVANCE DATA

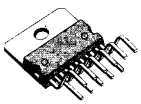
- WIDE SUPPLY RANGE (5.5 - 40V)
- VERY LOW ON RESISTANCE (TYP. 300mΩ)
- OUTPUT CURRENT UP TO 2A
- HIGH PERFORMANCE DIAGNOSTIC
- UNDERVOLTAGE DISABLE
- OVERVOLTAGE AND SHORT CIRCUIT PROTECTION
- CMOS COMPATIBLE CONTROL INPUTS

MULTIPOWER BCD TECHNOLOGY



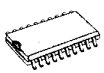
Clipwatt 11

ORDERING NUMBER: L9360



Multiwatt 11

ORDERING NUMBER: L9360M



SO20L (12+4+4)

ORDERING NUMBER: L9360D

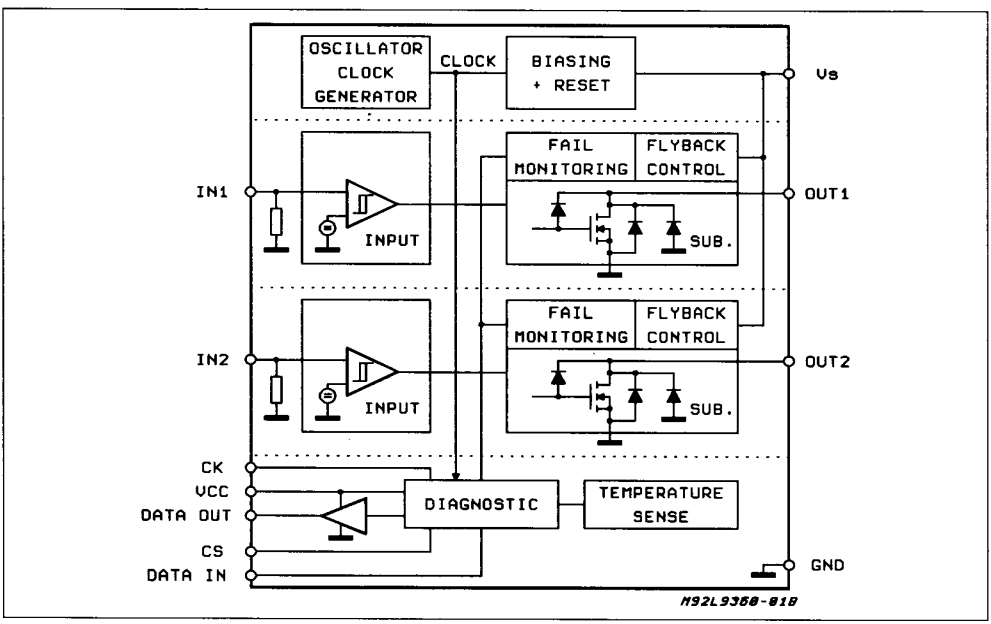
DESCRIPTION

The L9360 is a monolithic dual low side smart Power switch with DMOS power outputs, rated for operation in automotive environment.

It is intended to drive injectors connected to the positive battery voltage.

Thanks to its CMOS compatibility and its high performance diagnostic it is very well suited for handshake data with a microcontroller.

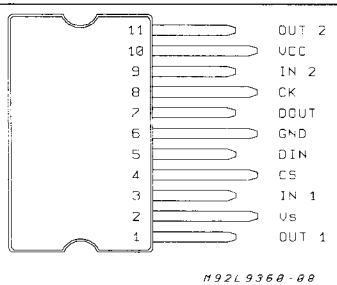
BLOCK DIAGRAM



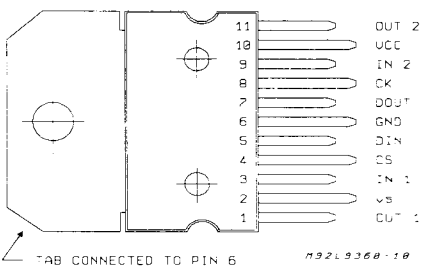
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	40	V
I_{OCL}	Output Clamping Current	2	A
E_{OCL}	Output Dissipated Energy	TBD	J
I_{or}	Reverse Output Current (Pd ≤ 1W)	-2	A
V_{CC}	Stabilized Logic Supply Voltage	7	V
V_{CCrev}	Reverse Stabilized Logic Supply Voltage	-0,3	V
V_I	Input Voltage	7	V
V_{Irev}	Reverse Input Voltage	-0.3	V
V_{Id}	Data Pin Voltage	7	V
V_{Idrev}	Reverse Data Pin Voltage	-0.3	V
T_{stg}	Storage Temperature	-55 to 150	°C
$T_{j\text{-}case}$	Operating Junction Temperature	-40 to 150	°C
$T_{j\text{-}SD}$	Thermal Overload Detection Temperature	150 to 165	°C
$T_{j\text{-}SDH}$	Thermal Threshold Hysteresis	Typ. 20	°C
V_{ESD}	Protected According to MIL883C		

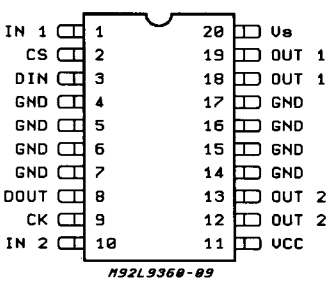
PIN CONNECTIONS (top view)



Clipwatt 11



Mulwatt 11



SO20 12+4+4

THERMAL DATA

Symbol	Parameter		Max. Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	**Clipwatt 11**	70	°C/W
		Multiwatt 11	60	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction to pins	**SO20L**	20	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance junction-case	**Multiwatt 11**	3	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 5.5 to 25V, V_{CC} = 4.5 to 5.5V, T_j =–40 to 150°C unless otherwise specified; the voltage and currents are assumed positive, when oriented in the arrows direction shown in the application circuit diagram)

OUTPUT STAGE (EACH CHANNEL)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{DSON}	On Resistance	VI = HIGH, V_S >7V V_I = HIGH, V_S <7V		300 400	600 1000	mΩ mΩ
I_{OSC}	Out Short Circuit Current		2	3	4	A
V_{OCL}	Output Clamping Voltage	I_O = 0.2mA	70	80	100	V
V_{ODG}	Output Internal Voltage	V_I = LOW, see Fig. 5	0.45V_S	0.5V_S	0.55VS	V
$R1_{ODG}$	Internal Output Resistance	V_I = LOW, see Fig. 5		20		KΩ

SUPPLY VOLTAGE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CCDC}	DC Supply Current (VCC)			1	2	mA
I_S	Supply Current (V_S)	V_{I1} = V_{I2} = LOW		4	7	mA
		V_{I1} = V_{I2} = HIGH		16	25	mA
		V_{I1} = V_{I2} = HIGH; V_S= 14V		10		mA

CONTROL INPUTS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Level	VCC = 5V		2	1.5	V
V_{IH}	Input HIGH Level	V_{CC} = 5V	3.5	3.2		V
V_{ITH}	Input Threshold Hysteresis		1	1.2	1.6	V
td_{ON}	Input to Out Delay Time	R_L = 14Ω; V_S= 14V		1.5	10	µs
t_{OR}	Output Rise Time	R_L = 14Ω; V_S= 14V		3.5	10	µs
t_{dOFF}	Input to Out Delay Time	R_L = 14Ω; V_S= 14V		2	10	µs
t_{OF}	Output Fall Time	R_L = 14Ω; V_S= 14V		1.2	10	µs
R_{IN}	Input Resistance		100	200	300	KΩ

DIAGNOSTIC & PROTECTIONS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CSL}	CS Input LOW Level	V_{CC} = 5V		2	1.5	V
V_{OIL}	Data Input LOW Level	V_{CC} = 5V		2	1.5	V
V_{CKL}	CK Input LOW Level	V_{CC} = 5V		2	1.5	V
V_{CSH}	CS Input HIGH Level	V_{CC} = 5V	3.5	3.2		V
V_{DIH}	Data Input HIGH Level	V_{CC} = 5V	3.5	3.2		V
V_{CKH}	CK Input HIGH Level	V_{CC} = 5V	3.5	3.2		V
V_{DOL}	Data Output LOW	I_{DO} = 1mA		0.2	0.5	V
V_{DOH}	Data Output HIGH	I_{DO} = -200µA; V_{CC} = 5V	4			V
I_{DOL}	Data Output Leakage Current	V_{DO} = V_{CC}		1	10	µA
R_{LOL}	External Recognized Resistance for Open Load Detection	See fig. 5		10		KΩ
V_{OED}	Output Excessive Drop Thresh	See fig. 5	2	2.5		V
R_{OSG}	Output Resistance to GND for Short to GND Detection	See fig. 5		5		KΩ
t_{DOSG}	Output Short to GND Switch OFF			50	150	µs
t_{ES}	Error Recognition Time for the Stochastic Error	See fig. 4		5		µs
t_S	Time for Error Recognized	See fig. 4		50	150	µs
f_{OSG}	Internal Oscillator Frequency			500		KHz
f_{CLK}	External Clock Frequency				1	MHz

CIRCUIT DESCRIPTION

The device is realized in the BCD100 technology which combines CMOS logic, bipolar components and as output stages DMOS transistors which can withstands 100V drain-source voltage.

Via the CMOS compatible inputs (IN1, IN2) the power DMOS can be switched ON and OFF independently from each other. All functions of the device are guaranteed between 5.5V and 40V supply voltage. Between 5.5 to to 7V supply voltage the typical drain-source resistance increases from 250mΩ to 500mΩ typ. With this limitation a charge pump could be avoided.

For V_S below 5.5V the device can be disabled. Both outputs are switched OFF independently from the input status. The data output is switched to tristate. In the undervoltage mode (V_S < 5.5V) a possible failure status was reset. Below 3V the chip functions are not defined. The device is protected against short circuit to supply but not protected against thermal overload due to security reason. Only via the diagnostic the system is informed about a thermal overload and the other possible failure modes which are described separately. A quasi digital filter avoids that short time stochastic failures are stored in the diagnostic register.

When a short circuit to the supply is recognized and stored in the diagnostic register the output transistor is switched OFF. The output can be switched ON again only via a new input pulse.

The device needs a second supply voltage (V_{CC}) which comes normally from the same supply as for the µC.

This voltage supplies the logic and avoides problems whith logic level disturbances.

Figure 1: Two Chip Solution To Drive Four Valves: Parallel Data Out

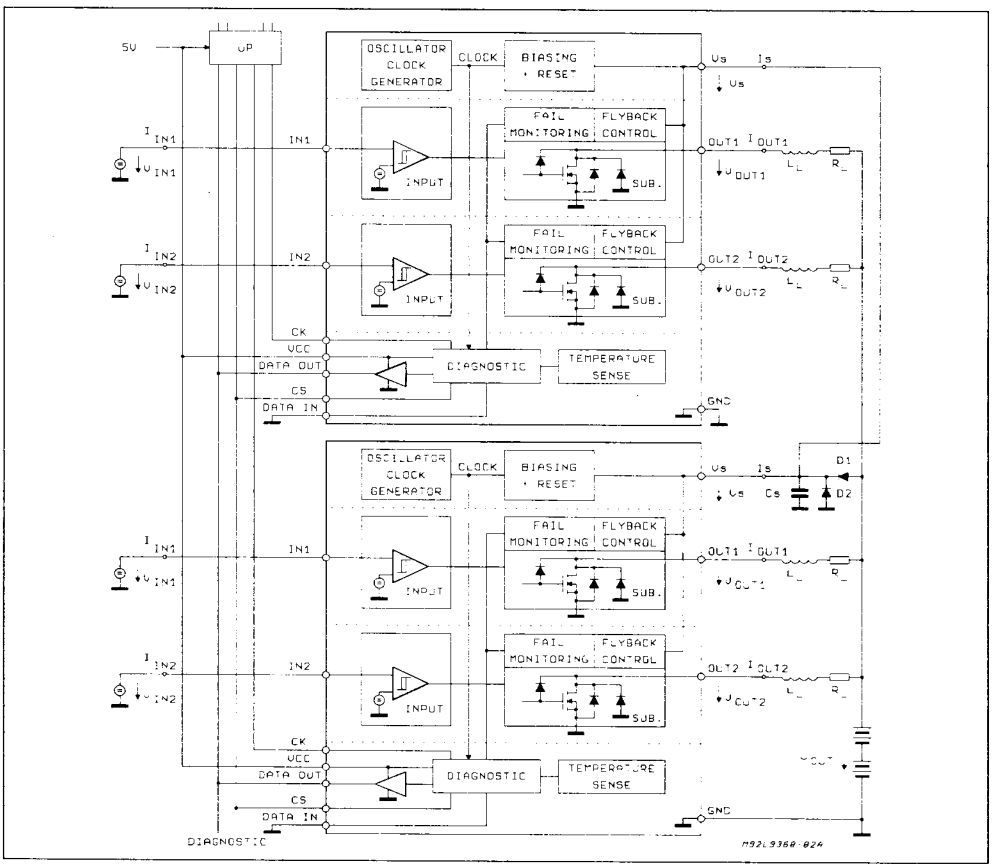
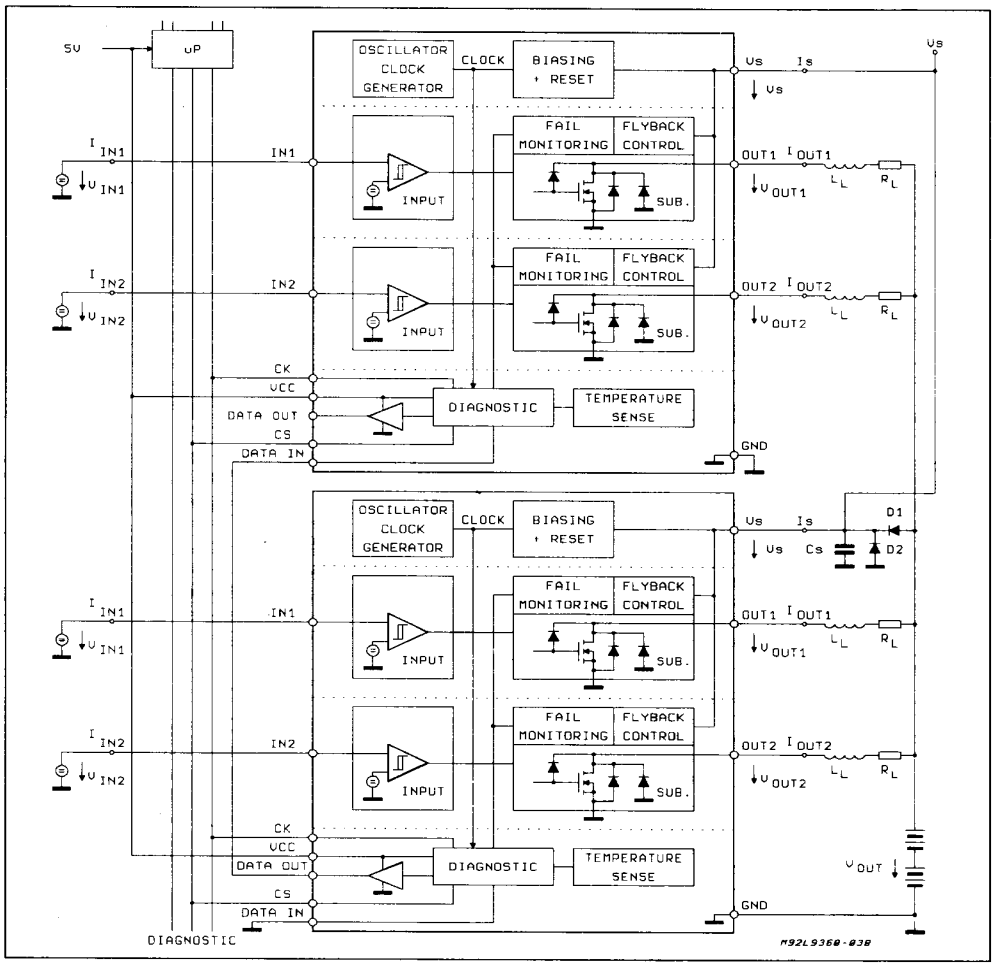


Figure 2; Two Chip Solution To Drive Four Valves: Serial Data Out



DIAGNOSIS

The diagnosis is able to detect the following states:

- OUTPUT SHORT-CIRCUIT TO BATTERY (SUPPLY VOLTAGE)
- OUTPUT SHORT-CIRCUIT TO GROUND
- OPEN LOAD
- THERMAL OVERLOAD

READING OF THE DIAGNOSIS REGISTER

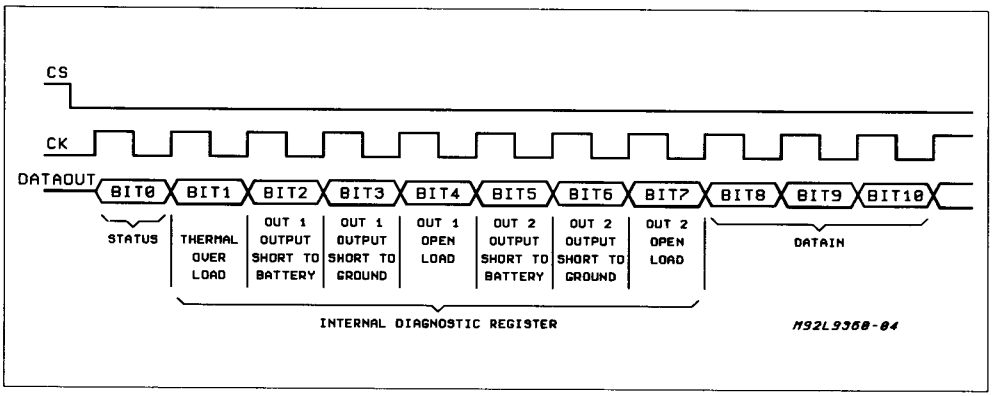
A low signal at the chip select CS-input and a positive edge of the clock signal at CK-input starts the reading of the diagnosis register.

The serial diagnosis register (Ref. to figure 3) is loaded synchronously with CK-signal at DATAOUT and new data fed through DATAIN as long as CS is "LOW".

After the nineth clock cycle the first DATAIN information is present at DATAOUT. The STATUS BIT 0 is "HIGH if one diagnosis register is set or the DATAIN-input is "HIGH", hence the presence of a failure can be detected by BIT 0.

The positive edge at CS clears the diagnosis register. During reading the diagnosis register (CS = "LOW") the single bits cannot be changed.

Figure 3: Serial Diagnostic



CASCADING OF SEVERAL INJECTOR DRIVERS

The possibility is given to read the diagnosis registers of several injector drivers via one diagnosis bus. Additionally the user can choose between two versions.

1. (figure 1):

The CK and DATAOUT terminals of the injector drivers are connected in parallel to the diagnosis bus. Each IC is provided with a separate CS-wire. The DATAIN-input is connected to GND.

2. (figure 2)

The CK and CS terminals are connected to the parallel diagnosis bus. The data line is connected in series through the terminals DATAIN and DATAOUT or each single IC. The DATAIN input of the first IC must be connected to GND.

The first version allow to read the desired diagnosis register immediately after the CS-signal is applied. in the other version all diagnosis registers have to be read one after the other whereby only a 3-wire bus is sufficient. In the other case each IC needs a separate CS-lead to the processor.

FAILURE DETECTION

Except the overtemperature signal all failure signals are filtered before setting the corresponding BIT in the diagnosis register.

The filter checks whether the failure signal is present during three times running the measure cycle within Ts. Spikes shorter than t_{ES} are ignored.

THERMAL OVERLOAD

If the chip exceeds T_{JSB} the "thermal overload"-BIT is set. Because the transistors are not switched off the element can be thermally destroyed if the control does not set the IN1 and IN2 inputs to "LOW".

OUTPUT SHOTR-CIRCUIT TO BATTERY (BIT2/5)

The output currents $I_{O1/2}$ are internally limited to 3A (typ).If the output current reaches the current limit the power DMOS leaves the resistive region and changes to the saturation region.

Consequently the drain source voltage increases and after reaching of typ. 2V the "output-short-circuit to battery" BIT is set and the power DMOS are switched off.

Repetitive control of IN_1 and IN_2 inputs (low-high sequence) switches on the DMOS again. But the bit in the diagnosis register is not resetted.

Figure 4

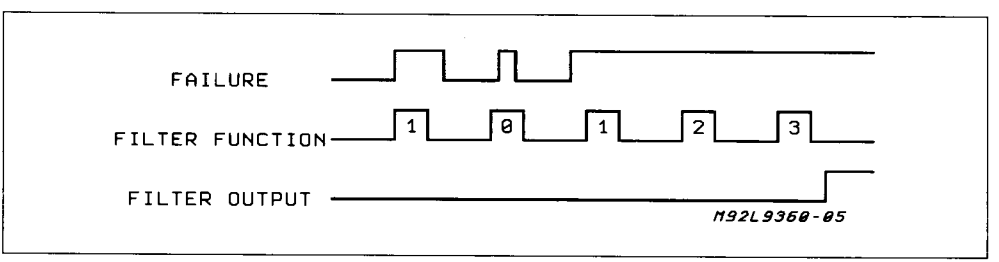
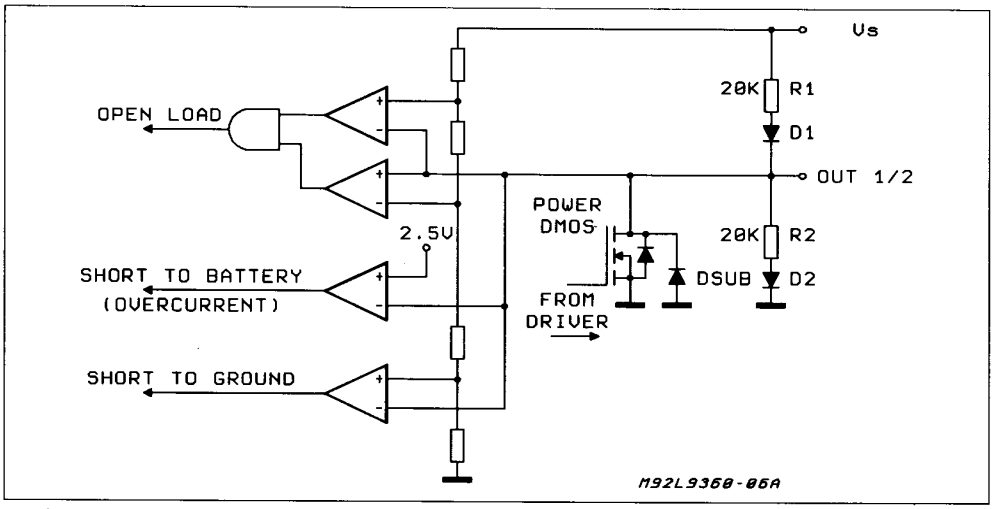


Figure 5: Principle Of Internal Diagnostic Detection



OUTPUT SHORT-CIRCUIT TO GND (BIT3/6) AND OPEN LOAD (BIT4/9).

In case of the switched off power DMOS the internal 20K resistors R_1 and R_2 divide the output voltage to half the supply voltage without load (fig.5).

A window comparator detects the output voltage and sets the "open load" BIT if the voltage deviates more than +/-0.25V_S from 0.5V_S. But if the output voltage decreases below 0.16V_S the "output short circuit to ground" BIT is set.

Figure 6: Diagnostic Detection Voltage Range