SONY

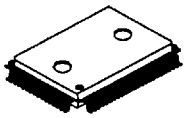
CXD2526AQ/AR

Audio Skip Guard Memory Controller

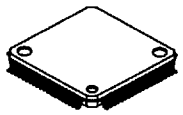
Description

The CXD2526AQ/AR is a memory controller designed for audio skip guard memory control configurations in MD systems. The CXD2526AQ/AR controls MD-format signal encoding/decoding as well as main data, C2PO data, subdata, system data for the microcontroller, and the external I/O status.

CXD2526AQ
80 pin QFP (Plastic)



CXD2526AR
80 pin LQFP (Plastic)



Features

- Data and C2PO FIFO function. External RAM for C2PO is not needed.
- Subdata buffering function. Subdata can be input and output through an external subdata interface.
- TOC data buffering function.
- All RAM data can be read/written via a serial interface for the microcontroller.
- DRAM refresh function
  (for both normal and low power mode).
- External RAM address space can be expanded up to 32M-bit
  (2 × 16M DRAMs: 1783 sectors max.)
  (When using SRAM, expansion up to 8 M-bit is possible.)
- RAM data capacity and remaining capacity calculation and comparison functions.
- C2PO/external input monitor function.

Structure

Silicon gate CMOS IC

Application

Mini Disc

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	Vss–0.5 to +7.0	V
• Input voltage	V_I	Vss–0.5 to +V_{DD}+0.5	V
• Output voltage	V_O	Vss–0.5 to +V_{DD}+0.5	V
• Storage temperature	Tstg	–55 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	+3.0 to +5.5	V
• Operating temperature	Topr	–20 to +75	°C

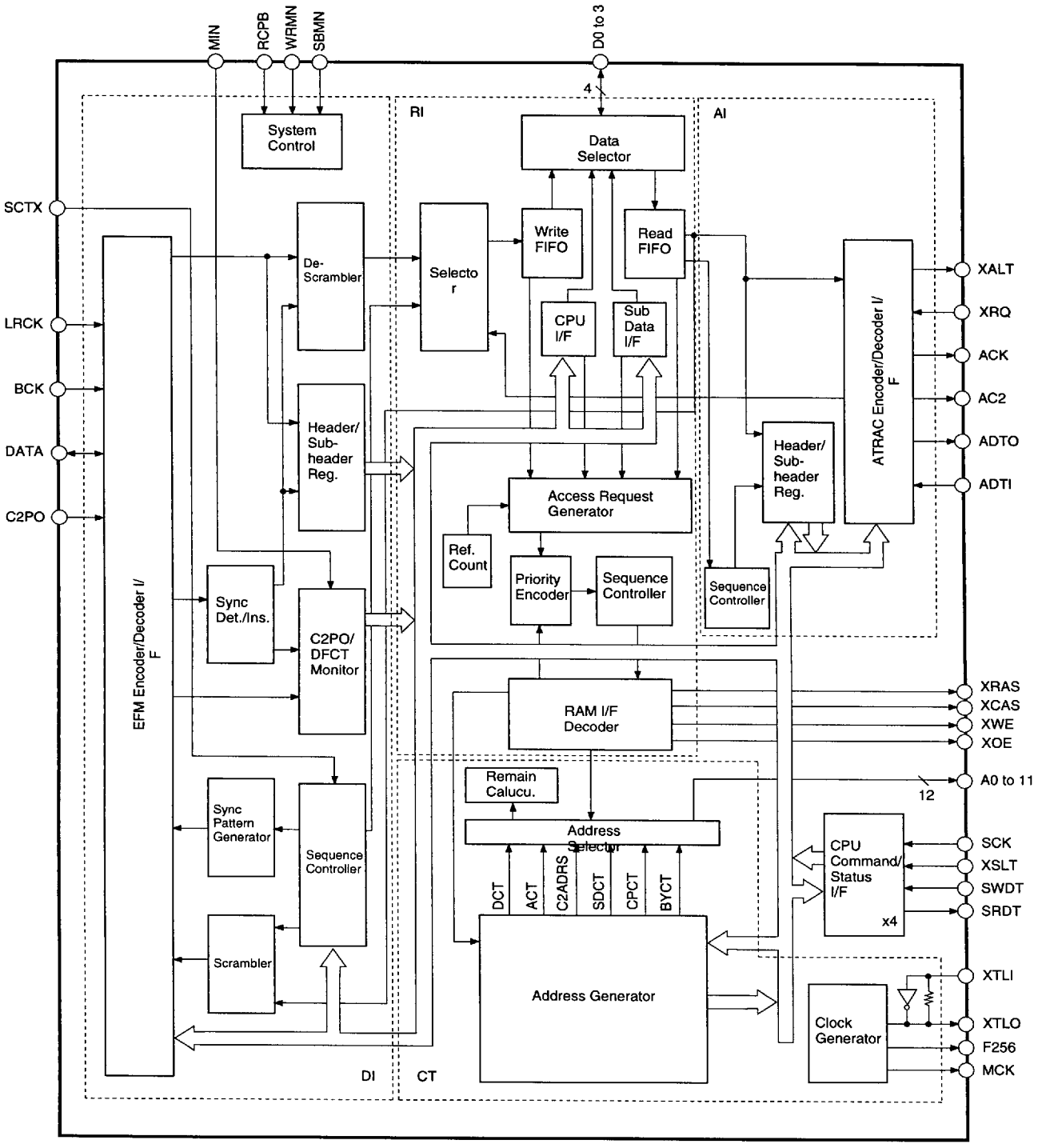
Input/Output Capacitance

• Input pin	C_I	9 (Max.)	pF	
• I/O pins	$C_{I/O}$	11 (Max.)	pF	When high impedance
• Output pin	C_{OUT}	11 (Max.)	pF	

Note) Measurement conditions: V_{DD}=V_I=0V
f=1MHz

E94217-PK

Block Diagram



Description of Each Block

The CXD2526A basically consists of four blocks.

(1) DI block

This is the interface block for the EFM encoder/decoder.

During playback, the input data from the EFM decoder is synchronized internally in sector units by the synchronization detection circuit. Synchronization is not only for input sync pattern detection but also is protected against detection errors by the insertion circuit; in addition, synchronization is controlled so that rapid recovery is possible even if synchronization is lost due to a track jump, etc. If write mode is in effect, input data and C2PO data that have passed through the descrambler circuit are sent to the RI block and are written to RAM based on the address generated by the counter within the CT block.

In addition, this block monitors C2PO data and MIN input pin, and passes the signals to the controller. Knowing the number and position of errors makes more sophisticated control possible.

During recording, this block encodes MD-format sector data. This block generates the sync byte, reads the header time from the register, reads the necessary data from memory, and then passes the data to the EFM encoder via the scrambler circuit. There are three types of sector data and, depending on the settings of the microcontroller, linking data, subdata, and main data can be generated.

(2) RI block

This is the RAM interface block.

This block accepts I/O requests from each of the other blocks and controls RAM access according to a priority ranking. There are five blocks that issue data I/O access requests to RAM; their priority rankings are as follows:

1. DI block
2. AI block
3. Refresh (in DRAM mode)
4. CPU RAM access
5. Subdata access via the external interface

As a result, access to the playback/recording data from the disc has the highest priority, while CPU and external subdata interface data access may be forced to wait due to the generation of internal requests.

(3) CT block

This block contains the counters that generate addresses in RAM. There are five types of counters:

1. DCT Generates addresses for read/write data for the EFM encoder/decoder.
2. ACT Generates addresses for transfer data for the ATRAC encoder/decoder.
3. CCT Generates addresses for CPU memory access.
4. SDCT Generates addresses for read/write data for the EFM encoder/decoder.
   Also generates addresses for memory access by the external subdata interface. This counter is useful for reading/writing subdata.
5. BCT Performs the transfer data count operations.

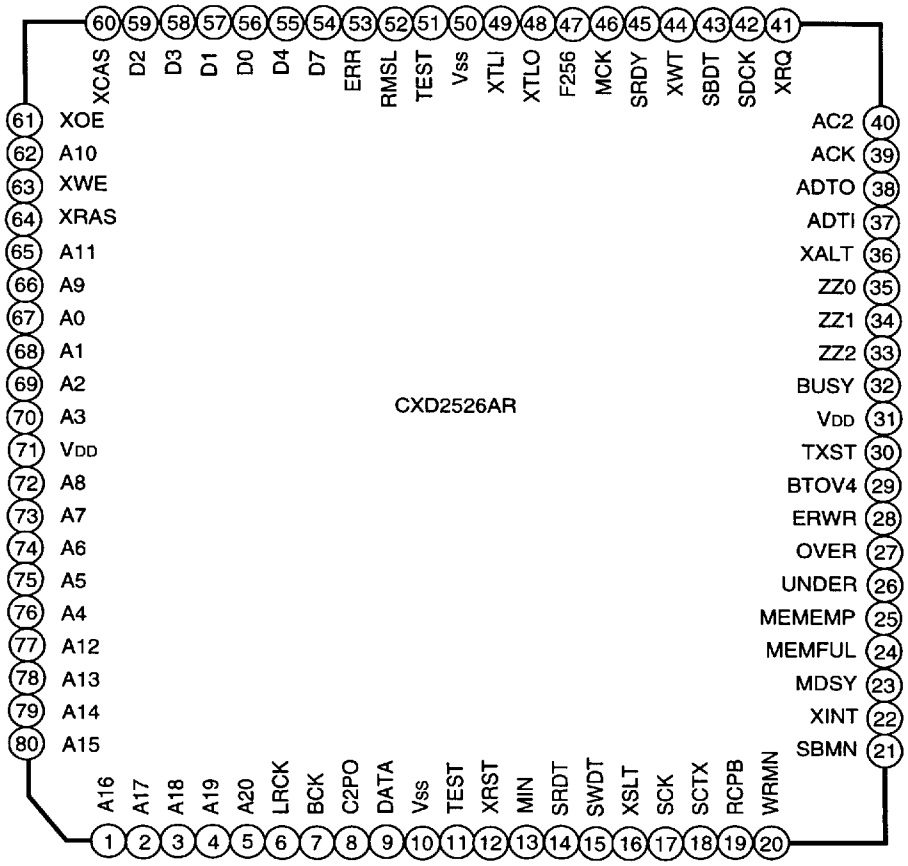
In addition, this block also provides functions that use the DCT and ACT to calculate C2PO addresses, monitor the data capacity, and compare whether the data capacity is greater or smaller than the specified threshold value.

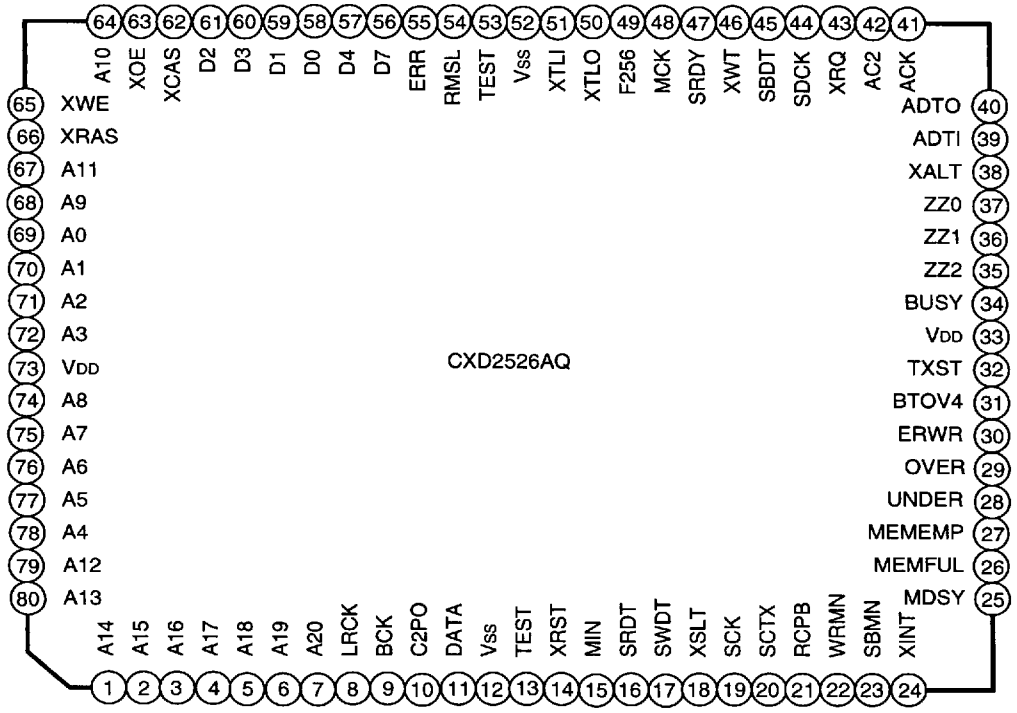
(4) AI block

This is the interface block for the ATRAC encoder/decoder.

This block performs I/O with the ATRAC encoder/decoder and issues requests to the RI block to exchange data.

Pin Configuration





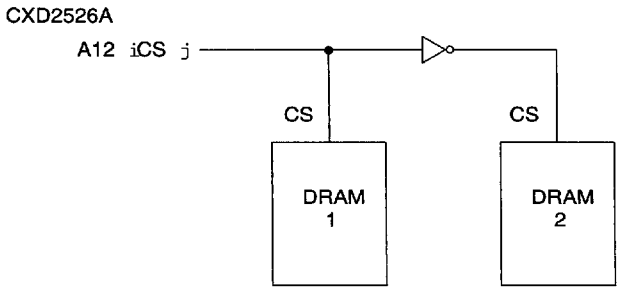
Pin Description

Pin No. Q	Pin No. R	Symbol	I/O		Pin Description
1	79	A14	O	H, L	When RMSL is high, SRAM address bus A14: when RMSL is low, WFFUL. *1
2	80	A15	O	H, L	When RMSL is high, SRAM address bus A15: when RMSL is low, RFEMP. *2
3	1	A16	O	H, L	When RMSL is high, SRAM address bus A16: when RMSL is low, WFOVF. *3
4	2	A17	O	H, L	When RMSL is high, SRAM address bus A17: when RMSL is low, WDTM. *4
5	3	A18	O	H, L	When RMSL is high, SRAM address bus A18: when RMSL is low, ZERO. *5
6	4	A19	O	H, L	When RMSL is high, SRAM address bus A19: when RMSL is low, MDTST. *6
7	5	A20	O	H, L	When RMSL is high, SRAM address bus A20: when RMSL is low, CMPSY. *7
8	6	LRCK	I		LRCK (=Fs) input from the EFM encoder/decoder.
9	7	BCK	I		BCK (=64Fs) input from the EFM encoder/decoder. *8
10	8	C2PO	I		C2PO input from the EFM encoder.
11	9	DATA	I/O	H, L	When playback mode, data input from EFM decoder; when recording mode, data output to EFM encoder.
12	10	Vss			Connect to GND.
13	11	TEST	I		Test pin. Fix low.
14	12	XRST	I		Reset input. (Reset when low.)
15	13	MIN	I		Monitor signal input for external input. Input the signal to be monitored. *9
16	14	SRDT	O	H, Z, L	Microcontroller serial data output. High impedance when the CXD2526A read resister is not selected.
17	15	SWDT	I		Microcontroller serial data input.
18	16	XSLT	I		Microcontroller serial data latch signal input. Latched when fall time.
19	17	SCK	I		Microcontroller serial data shift clock input
20	18	SCTX	I		Data output enable signal input in recording mode. Enabled when high.
21	19	RCPB	I		Low: playback mode; High: monitor recording mode.
22	20	WRMN	I		High: write mode; low: monitor mode.
23	21	SBMN	I		High: records input signal based on SDCT; Low: records based on DCT.
24	22	XINT	O	H, L	Input data MD sync detection signal.
25	23	MDSY	O	H, L	Interrupt request output. Low when interrupt status is generated.
26	24	MEMFUL	O	H, L	High when the main data area becomes full.
27	25	MEMEMP	O	H, L	High when the main data area is empty.
28	26	UNDER	O	H, L	High when RMS < THUND.
29	27	OVER	O	H, L	High when RMS ≥ THOVR
30	28	ERWR	O	H, L	High when the data from C2PO is written to RAM.
31	29	BTOV4	O	H, L	High when BCT ≥ 400 (Hex).
32	30	TXST	O	H, L	High during data transfer.
33	31	V_{DD}			System power supply.
34	32	BUSY	O	H, L	High during RAM access.

Pin No. Q	Pin No. R	Symbol	I/O		Pin Description
35	33	ZZ2	I		Test pin. Fix low.
36	34	ZZ1	I		Test pin. Fix low.
37	35	ZZ0	I		Test pin. Fix low.
38	36	XALT	O	H, L	Data ready or latch signal for the ATRAC encoder/decoder.
39	37	ADTI	I		Data input from the ATRAC encoder/decoder.
40	38	ADTO	O	H, L	Data output to the ATRAC encoder/decoder.
41	39	ACK	O	H, L	Data transfer clock output to the ATRAC encoder/decoder.
42	40	AC2	O	H, L	C2PO output for output data to the ATRAC encoder/decorder.
43	41	XRQ	I		Data request signal input from the ATRAC encoder/decorder.
44	42	SDCK	I		External subdata interface shift clock input.
45	43	SBDT	I/O	H, L	In playback mode, external subdata interface data output; in recording mode, data input.
46	44	XWT	O	H, L	External subdata interface wait signal. When low, the clock for reading new data must not be sent.
47	45	SRDY	O	H, L	External subdata interface access enable signal. When low, if the clock for reading/writing subdata is sent, it is ignored.
48	46	MCK	O	H, L	128Fs output.
49	47	F256	O	H, L	256Fs output.
50	48	XTLO	O		System clock output. (XTLI inverted output)
51	49	XTLI	I		System clock input. Input (512Fs=22.5792MHz)
52	50	Vss			Connect to GND.
53	51	TEST	I		Test pin. Fix low.
54	52	RMSL	I		External RAM select. High: SRAM; low: DRAM.
55	53	ERR	I/O	H, L	C2PO I/O when EXTC2R, bit 4 of write register WR04 is 1. When 0, open.
56	54	D7	I/O	H, L	When RMSL is high, SRAM data bus D7; when low, open.
57	55	D4	I/O	H, L	When RMSL is high, SRAM data bus D4; when low, open.
58	56	D0	I/O	H, L	RAM data bus D0.
59	57	D1	I/O	H, L	RAM data bus D1.
60	58	D3	I/O	H, L	RAM data bus D3.
61	59	D2	I/O	H, L	RAM data bus D2.
62	60	XCAS	I/O	H, L	When RMSL is high, RAM data bus D6; when low, $\overline{CAS}$ output for DRAM.
63	61	XOE	O	H, L	RAM output enable.
64	62	A10	O	H, L	RAM address bus A10.
65	63	XWE	O	H, L	RAM write enable.
66	64	XRAS	I/O	H, L	When RMSL is high, data bus D5; when low, RAS output for DRAM.

Pin No. Q	Pin No. R	Symbol	I/O		Pin Description
67	65	A11	O	H, L	RAM address bus A11.
68	66	A9	O	H, L	RAM address bus A9.
69	67	A0	O	H, L	RAM address bus A11. *12
70	68	A1	O	H, L	RAM address bus A1.
71	69	A2	O	H, L	RAM address bus A2.
72	70	A3	O	H, L	RAM address bus A3.
73	71	V_{DD}			System power suypply.
74	72	A8	O	H, L	RAM address bus A8.
75	73	A7	O	H, L	RAM address bus A7.
76	74	A6	O	H, L	RAM address bus A6.
77	75	A5	O	H, L	RAM address bus A5.
78	76	A4	O	H, L	RAM address bus A4.
79	77	A12	O	H, L	When RMSL is high, RAM address bus A12; when low, CS output. *10
80	78	A13	O	H, L	When RMSL is high, RAM address bus A13; when low, SYOK output. *11

*1 WFFUL : High if write FIFO buffer becomes full.
*2 RFEMP : High if write FIFO buffer becomes empty.
*3 WFOVF : High if write FIFO buffer overflows.
*4 WDTM : Outputs the window timing within the DI block.
*5 ZERO : High when BCT=0.
*6 MDTSC : High for input data header sectors #00 to 1F; low in all other cases.
*7 CMPSY : Insertion sync timing.
*8 Polarity is set by WR0E LRSL.
*9 MIN can be read by RR0F.
*10 CS: DRAM chip select in the case of using two memory chips for WR04. (Refer to the figure below)
*11 Refer to the read resistrer RR01 SYOK for SYOK.
*12 This pin is used for DRAM. Leave this pin open if SRAM is selected when RMSL=high. In this case, the lowest bit of the address is used from A1.



Exampled of two DRAMs used

Electrical Characteristics

1. DC characteristics

DC characteristics 1 (V_{DD}=3.0±0.3V, Vss=0V, Topr=–20 to +75°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)		1.8			V	*2
	Low level input voltage	V_{IL} (2)				0.5	V	
Input voltage (3)	High level input voltage	V_{IH} (3)		0.8V_{DD}			V	*3
	Low level input voltage	V_{IL} (3)				0.2V_{DD}	V	
Output voltage (4)	High level output voltage	V_{OH} (4)	I_{OH}=–1mA	V_{DD}–0.8			µA	*4
	Low level output voltage	V_{OL} (4)	I_{OL}=–2mA			0.4	µA	
Input leak current		I_{IL}	V_{IN}=V_{SS}=V_{DD}	–10		10	µA	*5
				–40		40	µA	*6
Tri-state output leak current		Ioz		–40		40	µA	*7

DC characteristics 2 (V_{DD}=4.0±5.5V, Vss=0V, Topr=–20 to +75°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)		2.2			V	*2
	Low level input voltage	V_{IL} (2)				0.8	V	
Input voltage (3)	High level input voltage	V_{IH} (3)		0.8V_{DD}			V	*3
	Low level input voltage	V_{IL} (3)				0.2V_{DD}	V	
Output voltage (4)	High level output voltage	V_{OH} (4)	I_{OH}=–1mA	V_{DD}–0.8			µA	*4
	Low level output voltage	V_{OL} (4)	I_{OL}=–2mA			0.4	µA	
Input leak current		I_{IL}	V_{IN}=V_{SS}=V_{DD}	–10		10	µA	*5
				–40		40	µA	*6
Tri-state output leak current		Ioz		–40		40	µA	*7

Applicable pins

*1 LRCK, BCK, C2PO, DATA, TEST, SWDT, XSLT, SCK, SCTX, RCPB, WRMN, SBMN, ZZ2, ZZ1, ZZ0, ADTI, XRQ, SDCK, SBDT, TEST, RMSL, ERR

*2 D7, XRAS, XCAS, D4, D3, D2, D1, D0

*3 XRST, MIN

*4 A20 to A0, SRDT, XINT, MDSY, ADTO, AC2, XWT, SRDY, XOE, XWE, D7, XRAS, XCAS, D4, D3, D2, D1, D0, MCK, F256, MEMFUL, MEMEMP, UNDER, OVER, ERWR, BTOV4, TXST, BUSY, DATA, XALT, ACK, SBDT, ERR

*5 LRCK, BCK, C2PO, TEST, SWDT, XSLT, SCK, SCTX, RCPB, WRMN, SBMN, ZZ2, ZZ1, ZZ0, ADTI, SDCK, TEST, RMSL

*6 DATA, XRQ, SBDT, ERR

2. AC characteristics

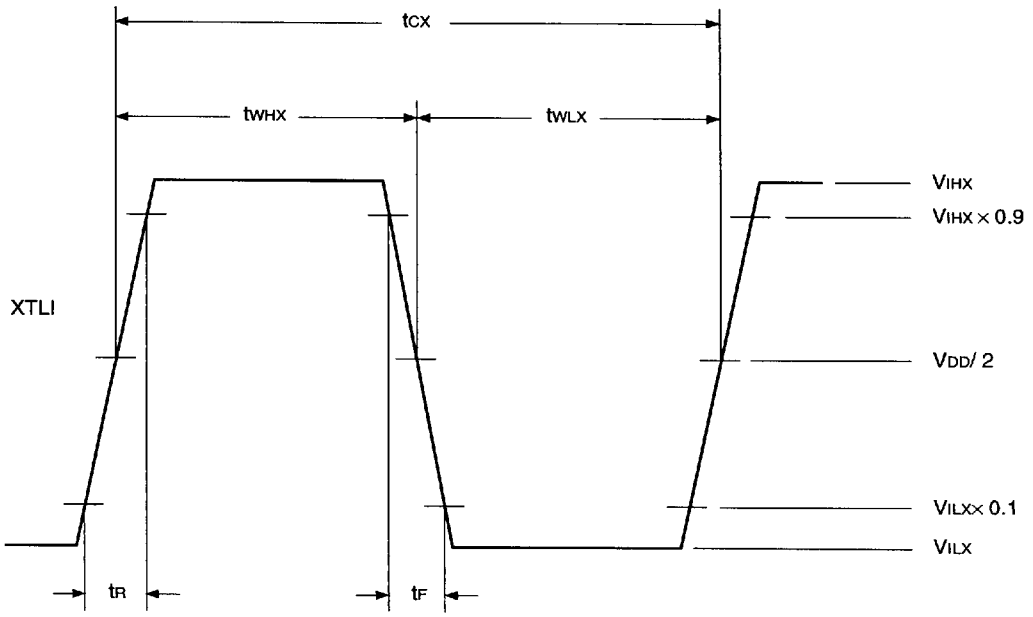
(1) XTLI pin

• When using self-oscillation (Topr=–20 to +75°C, V_{DD}=3.0 to 5.5V)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	$f_{MAX.}$	20	22.5792	25	MHz

• When inputting a pulse to XTLI (Topr=–20 to +75°C, V_{DD}=3.0 to 5.5V)

Item	Symbol	Min.	Typ.	Max.	Unit
High-level pulse width	t_{WHX}	20		25	ns
Low-level pulse width	t_{WLX}	20		25	ns
Pulse cycle	t_{CX}	40		50	ns
Input high level	V_{IHX}	0.7V_{DD}			V
Input low level	V_{ILX}			0.3V_{DD}	V
Rise time Fall time	t_R, t_F			10	ns



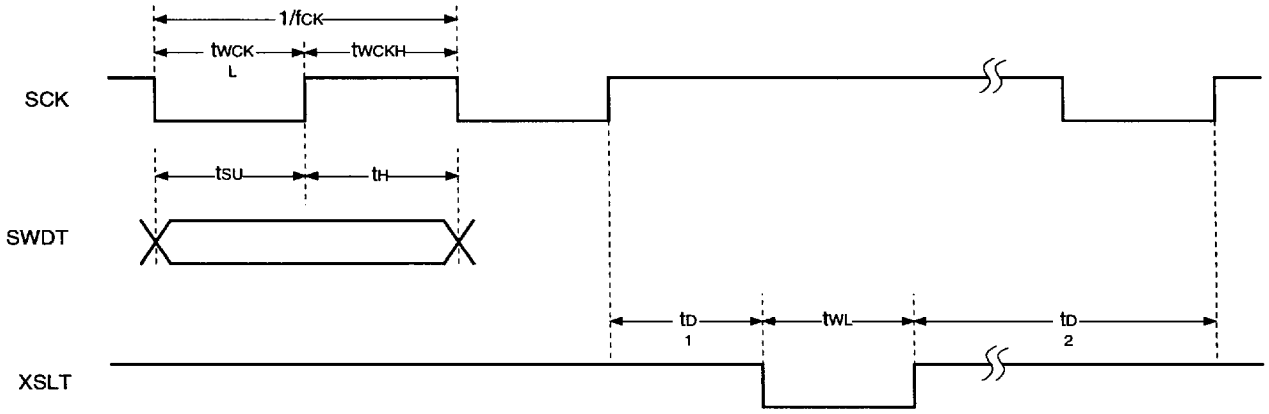
• When inputting a sine wave to the XTLI pin via a capacitor

(Topr=–20 to +75°C, V_{DD}=3.0 to 5.5V)

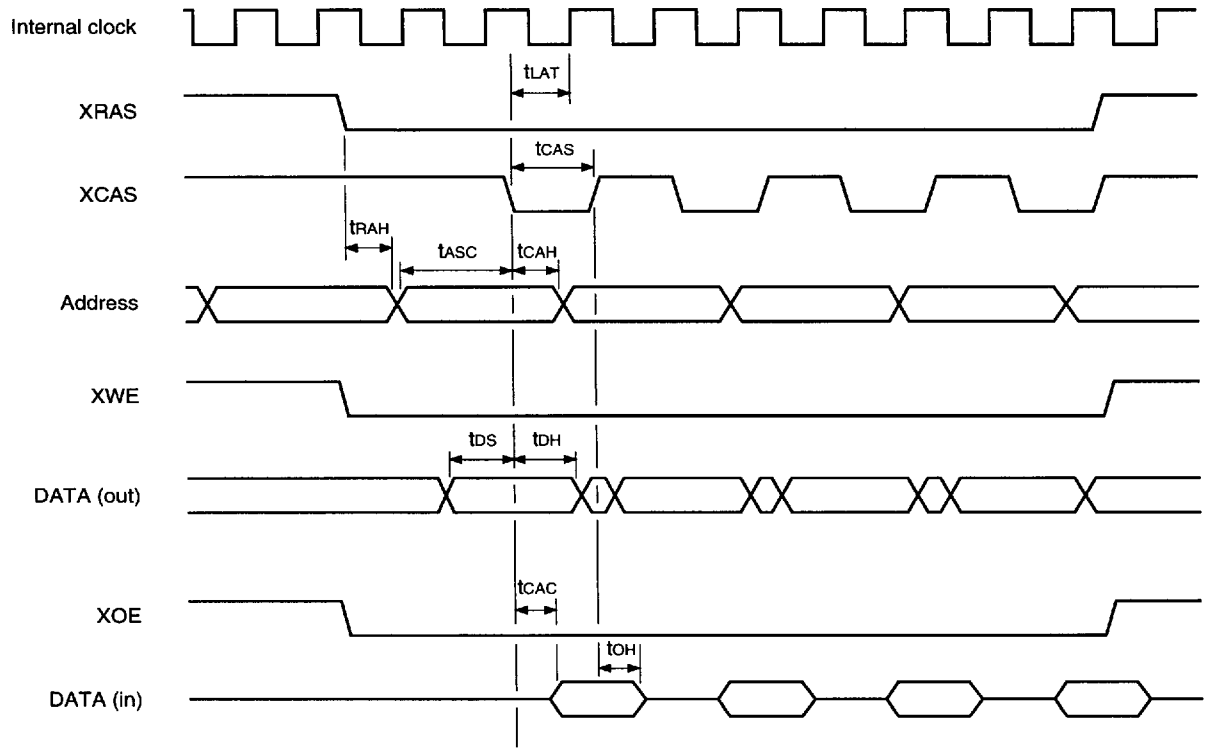
Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD}+0.3	Vp-p

(2) SCK, SWDT and XSLT pins (V_{DD}=3.0 to 5.5V, Vss=0V, Topr=–20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}	100		2.5	MHz
Clock pulse width (L)	t_{WCKL}	0.2		120	µs
Clock pulse width (H)	t_{WCKH}	0.2		120	µs
Setup time	t_{SU}	200			ns
Hold time	t_H	200			ns
Delay time 1	t_{D1}	200			ns
Delay time 2	t_{D2}	200			ns
Latch pulse width	t_{WL}	400			ns



3. DRAM interface (V_{DD}=3.0V to 5.5V; external load: 40pF or less)

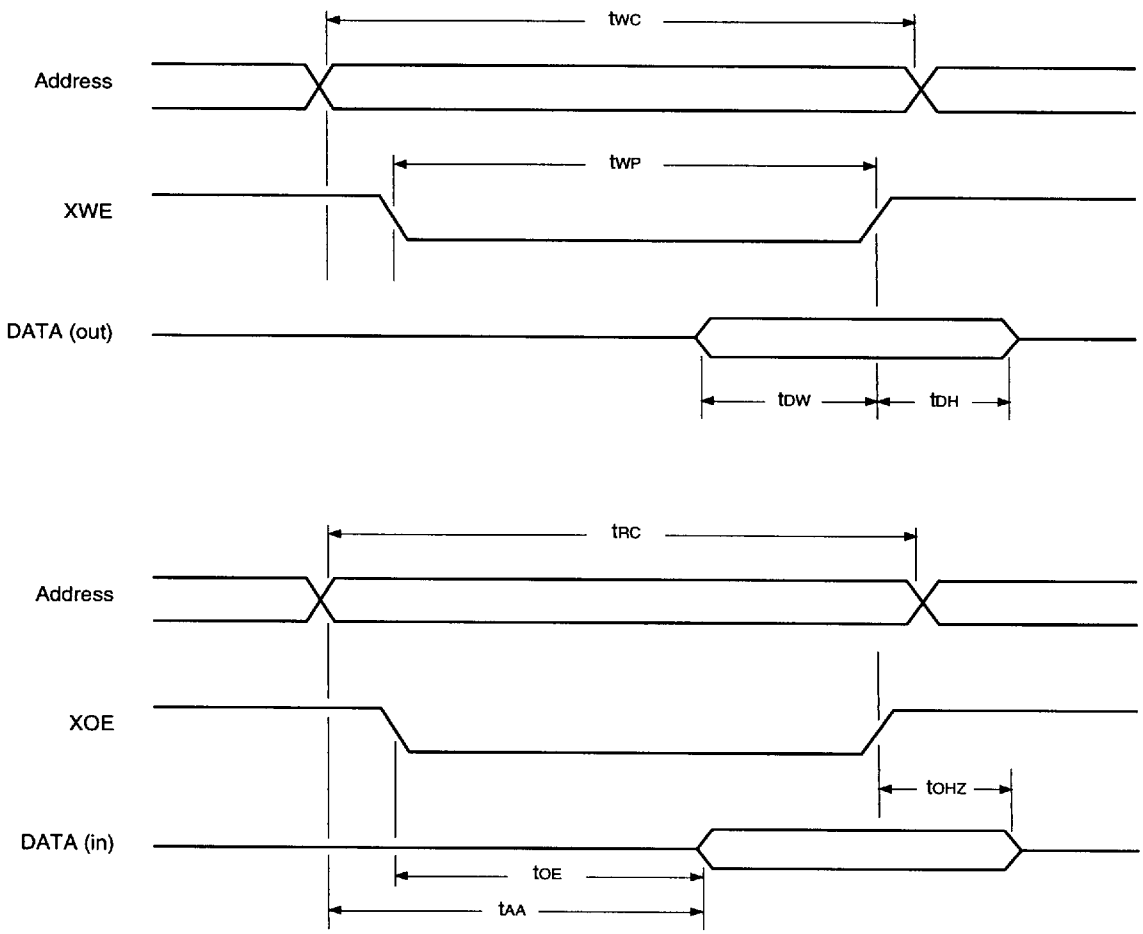


DRAM that can be connected to the CXD2526AQ/AR are those that can handle a × 4-bit data bus, high-speed page mode (early write cycle), and CAS before RAS refresh. For the access times, refer to the timing chart shown above.

	Min.	Typ.	Max.
t_{CAS}	70	—	—
t_{RAH}	75	—	—
t_{ASC}	65	—	—
t_{CAH}	75	—	—
t_{DH}	65	—	—
t_{DS}	60	—	—
t_{OH}	50	—	—
t_{CAC}	—	—	40
t_{LAT}	50	70	85

(Unit: ns)

4. SRAM interface (V_{DD}=3.0 to 5.5V; external load: 40pF or less)



	Min.	Typ.	Max.
t_{WC}	150	—	—
t_{WP}	100	—	—
t_{DW}	60	—	—
t_{DH}	0	—	—
t_{RC}	150	—	—
t_{OE}	—	—	70
t_{AA}	—	—	150
t_{OHZ}	—	—	50

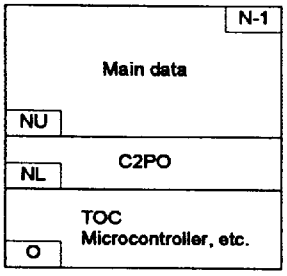
(Unit: ns)

Description of Functions

1. Basic Operation

(1) Partitioned use of memory

In order to share memory resources effectively, memory is generally partitioned as shown below. The memory size is N. NU and NL are set by WR10 and WR11. The main data size is N-NU.



During playback mode, the C2PO area must be at least 1/8 the size of the main data area. It is also necessary to select NU and NL so that the following equation is true:

$$NL \leq NU - \frac{N-NU}{8} = \frac{9NU-N}{8}$$

The area from 0 to NL-1 can be used as extended RAM for the microcontroller for subdata, TOC, etc.
In addition, during recording mode, because there is no need to handle C2PO data, the area from NL to NU-1 can be used freely. Normally, NL is set to be NU.

(2) Counters

The CXD2526A has four counters that generate addresses and one that keeps a count of the transfer bytes.

(1) DCT (drive read/write counter)
: Generates R/W addresses for I/O data for the EFM encoder/decoder.

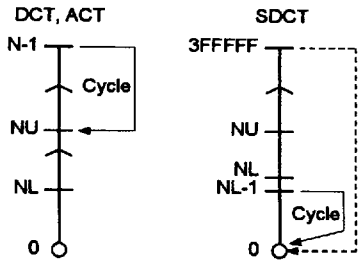
(2) ACT (ATRAC encoder/decoder R/W counter)
: Generates R/W addresses for I/O data for the ATRAC encoder/decoder.

(3)CCT (CPU R/W counter)
: Generates R/W addresses for I/O data accessed by the CPU.

(4) SDCT (Sub Data R/W counter)
: Generates R/W addresses either for I/O data for the microcontroller for external subdata, or for I/O data for the EFM encoder/decoder.

(5) BCT (byte counter)
: Byte transferring counter and also down counter either for the EFM encoder or for the ATRAC encoder/decoder.

DCT and ACT are cyclical counters that return to the value NU as the next step after highest address specified for the normal RAM size (WR04) is reached. SDCT is a cyclical counter that returns to 0 as the next step after the value NL-1 is reached.

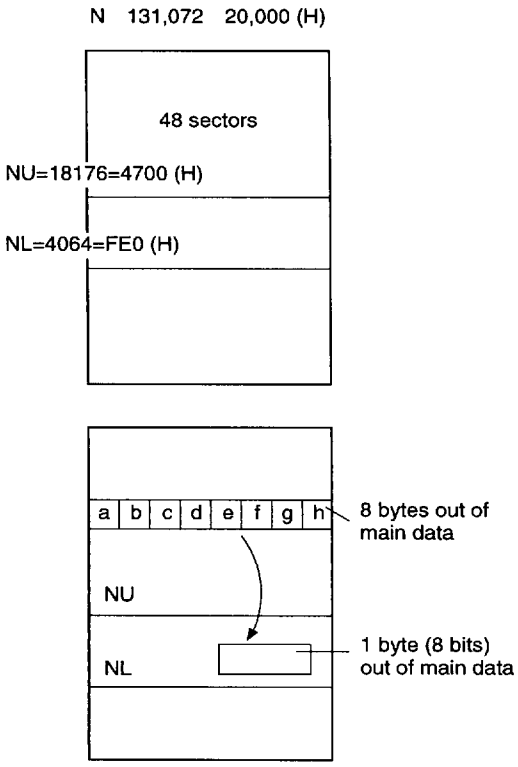


ACT and DCT never contain a value below NU and SDCT never contains a value equal to NL or more. There is no chance of data in other areas being damaged.

(3) C2PO address generation

When SBMN=low and EXTC2R (WR04)=0 in playback mode, the C2PO address is automatically calculated based on the values of DCT and ACT, and is input/output at the same time as data. The relationship between a data address and the address where the C2PO information for that data is recorded as described below.

$$\text{C2PO address} = NL + \left[\frac{\text{data address} - NU}{8}\right]$$



Setting example:

When using a 1M DRAM, 48 sectors were allocated as the main data area.

N=20000 (H) =131,072
NU=4700 (H) =18,176
NL=FE0 (H) =4,064

In this case, the C2PO corresponding to the data in address 12345 (H) =74,565 is as follows.

$$\text{C2PO address} = FE0\ (H) + \left[\frac{12345\ (H) - 4700\ (H)}{8}\right]$$

$$= FE0\ (H) + 1B88\ (H)$$
$$= 2B68\ (H)$$

Furthermore, the bit position is bit 5, since the lowest significent bits of 12345 (H) are 101 (B).

(In the above example)
Address 12340: no errors in data (0)
Address 12341: error in data (1)
Address 12342: no errors in data (0)
Address 12343: error in data (1)
Address 12344: error in data (1)
Address 12345: error in data (1)
Address 12346: no errors in data (0)
Address 12347: no errors in data (0)
In this case, the data in 2B68 (H) is 0011, 1010=3A (H).

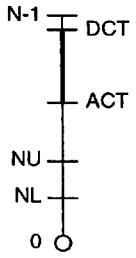
Even during playback mode, if SDCT is selected for getting data (SBMN is high), C2PO data is not retrieved.

(4) Data size calculation

RMS=DCT–ACT is calculated, and the result is stored in a read register (RR0C). At this point, NU is used for compensation:

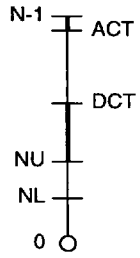
(1) When DCT ≥ ACT:

RMS = DCT – ACT



(2) When ACT > DCT:

RMS = (N–ACT)+(DCT–NU)
= (DCT–ACT)+(N–NU)



The RMS value in playback mode is the amount of main data buffered, and in recording mode, is the amount of free area in the main data area.

(5) Data size comparison

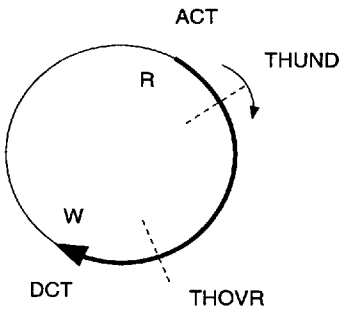
The RMS value computed in item (4) above is compared with the threshold values set in write registers WR12 and 13, and an interrupt is generated based on their relationship.

This function is useful in generating the timing for starting and stopping data retrieval.

If RMS ≥ THOVR changes from false to true, the THOVR status (RR00) is set.

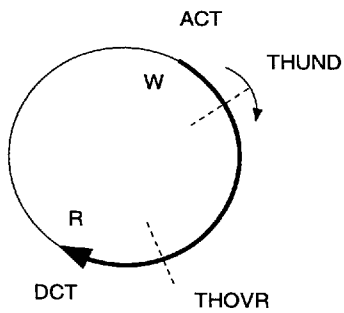
If RMS < THUND changes from false to true, the THUND status (RR00) is set.

Playback mode



RMS =DCT–ACT
=W–R
=data size

Recording mode



RMS =DCT–ACT
=R–W
=size of unrecorded area

2. Operation during Playback

(1) Write mode/monitor mode switching

If the external input pin WRMN is

high: write mode

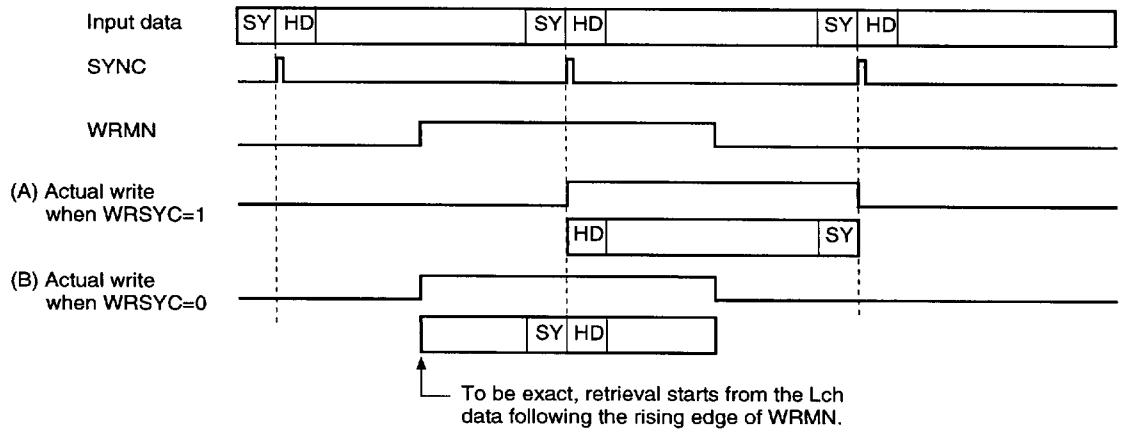
low: monitor mode

In write mode, writing to RAM is enabled for all input data, including sync/headers, from the EFM decoder.

Bit 6 of write register WR0E:

When WRSYC=1, writes are synchronized with the input sync timing.

When WRSYC=0, writes are not synchronized with the input sync timing.



If monitor mode is selected, all writes to RAM are prohibited. The headers/subheaders are pulled in internal registers (RR02, RR03), regardless of the mode.

(2) Sub/main switching

When the external input pin SBMN is

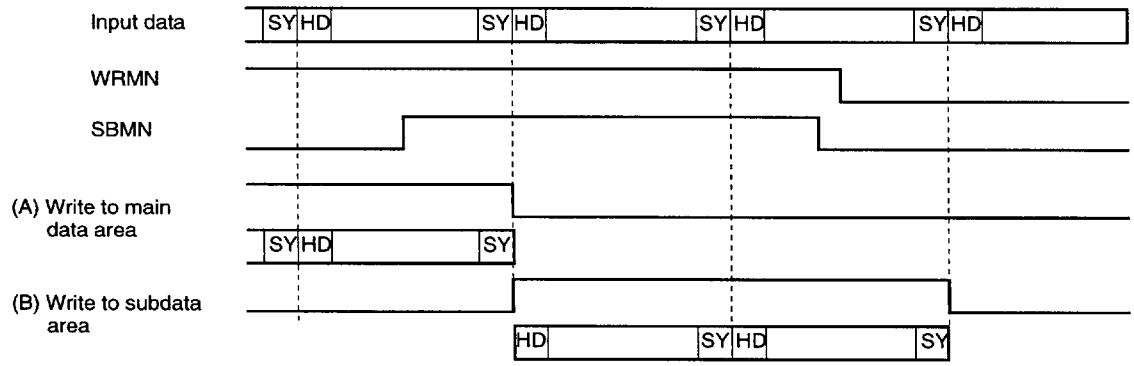
high: external input is pulled in memory based on the SDCT counter

low: external input is pulled in memory based on the DCT counter

If the DCT counter is selected and EXTC2R (WR04)=0, C2PO information is pulled in the same manner, based on the address shown in section 6-1.(3).

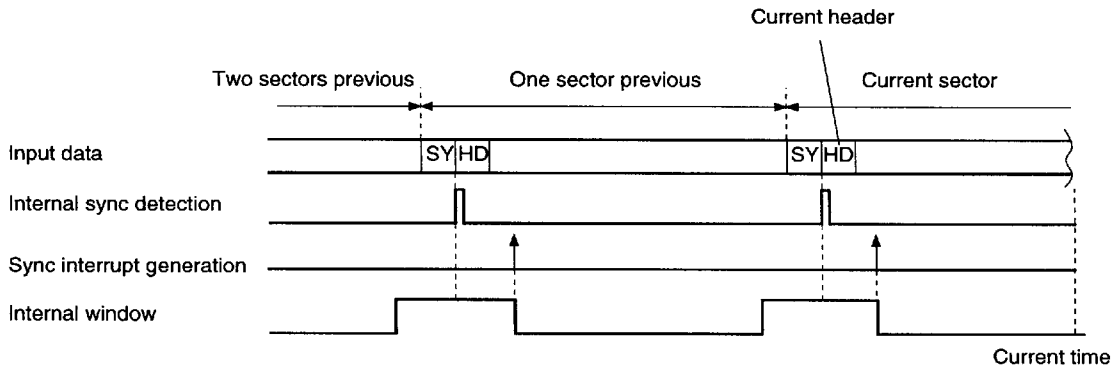
If the SDCT counter is selected, C2PO information is not pulled in.

Note that this switching is performed in synchronization with SYNC.



(3) Decoder

This section describes the internal operation of the MD sector data decoder.



The sector being input to this IC is called the "current sector". When sync is detected or after 12 LRCK cycles of the inserted timing (the timing for closing the window), a sync interrupt is generated. At this point, the current header sync status (RR01), the header data (RR02) and the four bytes of data (RR03) following the header can be read from the register; in addition, if in write mode (WRMN is high), it is also possible to read as the current header address (RR04) the address in memory where the first byte of the current header is written.

The contents of the sync status register are as follows:

SYOK : Indicates that the current header sync was read either after the previous sector sync or after 2352 bytes in the insertion timing.

NOSY : Indicates that the current header sync was not detected in the window.

ILSY : Set when the sync pattern was detected outside of the window.

WNDLK : Indicates that the insertion timing is synchronized correctly and the window is active.

EIB : Indicates that a C2PO error exists within the sector previous to the current sector.

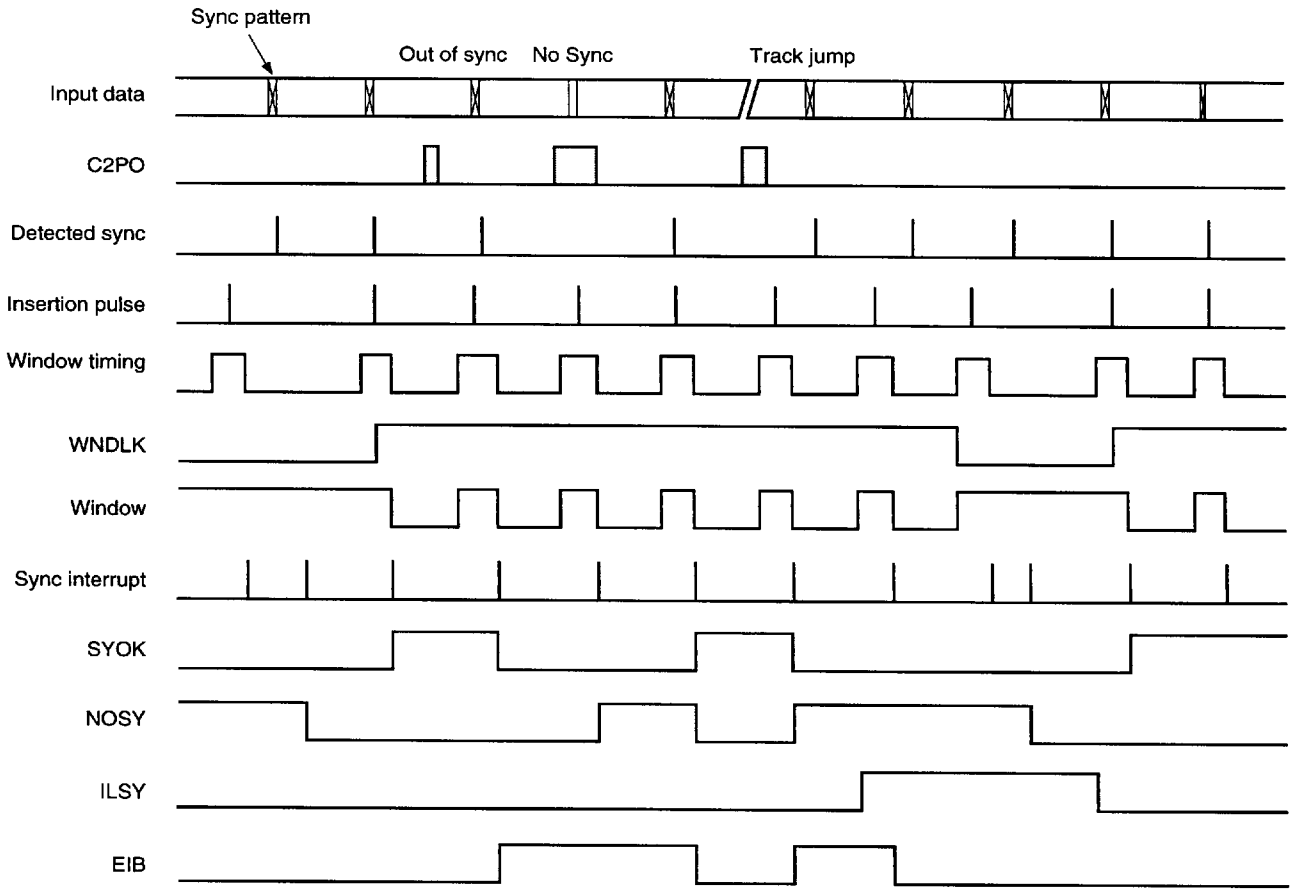
Decoder's automatic algorithm (sync detection/windows/insertion protection)

The input data sync pattern is detected and the insertion counter is reset with the same timing. If sync is detected after 2352 bytes, the insertion timing is assumed to be synchronized, and the window is activated.

Sync detected while the window is not active are all effective and are treated as insertion counter reset inputs.

When the window is active, only sync detected within the window are effective as resets; sync outside the window are read as illegal sync.

If illegal sync occur in two consecutive frames, it is decided that the insertion synchronization has been lost, the window is opened, and any sync detection becomes valid for synchronization purposes.



(4) Transfers to the ATRAC decoder

a) Normal transfers

During playback, the following procedure is necessary in order to transfer data to the ATRAC decoder:

1. Set the start address of the data to be transferred in ACT. (WR08)
2. Set the number of bytes to be transferred in BCT. (WR08)
   (Actually, set the number of bytes-1; refer to the register commands.)
3. Transfer triggered. (WR06)

The CXD2526A transfers data to the ATRAC decoder based on the ACT address value while counting down the BCT. When the BCT reaches zero and the last bit of the last byte has been transferred, the PBTXED status of RR00 is generated.

Although transfers are made at a maximum data rate of 5.6448Mbps (705KB/s), if the input XRQ pin from the ATRAC decoder goes high, the transfer process waits.The following are the transfer trigger options:

1. Getting the transmission header time ..... ACHDLD
2. Autoloading the byte counter value ..... BTLD
3. Autotrigger ..... AUTTRG

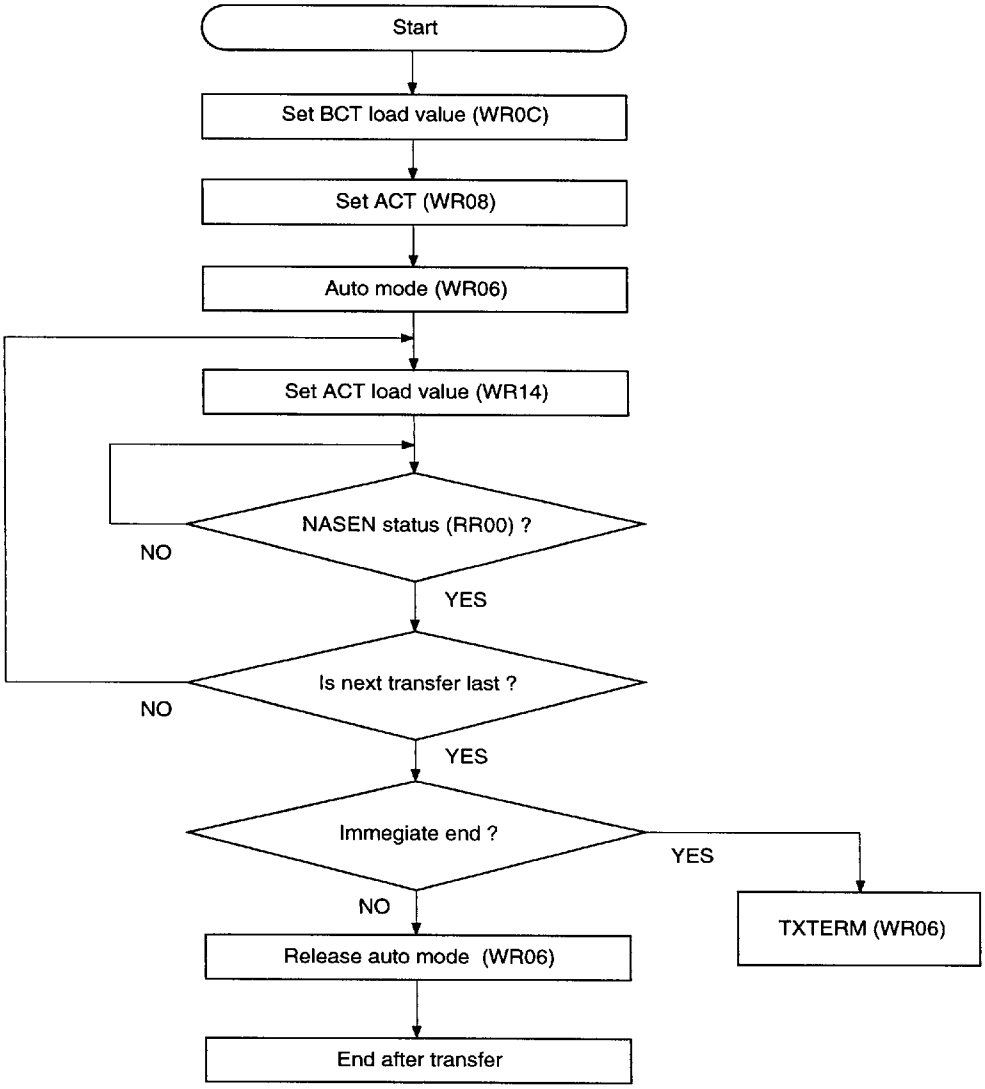
For details, refer to the WR06 register commands.

b) Autotrigger mode transfer (AUTTRAG of WR06)

In autotrigger mode, when a transfer ends, the next setting values for the ACT (ACTLV value of WR14) and BCT (BCTLV value of WR0C) are automatically loaded and the next transfer is triggered automatically.

Because the value loaded to the BCT is normally the same as the previous value, there is no special reason to set it again once it has been set, but the start address for the transfer does need to be set before one transfer is completed. In other words, it must be set before the ATRAC decoder finishes reading the transfer bytes for one sector (approximately 65ms).

First, set the ACT value and then send the transfer trigger in autotrigger mode. At this point, write the ACT start address for the next transfer in WR14. Once the transfer is completed and this ACTLV load value and the BCTLV load value are loaded, the NASEN status (RR00) is generated. In this way, data can be sent one after the other (without demanding strict timing). If auto trigger mode is cleared, transfer is terminated once the current transfer bytes have all been sent and the PBTXED (RR00) status is generated. Note that the auto trigger mode is always set during the recording mode.



3. Operation during Recording

C2PO data is not written during recording.
Data from the ATRAC encoder is stored in a buffer as is; after a header is added and the data is scrambled, the sync pattern is added and the data is sent to the EFM encoder.

(1) Recording data buffering

If WRMN is high, the data from the ATRAC encoder is immediately stored in a buffer according to the ACT value.

(2) Recording data transfer

When the trigger command (TXTRG of WR06) is sent from the microcontroller and the SCTX pin is high, data transfer starts from Lch (data immediately after the changing of LRCK polarity to Lch) to the EFM encoder.
After synchronized (12 bytes), the header (4 bytes) specified by register WR02 and the subheader (4 bytes) specified by WR03 are sent, followed by the number of bytes of data (based on SC0 and SC1 (WR06)) specified by BCTLV (WR0C).
In the case of the MD format, the number of bytes of main data to be sent per sector is:
2352–12–8=2332 bytes, which is further adjusted as follows:

2332–1=2331=91B (H)

Therefore, it is necessary to send 09, 1B (H) to WR0C. All data after synchronized is scrambled before it is sent.

Data specified by SC0 and SC1 are as follows:

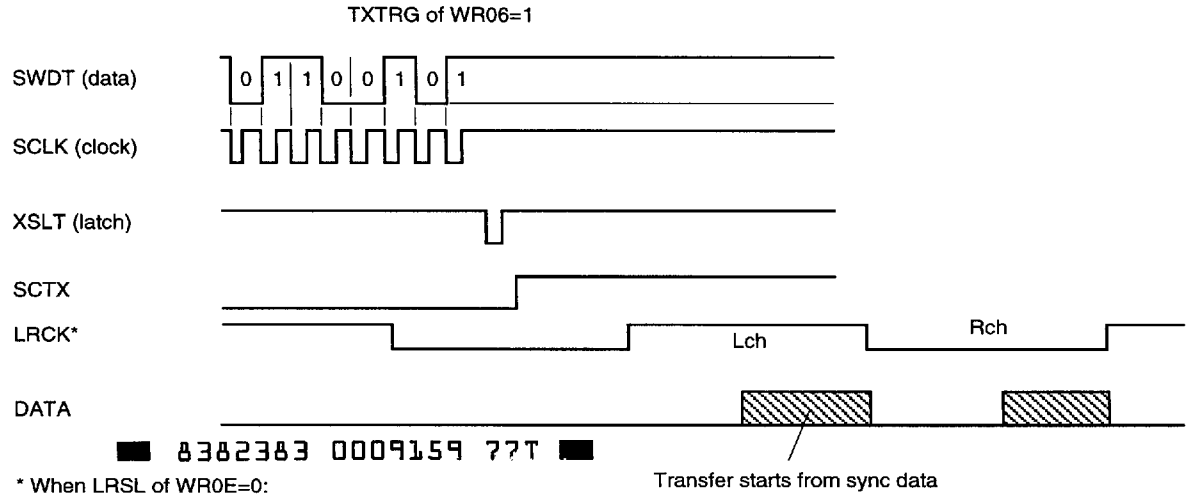
SC1, 0=00 : linking data
Generates/transfers all-zero data. Data is not read from memory, and the DCT value does not change.

SC1, 0=01 : main data
Data is read from memory based on the address indicated by DCT and sent.

SC1, 0=10 : subdata
Data is read from memory based on the address indicated by SDCT and sent.

SC1, 0=11 : transfer end

Timing chart for start of record data transfer



* When LRSL of WR0E=0:

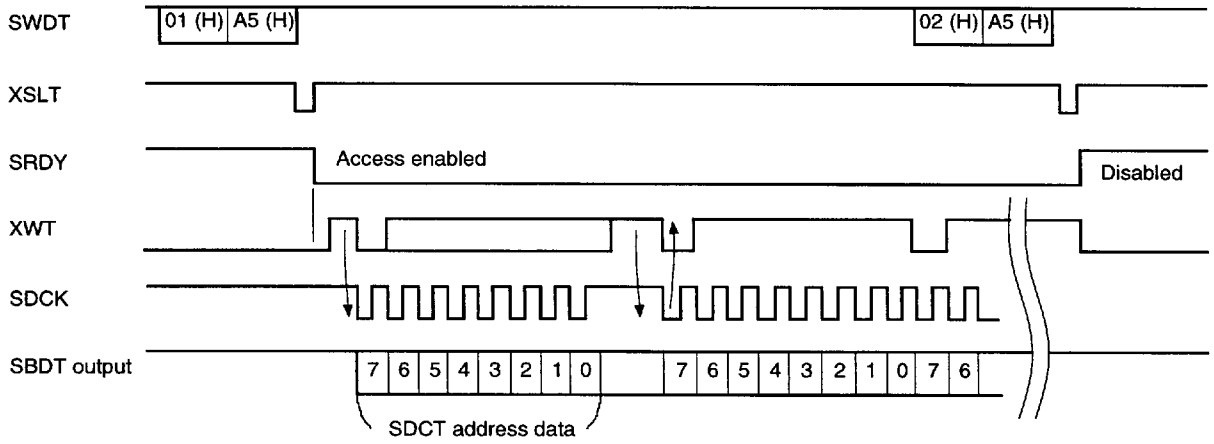
4. External Subdata Interface

Data I/O can be performed through the external subdata interface.
During playback, the external subdata interface is used for reading memory. If the control microcontroller sends the command SBDTEN of WR05=1, the SRDY pin goes low, indicating that external interface access is enabled. If the clock is then sent to SDCK, memory is read according to the address based on SDCT, and the data is read from the SBDT pin MSB first. SDCT is automatically incremented with each read from memory.
If XWT is high, it is permissible to send the clock for the read and then read the data. In this case, XWT becomes low while the MSB bits are being output, but if a wait has been initiated regarding internal access, XWT will remain low for an extended period. Normally, because XWT returns to the high level right away, it is permissible to continuously send the clock needed to read the next byte. If XWT is low when the next new byte is to be read, the internal memory read operation is not yet complete; therefore, the clock must not be sent until XWT is high.
If the SBDTDS of WR05=1 command is sent, SRDY pin goes high, and external interface access is disabled.
Data in memory at the address indicated by the SDCT value can be read through the external interface. In order to pass subdata to the external interface, it is necessary to load the subdata into a certain area in memory beforehand and then set the start address value in SDCT before sending the external interface access command. Doing this requires the following controls, for example:

1. Set the start address to which data is to be loaded in SDCT.
2. Load the target subdata on the disc into memory based on SDCT. (Sectors FC to FF (H); in the case of a recordable MD, FF (H))
3. Once the data is loaded, set the SDCT again.
4. Send the external access enable command.
5. Send the external access disable command.

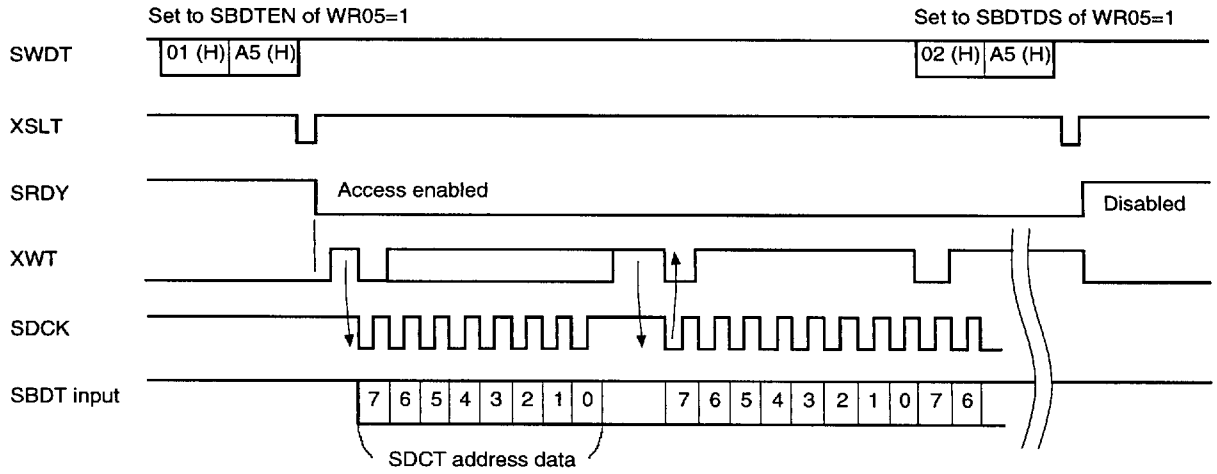
The control microcontroller must not make any accesses that would use the SDCT because SDCT is surrendered to the external interface during the interval of step 4 and 5.

• **Timing chart for external subdata interface read system (during playback)**



Operation during recording is basically the same as during playback. The SBDT pin becomes the input for writing data from the external interface.

• **Timing chart for external subdata interface write system (during recording)**



Description of Register Commands (All transfers are performed LS bit first, MS byte first)

• Write Register

Register No.	Name	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
WR00	Interrupt Control Register	MDSY	PBTXED	RPSEN	OVRFUL	THOVR	THUND	NASEN	SGSY
WR01	Decoder Control Register	AUTALG	INSEN	WNDEN	WNDRST	SYDTEN	1	0	1
WR02 -1	REC TX Header	RTHD 24	RTHD 25	RTHD 26	RTHD 27	RTHD 28	RTHD 29	RTHD 30	RTHD 31
-2		RTHD 16	RTHD 17	RTHD 18	RTHD 19	RTHD 20	RTHD 21	RTHD 22	RTHD 23
-3		RTHD 08	RTHD 09	RTHD 10	RTHD 11	RTHD 12	RTHD 13	RTHD 14	RTHD 15
-4		RTHD 00	RTHD 01	RTHD 02	RTHD 03	RTHD 04	RTHD 05	RTHD 06	RTHD 07
WR03 -1	REC TX Subheader	RTSH 24	RTSH 25	RTSH 26	RTSH 27	RTSH 28	RTSH 29	RTSH 30	RTSH 31
-2		RTSH 16	RTSH 17	RTSH 18	RTSH 19	RTSH 20	RTSH 21	RTSH 22	RTSH 23
-3		RTSH 08	RTSH 09	RTSH 10	RTSH 11	RTSH 12	RTSH 13	RTSH 14	RTSH 15
-4		RTSH 00	RTSH 01	RTSH 02	RTSH 03	RTSH 04	RTSH 05	RTSH 06	RTSH 07
WR04	RAM SIZE Reg.	RAMSZ 0	RAMSZ 1	RAMSZ 2	REFSEL	EXTC2R	OVRST P	0	0
WR05	SUB DATA CTL	SBDTEN	SBDTDS	RFRST	WFRST	0	0	0	0
WR06	TX Trigger	TXTRG	TXTRM	0	ACHDLD	BTLD	AUTTR G	SC0	SC1
WR07 -1	Drive R/W CT (DCT)	DCT 16	DCT 17	DCT 18	DCT 19	DCT 20	DCT 21	0	0
-2		DCT 08	DCT 09	DCT 10	DCT 11	DCT 12	DCT 13	DCT 14	DCT 15
-3		DCT 00	DCT 01	DCT 02	DCT 03	DCT 04	DCT 05	DCT 06	DCT 07
WR08 -1	ATRAC Encoder/Decoder R/W CT (ACT)	ACT 16	ACT 17	ACT 18	ACT 19	ACT 20	ACT 21	0	0
-2		ACT 08	ACT 09	ACT 10	ACT 11	ACT 12	ACT 13	ACT 14	ACT 15
-3		ACT 00	ACT 01	ACT 02	ACT 03	ACT 04	ACT 05	ACT 06	ACT 07
WR09 -1	CPU R/W CT (CCT)	CCT 16	CCT 17	CCT 18	CCT 19	CCT 20	CCT 21	0	0
-2		CCT 08	CCT 09	CCT 10	CCT 11	CCT 12	CCT 13	CCT 14	CCT 15
-3		CCT 00	CCT 01	CCT 02	CCT 03	CCT 04	CCT 05	CCT 06	CCT 07
WR0A -1	Subdata R/W CT (SDCT)	SDCT 16	SDCT 17	SDCT 18	SDCT 19	SDCT 20	SDCT 21	0	0
-2		SDCT 08	SDCT 09	SDCT 10	SDCT 11	SDCT 12	SDCT 13	SDCT 14	SDCT 15
-3		SDCT 00	SDCT 01	SDCT 02	SDCT 03	SDCT 04	SDCT 05	SDCT 06	SDCT 07
WR0B -1	Byte CT (BCT)	BCT 08	BCT 09	BCT 10	BCT 11	BCT 12	0	0	0
-2		BCT 00	BCT 01	BCT 02	BCT 03	BCT 04	BCT 05	BCT 06	BCT 07

Register No.	Name	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
WR0C -1	Byte CT Load Value (BCTLV)	BLV 08	BLV 09	BLV 10	BLV 11	BLV 12	0	0	0
-2		BLV 00	BLV 01	BLV 02	BLV 03	BLV 04	BLV 05	BLV 06	BLV 07
WR0D	CPU Write Data	CPDT 00	CPDT 01	CPDT 02	CPDT 03	CPDT 04	CPDT 05	CPDT 06	CPDT 07
WR0E	Input Format	LMSL	BCKSL	BCKMD	C2SL	LRSL	DPSL	WRSYC	1
WR0F	Reserved	0	0	0	0	0	0	0	0
WR10 -1	NL	NL 16	NL 17	NL 18	NL 19	NL 20	NL 21	0	0
-2		NL 08	NL 09	NL 10	NL 11	NL 12	NL 13	NL 14	NL 15
-3		NL 00	NL 01	NL 02	NL 03	NL 04	NL 05	NL 06	NL 07
WR11 -1	NU	NU 16	NU 17	NU 18	NU 19	NU 20	NU 21	0	0
-2		NU 08	NU 09	NU 10	NU 11	NU 12	NU 13	NU 14	NU 15
-3		0	0	0	NU 03	NU 04	NU 05	NU 06	NU 07
WR12 -1	THUND	UND 16	UND 17	UND 18	UND 19	UND 20	UND 21	UND 22	UND 23
-2		UND 08	UND 09	UND 10	UND 11	UND 12	UND 13	UND 14	UND 15
-3		0	0	0	0	0	0	UND 06	UND 07
WR13 -1	THOVR	OVR 16	OVR 17	OVR 18	OVR 19	OVR 20	OVR 21	OVR 22	OVR 23
-2		OVR 08	OVR 09	OVR 10	OVR 11	OVR 12	OVR 13	OVR 14	OVR 15
-3		0	0	0	0	0	0	OVR 06	OVR 07
WR14 -1	ATRAC Decoder Address Load Value (ACTLV)	ALV 16	ALV 17	ALV 18	ALV 19	ALV 20	ALV 21	0	0
-2		ALV 08	ALV 09	ALV 10	ALV 11	ALV 12	ALV 13	ALV 14	ALV 15
-3		ALV 00	ALV 01	ALV 02	ALV 03	ALV 04	ALV 05	ALV 06	ALV 07

• **Read Register**

Register No.	Name	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
RR00	Interrupt Status	MDSY	PBTXED	RPSEN	OVRFUL	THOVR	THUND	NASEN	SGSY
RR01	Decoder Status	SYOK	NOSY	/	ILSY	WNDLK	EIB	/	/
RR02 -1	Current Header	CHD 24	CHD 25	CHD 26	CHD 27	CHD 28	CHD 29	CHD 30	CHD 31
-2		CHD 16	CHD 17	CHD 18	CHD 19	CHD 20	CHD 21	CHD 22	CHD 23
-3		CHD 08	CHD 09	CHD 10	CHD 11	CHD 12	CHD 13	CHD 14	CHD 15
-4		CHD 00	CHD 01	CHD 02	CHD 03	CHD 04	CHD 05	CHD 06	CHD 07
RR03 -1	Current Subheader	CSH 24	CSH 25	CSH 26	CSH 27	CSH 28	CSH 29	CSH 30	CSH 31
-2		CSH 16	CSH 17	CSH 18	CSH 19	CSH 20	CSH 21	CSH 22	CSH 23
-3		CSH 08	CSH 09	CSH 10	CSH 11	CSH 12	CSH 13	CSH 14	CSH 15
-4		CSH 00	CSH 01	CSH 02	CSH 03	CSH 04	CSH 05	CSH 06	CSH 07
RR04 -1	Current Header Address	CHA 16	CHA 17	CHA 18	CHA 19	CHA 20	CHA 21	/	/
-2		CHA 08	CHA 09	CHA 10	CHA 11	CHA 12	CHA 13	CHA 14	CHA 15
-3		CHA 00	CHA 01	CHA 02	CHA 03	CHA 04	CHA 05	CHA 06	CHA 07
RR05 -1	TX Header	THD 24	THD 25	THD 26	THD 27	THD 28	THD 29	THD 30	THD 31
-2		THD 16	THD 17	THD 18	THD 19	THD 20	THD 21	THD 22	THD 23
-3		THD 08	THD 09	THD 10	THD 11	THD 12	THD 13	THD 14	THD 15
-4		THD 00	THD 01	THD 02	THD 03	THD 04	THD 05	THD 06	THD 07
RR06 -1	TX Subheader	TSH 24	TSH 25	TSH 26	TSH 27	TSH 28	TSH 29	TSH 30	TSH 31
-2		TSH 16	TSH 17	TSH 18	TSH 19	TSH 20	TSH 21	TSH 22	TSH 23
-3		TSH 08	TSH 09	TSH 10	TSH 11	TSH 12	TSH 13	TSH 14	TSH 15
-4		TSH 00	TSH 01	TSH 02	TSH 03	TSH 04	TSH 05	TSH 06	TSH 07
RR07 -1	Drive R/W CT (DCT)	DCT 16	DCT 17	DCT 18	DCT 19	DCT 20	DCT 21	/	/
-2		DCT 08	DCT 09	DCT 10	DCT 11	DCT 12	DCT 13	DCT 14	DCT 15
-3		DCT 00	DCT 01	DCT 02	DCT 03	DCT 04	DCT 05	DCT 06	DCT 07
RR08 -1	ATRAC Encoder/Decoder R/W CT (ACT)	ACT 16	ACT 17	ACT 18	ACT 19	ACT 20	ACT 21	/	/
-2		ACT 08	ACT 09	ACT 10	ACT 11	ACT 12	ACT 13	ACT 14	ACT 15
-3		ACT 00	ACT 01	ACT 02	ACT 03	ACT 04	ACT 05	ACT 06	ACT 07

/: don't care

Register No.	Name	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
RR09 -1	CPU R/W CT (CCT)	CCT 16	CCT 17	CCT 18	CCT 19	CCT 20	CCT 21	/	/
-2		CCT 08	CCT 09	CCT 10	CCT 11	CCT 12	CCT 13	CCT 14	CCT 15
-3		CCT 00	CCT 01	CCT 02	CCT 03	CCT 04	CCT 05	CCT 06	CCT 07
RR0A -1	Sub Data R/W CT (SDCT)	SDCT 16	SDCT 17	SDCT 18	SDCT 19	SDCT 20	SDCT 21	/	/
-2		SDCT 08	SDCT 09	SDCT 10	SDCT 11	SDCT 12	SDCT 13	SDCT 14	SDCT 15
-3		SDCT 00	SDCT 01	SDCT 02	SDCT 03	SDCT 04	SDCT 05	SDCT 06	SDCT 07
RR0B -1	Byte CT (BCT)	BCT 08	BCT 09	BCT 10	BCT 11	BCT 12	/	/	/
-2		BCT 00	BCT 01	BCT 02	BCT 03	BCT 04	BCT 05	BCT 06	BCT 07
RR0C -1	RMS	RMS 16	RMS 17	RMS 18	RMS 19	RMS 20	RMS 21	/	/
-2		RMS 08	RMS 09	RMS 10	RMS 11	RMS 12	RMS 13	RMS 14	RMS 15
-3		RMS 00	RMS 01	RMS 02	RMS 03	RMS 04	RMS 05	RMS 06	RMS 07
RR0D	CPU DATA READ	CPDT 00	CPDT 01	CPDT 02	CPDT 03	CPDT 04	CPDT 05	CPDT 06	CPDT 07
RR0E -1	C2PO Monitor Status	CMS 16	CMS 17	CMS 18	CMS 19	CMS 20	CMS 21	CMS 22	CMS 23
-2		CMS 08	CMS 09	CMS 10	CMS 11	CMS 12	CMS 13	CMS 14	CMS 15
-3		CMS 00	CMS 01	CMS 02	CMS 03	CMS 04	CMS 05	CMS 06	CMS 07
RR0F -1	Ext Monitor Status	DMS 16	DMS 17	DMS 18	DMS 19	DMS 20	DMS 21	DMS 22	DMS 23
-2		DMS 08	DMS 09	DMS 10	DMS 11	DMS 12	DMS 13	DMS 14	DMS 15
-3		DMS 00	DMS 01	DMS 02	DMS 03	DMS 04	DMS 05	DMS 06	DMS 07

/: don't care

1. Register Data I/O

Register data I/O is performed according to the CPU interface timing (described later).
Data is sent MS Byte first (most significant (or higher) byte first) and read LS Bit first. The 1 byte immediately preceding the latch means the address; if these are not selected properly, the data is ignored.

2. Write Registers

(1) Interrupt Control Register (WR00)

By setting each bit of this register to "1", interrupt requests from this IC to the CPU according to the corresponding interrupt status are enabled. As a result, if an enabled interrupt is generated, the XINT pin goes low. The values of each bit of this register have no effect on the corresponding interrupt status.
All status are reset by reading the status from RR00.
Reset is executed when the RR00 address is transferred from SWDT then XSLT is at falling edge.

Bit 0 : MDSY (Sync Interrupt) ... default 0
In playback mode, the MDSY status is set when either the sync pattern is detected within the sync window or after 12 LRCK cycles of the inserted timing. After this status is set, the sync status or header time can be read.

Bit 1 : PBTXED (PB TX End) ... default 0
In playback mode, PBTXED is set according to the timing when the transfer of data to the ATRAC decoder is completed. To be precise, after the transfer byte counter reaches zero, the read FIFO buffer becomes empty, and all of the last byte (8 bits) has been transferred, this bit is set. This bit is not set in auto trigger mode (AUTTRG of WR06).

Bit 2 : RPSEN (Rec Parameter Set Enable) ... default 0
In recording mode, the RPSEN status is set if, when transferring data to the EFM encoder, the recording data parameter values, that is, the TX header (WR02), the TX subheader (WR03) and the sector data type (SC0, SC1 of WR06), are ready to be set.

Bit 3 : OVRFUL (RAM Over or Full) ... default 0
The OVRFUL status is set when the main data area became full while data was being written to it. If WR04 OVRSTP="1", writing to RAM while it is full is prohibited.

Bit 4 : THOVR (Threshold Over) ... default 0
THOVR is set when the condition RMS ≥ THOVR changes from false to true.

Bit 5 : THUND (Threshold Under) ... default 0
THUND is set when the condition RMS < THUND changes from false to true.

Bit 6 : NASEN (Next ATRAC decoder Address Set Enable) ... default 0
In playback mode, this bit is set if, when transferring data in auto trigger mode (AUTTRG of WR06), it is permissible to set the next ACTLV value (WR14).

Bit 7 : SGSY (Sound Group Sync) ... default 0
This bit is set at the first falling edge of the XRQ pin after the pin has been continuously high for 3ms or more. During the exchange of signals with the ATRAC decoder, this pin is set every 11.6ms.

- When the CXD2527R is used as the ATRAC encoder/decoder, SGSY interruption is set every 11.6ms because the data is transferred by the unit of sound group.
- When the CXD2531BR is used as the ATRAC encoder/decoder, it takes 11.6ms for two SGSY interruptions because the data is transferred by the unit of sound flame.

(2) Decoder Control Register (WR01)

Bit 0 : AUTALG (Auto Algorithm) ... default 1

1: Selects the automatic algorithm for the MD sector format decoder sync detection/insertion function.

0: Selects manual mode; operation conforms with the settings of bits 1 through 4 of this register.

The automatic algorithm is equivalent to INSEN=WNDEN=SYDTEN=1; if the protection window detects two consecutive illegal sync (refer to RR01), then the window is reset and opened.

Bit 1 : INSEN (INSEN) ... default 0

1: Sync insertion is performed.

0: Sync insertion is not performed.

Bit 2 : WNDEN (Window Enable) ... default 0

1: The sync protection window is active. Patterns detected outside of the window are treated as illegal sync, and are not used for reset for the insertion timing, etc.

0: The window is open, and all detected sync are valid.

Bit 3 : WNDRST (Window Reset) ... default 0

If this bit is set to 1 and the window is active, the window is reset and opened. After the window is reset, this bit is automatically reset to 0. This function is effective in the event of a track jump, when a new sync is detected and it is desirable to quickly lock the window.

Bit 4 : SYDTEN (Sync Detect Enable) ... default 0

1: Sync detection is enabled.

0: Sync detection is not performed.

Bits 5, 6, 7 : Fixed to 1, 0, 1, respectively.

(3) REC TX Header (WR02) ... default 00, 00, 00, 00

This is a four-byte register. In recording mode, this register specifies the four bytes of the header portion of the sector data being sent to the EFM encoder. The byte order, starting with the MS Byte, corresponds with the cluster number (2 bytes), the sector number (1 byte), and the mode (1 byte).

(4) REC TX Subheader (WR03) ... default 00, 00, 00, 00

This is a four-byte register. In recording mode, this register specifies the four bytes that follow the header data in the sector data being sent to the EFM encoder.

In the MD format, these bytes are all zeros, so these bytes can be left at their default values.

(5) RAM SIZE (WR04)

Bit 0 : RAMSZ 0 ... default 0
Bit 1 : RAMSZ 1 ... default 0
Bit 2 : RAMSZ 2 ... default 0
Specify the RAM size to be used as follows:

RAMSZ2,	RAMSZ1,	RAMSZ0	
=0	0	0	: 1Mbit
=0	0	1	: 2Mbits (1M × 2)
=0	1	0	: 4Mbits
=0	1	1	: 8Mbits (4M × 2)
=1	0	0	: 16Mbits
=1	0	1	: 32Mbits (16M × 2)

Note that when using DRAM, if RAMSZ0=1 it is assumed that two memory chips are being used, and an external circuit is required. Furthermore, A12 output is used as chip select. In addition, 16M DRAM correspond to the 4K refresh type.

Bit 3 : REFSEL (Refresh Select) ... default 0
Selects the refresh cycle.
0: Performs CAS before RAS refresh on DRAM with a cycle of 256 times that of the XTLI input, that is, an 11.3µs cycle.
1: Suited for low-power versions of DRAM, this selects a refresh cycle of 8 times, that is, 90.7µs.

Bit 4 : EXTC2R (External C2PO R/W Mode) ... default 1
0: During playback, C2PO R/W is performed within a single RAM chip based on an address calculated from the main data address using the NU and NL values (WR10, 11).
1: This mode uses external RAM exclusively for C2PO. When using this mode, connect a 1-bit RAM data wire to the ERR pin. In this mode, the C2PO area in main data RAM becomes free area.

Bit 5 : OVRSTP (Overrun Stop) ... default 1
1: Prohibits subsequent writing of the next main data if the main data area becomes full. (In this case, the OVRFUL status in RR00 is set.)
0: Even if the main data area becomes full, writes are not prohibited. As a result, the data write position and data read position may overrun the area. Caution is required, since the RAM capacity remaining is cleared if an overrun occurs.

Bits 6, 7 : Fixed to 0.

(6) SUBDATA CONTROL (WR05)

This register enables/disables R/W access to subdata from the outside via the SBDT, SDCK, XWT, and SRDY pins.

Bit 0 : SBDTEN (Sub Data Access Enable) ... default 0
If this bit is set to 1, the SRDY pin goes low and subdata access from the outside is enabled.

Bit 1 : SBDTDS (Sub Data Access Disable) ... default 0
If this bit is set to 1, the SRDY pin goes high and subdata access from the outside is disabled. If a clock is input from the SDCK pin, it is ignored.
For details on external subdata access, refer to item 4. External Subdata Interface.

Bit 2 : RFRST (Read FIFO Reset)
If this bit is set to 1, the read FIFO buffer within the RI block is reset.

Bit 3 : WFRST (Write FIFO Reset)
If this bit is set to 1, the write FIFO buffer within the RI block is reset.

Bits 4 to 7 : Fixed to 0.

(7) TX Trigger (WR06) ... default 00

This register specifies the trigger and various options when transferring data to the ATRAC decoder or the EFM encoder.

Bit 0 : TXTRG (TX Trigger)

The transfer starts when this bit is set to 1. This bit is actually set in the transfer preparation state; the timing for the actual start of transfer is:

In playback mode, the data is sent after the data is written in the read FIFO buffer and the ATRAC decoder is prepared to receive data (XRQ is low).

In recording mode, the Lch data is sent first, being followed by the sector sync data to EFM encoder, when the SCTX pin is high.

Refer to 3. Operation during Recording.

Bit 1 : TXTERM (TX Terminate)

If this bit is set to 1, the transfer terminates. The actual termination timing is as follows:

In playback mode, reading new data from RAM is prohibited and once the data written in the read FIFO buffer has all been sent, the transfer is terminated and the PBTXED status (RR00) is set.

In recording mode, the transfer is terminated once the sector data currently being sent is transferred.

Bit 2 : Fixed to 0.

Bit 3 : ACHDLD (ATRAC decoder TX Header Load Option)

In playback mode, if this bit is set to "1" at the same time as the TXTRG bit, the initial 8 bytes are not transferred to the ATRAC decoder but are instead loaded into the internal registers RR05 and RR06. The data following the first 9 bytes is sent to the ATRAC decoder.

If the transfer data start address is set to the header data position, the control microcontroller can read the header data of the sector transferred to the ATRAC decoder regardless of the volume of the data stored in memory; based on that address, the microcontroller can calculate and display the playback time, etc.

Bit 4 : BTLD (BCT Load Option)

In playback mode, if this bit is set to "1" at the same time as the TXTRG bit, the value specified by WR0C is loaded into the transfer byte counter (BCT). Using this option eliminates the necessity of setting the BCT each time a transfer is triggered.

Bit 5 : AUTTRG (Auto Trigger Mode)

In playback mode, if this bit is set to "1", the transfer is performed in auto trigger mode. In this mode, when the transfer byte counter (BCT) reaches zero during the data transfer, the value of WR0C is automatically loaded into the BCT and the value of WR14 is automatically loaded into the ACT, and transfer continues without stopping. For details refer to section 2-(4), (b).

Bit 6 : SC0 (Sector Data Select 0)

Bit 7 : SC1 (Sector Data Select 1)

During recording mode, this bit specifies the type of the sector data to be sent to the EFM encoder.

SC1, SC0

=0, 0: Linking data

No data is read from memory; instead, all-zero data is created and transferred.

=0, 1: Main data

The contents of memory based on DCT are read sequentially and sent as sector data.

=1, 0: Subdata

The contents of memory based on SDCT are read sequentially and sent as sector data.

=1, 1: End of transfer

There are two ways of the end of transfer in recording: TXTERM=1 or SC1, SC0=1.1

(8) Drive R/W (WR07) ... default 00, 00, 00

This is a three-byte register that sets the Drive R/W CT (DCT) value.
The counter is a 22-bit counter. In addition, the value should be specified so that the result will fit in the RAM size specified by WR04.

(9) ATRAC encoder/decoder R/W CT (WR08) **... default 00, 00, 00**

This is a three-byte register that sets the ATRAC encoder/decoder R/W CT (ACT) value.

(10) CPU R/W CT (WR09) ... default 00, 00, 00

This is a three-byte register that sets the CPU R/W CT (CCT) value.

(11) SubData R/W CT (WR0A) ... default 00, 00, 00

This is a three-byte register that sets the SubData R/W CT (SDCT) value.

(12) Byte CT (WR08) ... default 1F, FF

This is a two-byte register that sets the Byte CT (BCT) value.
The Byte CT is a 13-bit counter. Set the number of bytes-1 to be transferred. For example, to transfer 2336 bytes, set 2336–1=2335, or 09, 1F.

(13) Byte CT Load Value (WR0C) ... default 00, 00

This is a two-byte register.
In playback mode, specify either the value to be loaded in the BCT by the BCT load position (BTLD of WR06) or the value to be loaded each time in auto trigger mode (AUTTRG of WR06).
In recording mode, set the number of main data bytes, which is:

2352–12 (sync) –8 (header/subheader) –1=2331=09, 1B

(14) CPU Write Data (WR0D)

This is a one-byte register. The data set in this register is written to the memory address indicated by the CCT (WR09), and then the CCT value is incremented.
Write accesses to memory by the microcontroller may sometimes be forced to wait, depending on the status of other access requests within the RI block. Therefore, after sending the memory write data and command and supplying the latch pulse, the memory write operation is not completed as long as the SRDT pin is low, which means the next latch pulse for writing the next data in RAM must not be supplied until the previous operation is completed.
To write the same data continuously, it is possible to do so just by continuing to send the latch pulse; it is not necessary to resend the data and address.
By using this command together with RR0D, the CPU can read/write any address value within memory via WR09.

(15) Input Format Register (WR0E)

This register specifies the interface format from the EFM decoder.

Bit 0 : LMSL (LSB/MSB First Select) ... default 0
- 0: MSB first
- 1: LSB first

Bit 1 : BCKSL (BCK Polarity Select) ... default 0
- 0: Input LRCK and DATA change and are input at the rising edge of BCK.
- 1: Input LRCK and DATA change and are input at the falling edge of BCK.

Bit 2 : BCKMD (BCK Mode) ... default 0
- 0: When BCK has 34 clocks or more during 1 LRCK cycle
- 1: When BCK has 32 input during 1 LRCK cycle

Bit 3 : C2SL (C2PO Byte Order Select) ... default 0
- 0: C2PO MS Byte First
- 1: C2PO LS Byte First

Bit 4 : LRSL (LRCK Polarity Select) ... default 0
- 0: Lch data when LRCK is high, Rch data when LRCK is low
- 1: Lch data when LRCK is low, Rch data when LRCK is high

Bit 5 : DPSL (Data Position Select) ... default 0
- 0: Data is input by rear word truncation against the LRCK edge
- 1: Data is input by front word truncation against the LRCK edge

Bit 6 : WRSYC (Write Mode Synchronization) ... default 1
- 1: Data retrieval starts/stops immediately after sync detection or insertion timing arrives after the WRMN pin logic changes. In other words, after WRMN goes high, retrieval starts with the header data after the sync data, and when WRMN goes low, writing stops after the next sync data is retrieved.
- 0: Write mode starts immediately after WRMN goes high. (To be precise, after WRMN goes high, retrieval starts from the data immediately following the change in polarity of LRCK to the Lch.

Bit 7 : Fixed to 1.

(16) Reserved (WR0F)

(17) NL (WR10) ... default 00, 00, 00

This is a three-byte register that sets the start address of the C2PO area. Set a value equal to the actual value-1. For example, to set NL=123 [H], set the value 00, 01, 02.

(18) NU (WR11) ... default 00, 00, 00

This is a three-byte register that sets the start address of the main data area. The lower 3 bits are fixed to 0, and if these are set to any other values, those values are ignored.

(19) Threshold Value for Running Under (WR12)

This is a three-byte register that sets the threshold value (THUND) for data size comparisons. When RMS < THUND changes from being untrue to true, the RR00 THUND status is set and an interrupt is generated. Note that the lower 6 bits are fixed to 0, and if they are set to any other values, those values are ignored.

(20) Threshold Value for Running Over (WR13)

This is a three-byte register that sets the threshold value (THOVR) for data size comparisons. When RMS ≥ THOVR changes from being untrue to true, the RR00 THOVR status is set and an interrupt is generated. Note that the lower 6 bits are fixed to 0, and if they are set to any other values, those values are ignored.

(21) ATRAC Decoder Load Value (WR14)

This is a three-byte register that sets the value loaded into the ACT at the time of the auto trigger when performing a data transfer in auto trigger mode (AUTTRG of WR06).

3. Read Registers

(1) Interrupt status register (RR00)

Bit 0 : MDSY
Set to "1" if MDSY interrupt is generated.
Bit 1 : PBTXED
Set to "1" if PBTXED interrupt is generated.
Bit 2 : RPSEN
Set to "1" if RPSEN interrupt is generated.
Bit 3 : OVRFUL
Set to "1" if OVRFU interrupt is generated.
Bit 4 : THOVR
Set to "1" if THOVR interrupt is generated.
Bit 5 : THUND
Set to "1" if THUND interrupt is generated.
Bit 6 : NASEN
Set to "1" if NASEN interrupt is generated.
Bit 7 : SGSY
Set to "1" if SGSY interrupt is generated.

For details on each interrupt status, refer to the section WR00 in 2.(1). When a latch is sent after sending from SWDT to RR00 address in order to read this register, all status are cleared.
The MDSY status is set after sync detection or 12 LRCK cycles for insertion timing.

(2) Decoder Status (RR01)

If the MDSY interrupt is generated, the current sector sync and the previous sector information to current sector can be read.

Bit 0 : SYOK This bit is read as "1" when the current sector sync pattern was detected with the same timing as the insertion timing. In other words, this bit indicates that a sync was detected 2352 bytes after the previous sync to the current sector detection or insertion.
Bit 1 : NOSY This bit is read as "1" when sync was not detected within the window.
Bit 2 : Reserved.
Bit 3 : ILSY This bit is read as "1" when sync was detected within the window.
Bit 4 : WNDLK This bit is read as "1" when the sync detection timing and the insertion timing are synchronized and the window is locked.
Bit 5 : EIB This bit is read as "0" if there were no errors (C2PO) in the input data (2352 bytes of header, data and sync) of the previous sector to the current sector, and as "1" if there were errors.
Bit 6, 7 : Reserved.

(3) Current Header (RR02)

This is a four-byte read register. The current header can be read from this register.

Cluster number	CHD31 to 24
Sector number	CHD15 to 08
Mode	CHD07 to 00

(4) Current Subheader (RR03)

This is a four-byte read register. The four bytes following the header can be read from this register.

(5) Current Header Address (RR04)

This is a three-byte read register. In write mode, the address where the first byte of the header of the current sector is written can be read from this register.

(6) TX Header (RR05)

This is a four-byte read register. If the WR06 ACHDLD option was selected for a data transfer to the ATRAC decoder in playback mode, the first eight bytes are not sent to the ATRAC decoder but are instead sent to RR05 and RR06.

Of those eight bytes, this register reads the first four bytes. These bytes show the header of the sector sent to the ATRAC decoder, making it possible for the microcontroller to calculate the playback time without being concerned about the amount of data buffered.

This register is effective during playback when data is transferred with WR06 ACHDLD=1. At least 12µs must be allowed between the falling edge of XSLT for setting WR06 and the falling edge of XSLT for the register read.

(7) TX Subheader (RR06)

This is a four-byte read register. The latter four bytes following RR05 can be read from this register.

(8) Drive R/W CT (DCT) (RR07)

This is a three-byte read register from which the DCT value can be read.

(9) ATRAC Encoder/Decoder R/W CT (ACT) (RR08)

This is a three-byte read register from which the ACT value can be read.

(10) CPU R/W CT (CCT) (RR09)

This is a three-byte read register from which the CCT value can be read.

(11) Sub Data R/W CT (SDCT) (RR0A)

This is a three-byte read register from which the SDCT value can be read.

(12) Byte CT (BCT) (RR0B)

This is a two-byte read register from which the BCT value can be read.

(13) RMS (RR0C)

This is a three-byte read register. RMS can be read from this register with the following values:

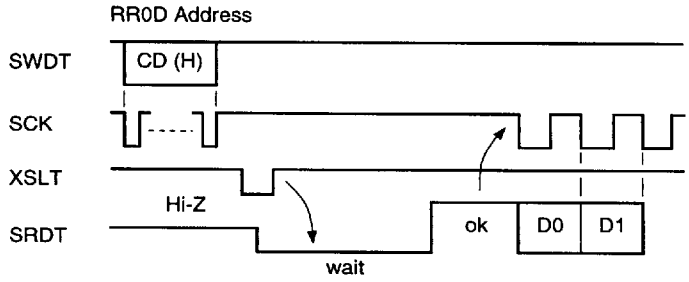
RMS =DCT–ACT (when DCT ≥ ACT)

=(ACT–DCT)+(N–NU) (when ACT > DCT)

(14) CPU DATA READ (RR0D)

This is a one-byte read register from which the microcontroller can read the memory data at the address specified by CCT. After the data is read, the CCT is incremented.

Read accesses to memory by the microcontroller may sometimes be forced to wait, depending on the status of other access requests within the RI block. Therefore, after sending RR0D address for memory reading and making XSLT fall, the memory read operation is not completed as long as the SRDT pin is low, which means the clock for reading data should not be supplied until the previous operation is completed. If the SRDT pin is high, this indicates that the read access has been completed, meaning that the clock can be sent and the data can be read.



(15) C2PO Monitor Status (RR0E)

This is a three-byte read register (CMS23 to 00) from which the C2PO status (number of C2PO errors, starting position, ending position) of the previous input sector data (header, data, sync) to the current sector can be read.

- CMS23 to 20

  Assuming "N" as the number of C2PO errors and "x" as the number represented by the four bits CMS23 to 20, then:

  (when N=0) x =0

  (when N≠0) $2^{x-1} \leq N < 2^x$

In other words, the number of C2PO errors is read out as follows:

CMS23	CMS22	CMS21	CMS20	Number of C2PO errors
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2 to 3
0	0	1	1	4 to 7
0	1	0	0	8 to 15
0	1	0	1	16 to 31
0	1	1	0	32 to 63
0	1	1	1	64 to 127
1	0	0	0	128 to 255
1	0	0	1	256 to 511
1	0	1	0	512 to 1023
1	0	1	1	1024 to 2047
1	1	0	0	2048 to

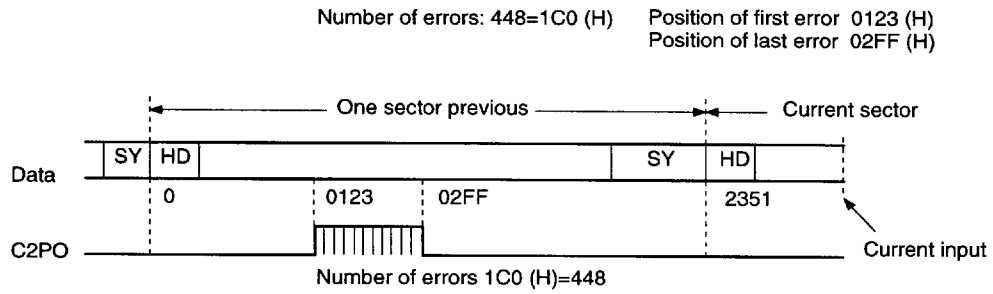
- CMS19 to 08

  Shows the first position where a C2PO error occurred, starting the count at "0" for the first byte of the header. The position is represented as a 12-bit binary value, with CMS19 as the MS Byte and CMS08 as the LS Bit. If there are no errors, these bits are read out all zeros.

- CMS07 to 00

  Indicates the position of the last C2PO error. These bits supply the upper 8 bits of the 12-bit representation of the position from 0 to 2351, with the lower 4 bits omitted. If there are no errors, these bits are read out all

<Example of C2PO Monitor Status>



BIT / Register No.	0	1	2	3	4	5	6	7
RR0E-1	1	0	0	0	1	0	0	1
RR0E-2	1	1	0	0	0	1	0	0
RR0E-3	1	1	1	1	0	1	0	0

The data that is read out in this case is as follows:
In other words, 91, 23, 2F.

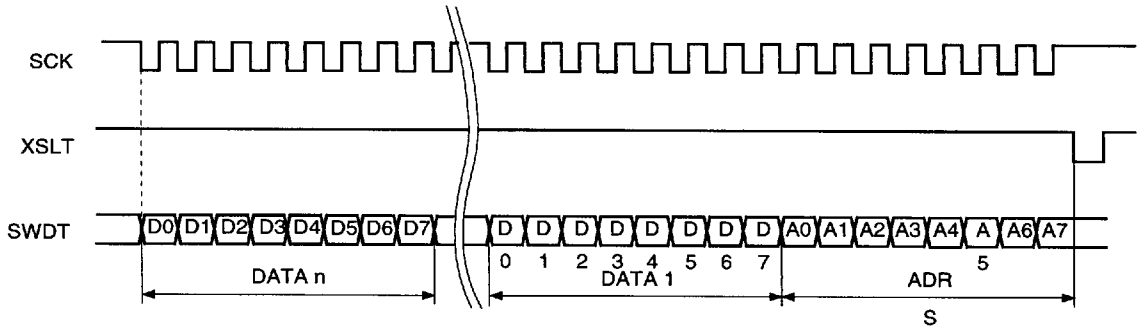
(16) External Monitor Status (RR0F)

This is a three-byte read register.

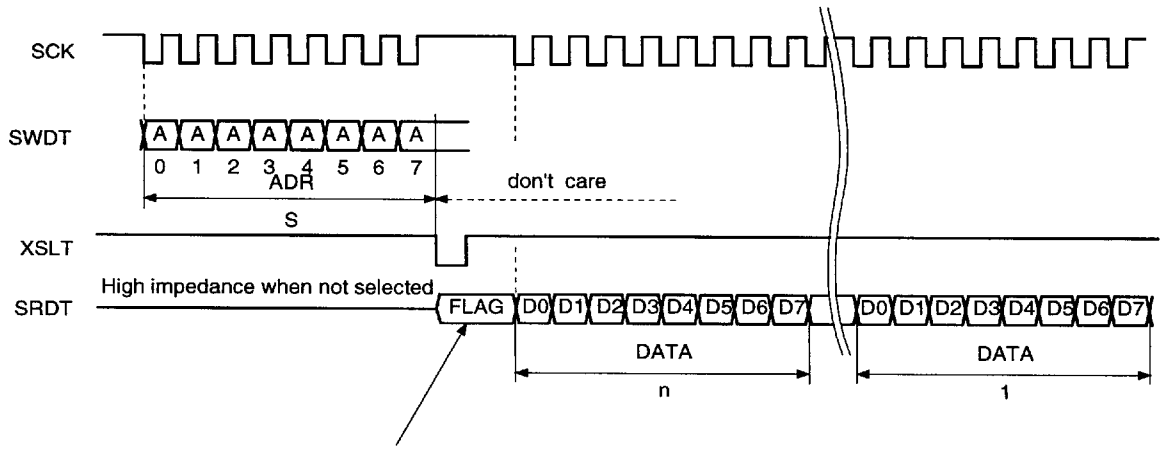
The MIN pin input interface is equivalent to the C2PO pin. The data is retrieved in synchronization with the main data. The data format that is read out is the same as for RR0E.

Microcomputer Interface

Data write



Data read



1) Only during memory read/write by the CPU (RR0D/WR0D):
   Low: wait; high; ready
2) Current header (RR02), Subheader (RR03), TX header (RR05), TX Subheader (RR06)
   Low: C2PO error; high: no C2PO error
3) High in all other cases

A7	A6	A5	A4	Allocation
1	0	0	X	CXD2525
1	0	1	X	CXD2526 Write register
1	1	0	X	CXD2526 Read register
1	1	1	X	CXD2527, CXD2531
0	X	X	X	CXA1082, CXA1602

Data is output LS Bit first (8-bit unit).

Data and Address Transfer Method

Address Setting

The relationship between the address and the register is shown below.
Assuming:
Write register: WRα (ß [H])
Read register: RRα (ß [H])

A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	α	ß [H]				Write register
1	1	0						Read register

Ex.) WR1A address: 10111010
RR0B address: 11001011

Data and Address Transfer

Register data transfer is performed LS Bit first, MS Byte first.
Address transfer is performed LS Bit first.

Write register setting

Ex.) The WR0B setting is as follows:
When
WR0B-1: 1A [H]
WR0B-2: 47 [H]
the transfer sequence is as follows:

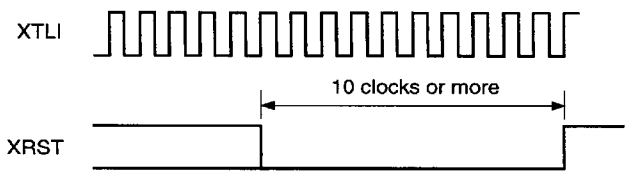
Transfer sequence →

D0 • • • • • D7	D0 • • • • • D7	A0 • • • • • A7
0 1 0 1 1 0 0 0	1 1 1 0 0 0 1 0	1 1 0 1 0 1 0 1
WR0B-1	WR0B-2	WR0B address

Read register data reads

Ex.) In the case of a data read from the current header (RR02), the RR02 address is transferred and then the latch signal (XSLT) is sent. Afterwards, if SRDT is high and there are no C2PO errors, SCK is sent and the data is read in the sequence RR02-1, RR02-2, RR02-3, and RR02-4.

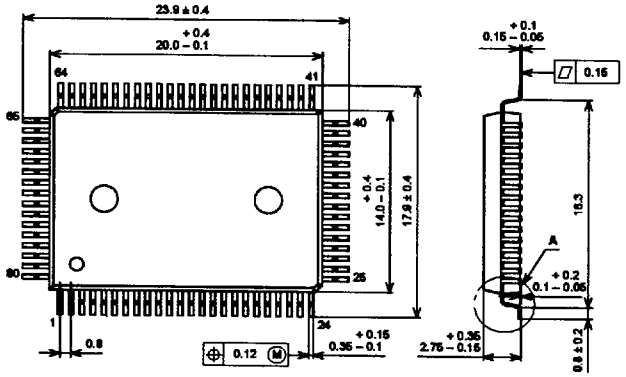
Reset timing



Package Outline Unit: mm

CXD2526AQ

80PIN QFP (PLASTIC)



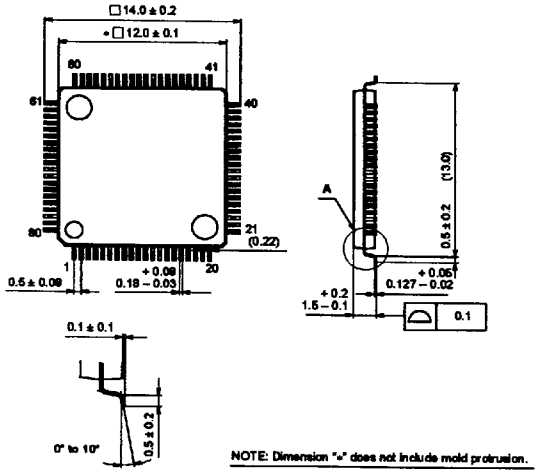
SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY

CXD2526AR

80PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-80P-L01
EIAJ CODE	*QFP080-P-1212-A
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g