VTC Inc.
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VM5317
DATA SEPARATOR

July, 1992

FEATURES

- VM5317 Operates at Data Rates Up to 22Mbit/s Using (1,7) Code
- Static Window Error Less Than 1ns
- Lockup Time Less Than 50 1F Clock Cycles
- User-Determined PLL Loop Filter Network
- External Control of PLL Loop Bandwidth
- Dual Gain PLL Loop
- TTL Control Pins, +5V Referenced ECL Data Signals
- Operates on +5V, +12V Power Supplies
- Available in a 44-Lead PLCC Package

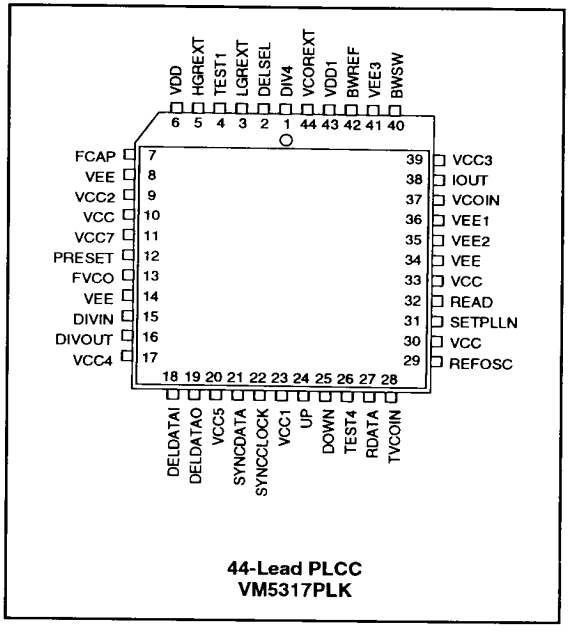
DESCRIPTION

The VM5317 data separator is a bipolar integrated circuit designed to be used in high-performance data recovery systems. The data separator is a phase locked loop which provides a stable read clock of up to 33 MHz for system timing during the disk readback operation. The data clock is recovered from the data stream coming off the disk. It tracks the slow variations in the data frequency but eliminates noise and peak shifting in the data. The VM5317 requires a 3T preamble field and is best suited for (1,7) RLL code. The VM5317 is fabricated using a CBP (complementary bipolar) high-speed process.

The circuit contains the following functional blocks: high-precision phase-frequency detector, charge pump, VCO, bandwidth switch, divider, data standardizer and synchronization control block. Refer to the block diagram.

DATA RECOVERY CIRCUITS

CONNECTION DIAGRAM



44-Lead PLCC
VM5317PLK

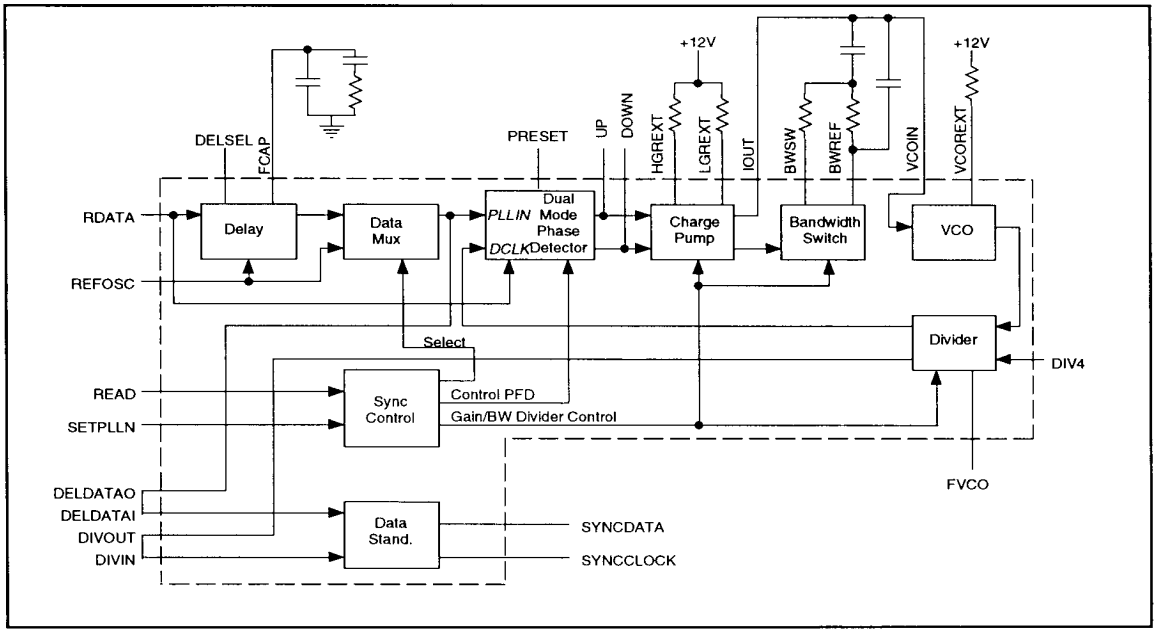
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65° to +150°C
Ambient Operating Temperature	0° to +70°C
Junction Operating Temperature	0° to +125°C
Supply Voltage, V_{CC}	
V_{EE} = 0V, V_{DD} = 12V	-0.5V to + 7.0V
Voltage Applied to TTL Inputs	
V_{EE} = 0V	-0.5V to V_{CC}+ 0.5V
Voltage Applied to ECL Inputs	
V_{EE} = 0V	0 to V_{CC}
ECL Output Current - Continuous	25mA
- Surge	50mA
Maximum Power Dissipation	1300mW
Junction Temperature	150°C
Thermal Impedance, 44-Lead PLCC	
Junction-to-Case, Θ_{JC}	10°C/W
Junction-to-Ambient, Θ_{JA}	53°C/W

RECOMMENDED OPERATING CONDITIONS

Data Rates	7.5 to 15Mbit/s for 1/2 (2,7) RLL code
	7.5 to 22Mbit/s for 2/3 (1,7) RLL code
Operating Temperature	0° to 70°C

BLOCK DIAGRAM



CIRCUIT OPERATION

SYNC Control

The data separator has three modes of operation: lock to reference oscillator, lock to preamble and lock to data. The sync control block uses the READ and SETPLLN control inputs to put each internal block of circuitry into the correct mode. The sync control block controls the input multiplexer, the phase/frequency detector, the charge pump gain, the bandwidth switch, and the divider setting. The data separator must always start in the lock to reference oscillator mode. This is a standby state which the data separator is in when not reading from the disk. In this mode of operation, the REFOSC input is selected, the phase detector is in the phase/frequency mode, the charge pump is in high gain and the divider block is dividing by two. This mode locks the PLL up quickly and guarantees that it is not locked to a harmonic. The lock to preamble mode is the next mode in the read sequence. In this mode, the RDATA input is selected, the phase detector is in the phase frequency mode, the charge pump is in high gain, and the divider is dividing the VCO frequency by 6. This is an asynchronous switch between the REFOSC and RDATA inputs but since their frequency is the same the loop only needs to correct for their phase difference. Once the phase difference has been tracked out by the loop, the data separator is put into the lock to data mode where the data is finally read. In this mode, the RDATA input is selected, the phase detector is in the phase mode, the charge pump is in low gain, and the divider is dividing by 2.

The control pin setting and corresponding modes are summarized in the Table 1.

Delay Line

The VM5317 uses an internal delay line to delay the data coming into the phase detector input. The delay allows the phase/frequency detector to anticipate incoming data and enable a phase comparison to occur. The delay is nominally one half the REFOSC period. A separate on chip PLL locks to the REFOSC frequency and regulates the propagation delay of the delay line. The filter for the delay PLL is external and is tied to the FCAP pin. This delay line configuration relies only on the reference oscillator frequency and is insensitive to external filter components on the FCAP pin, supply voltage,

Table 1: Control Pin Settings

Control Inputs		Modes			
READ	*SETPLLN*	*GAIN*	*MUX SEL*	*DIVIDER*	*PHASE/FREQUENCY DETECTOR*
1	X	high	REFOSC	div by 2	phase/freq mode
0	1	high	RDATA	div by 6	phase/freq mode
0	0	low	RDATA	div by 2	phase mode

1= logic high, 0 = logic low, X = don't care

temperature and IC processing. The data separator requires that the reference oscillator frequency be present at all times. The delay line has two ranges of operation which are controlled by the DELSEL input.

DATAMUX and Phase/Frequency Detector

The two high frequency inputs to the data separator are the REFOSC and the RDATA pins. The REFOSC pin is tied to an external reference oscillator or servo reference. The PLL locks to the REFOSC input when no data is being read from the disk. The RDATA pin is the input for the raw data and is tied to the output of the pulse detector circuit in the disk drive. Because these two signals are the highest frequencies coming on the chip, they are ECL signals. This helps reduce coupling of these signals into sensitive blocks of the PLL on chip. A multiplexer DATAMUX is used to select which input (REFOSC or RDATA) the PLL will lock to.

The output of the multiplexer goes to the PLLIN input of the phase/frequency detector (PFD) block. The phase/frequency detector is a coincidence type detector and has two modes of operation; the phase/frequency mode and phase mode. Each mode is described below.

The phase/frequency mode allows the PFD to detect both phase and frequency of the two incoming signals. This mode does not allow the PLL to lock to harmonics of the reference input. The phase/frequency mode is used along with the charge pump high gain mode to form a high-gain, high-bandwidth loop for fast lock up times. This mode is used when locking to the reference oscillator and the preamble. The PLLIN input to the PFD initiates an UP signal to the charge pump, and the DCLK input initiates a DOWN signal into the charge pump. When both signals are high, the internal flip-flops are reset which brings the UP and DOWN signals low again. The minimum pulse width of the UP and DOWN signals is determined by internal propagation delays and is approximately 8 ns. In a locked state, the rising and falling edges of the UP and DOWN signals are coincident and there is no net effect on the PLL frequency.

When in the phase mode, the PFD detects only the phase of the two inputs. The phase mode is used in conjunction with the charge pump low gain current for slow PLL response. The bit cell window is one period of the DIVOUT signal. The PLL adjusts this window so that the data bit falls in the center. In the phase mode, the PFD remains idle until a rising edge of a data bit is detected. This enables the phase detector to perform a phase comparison on the next rising edges coming into the detector. An internal delay line is used to delay the data coming into the phase detector. This allows the phase detector to anticipate incoming data pulses and perform a phase comparison. The internal delay line automatically adjusts itself so the delay time is one-half the REFOSC frequency or one-half the bit cell window.

Charge Pump

The charge pump is a high-speed, dual gain, bi-directional current source whose current flow is controlled by the digital phase/frequency comparator. The UP and DOWN signals from the PFD feed into the charge pump and cause it to pump current in or out of the lead-lag filter. The current pulses at the IOUT pin reflect the magnitude and sign of the phase error seen at the PFD. The high and low-gain charge pump currents are set by external resistors connected to the HGREXT and LGREXT pins. The high and low-gain currents are 2.0mA and 0.2mA, respectively. This gives a 10:1 current ratio between high and low gain.

Loop Filter and Bandwidth Switch

The charge pump output is filtered by a lead-lag filter before it enters the VCO. The filter resides external to the chip, allowing the system designer to control the loop dynamics (refer to the Typical Application schematic). The basic filter is composed of two capacitors (C11, C12) and one resistor (R11). When changing the PLL gain, it is desirable to change the filter characteristics the same time the charge pump currents are changed. The bandwidth switch allows an additional resistor R10 to be put in parallel with R11, thus changing the DC resistance element in the filter. When the loop is in a high gain mode, the BWSW pin acts as a low impedance voltage source which tracks BWREF. Thus R10 and R11 in parallel form the resistance in the filter. With the loop in low gain, BWSW acts as a high impedance and R10 plays no role in the filter.

VCO

The VCO is a multivibrator type oscillator which has good linearity over its frequency range. The only external component required is an external resistor which sets the VCO center frequency (VCOREXT). The VCO gain is controlled to 15.9MHz/V ± 20%. The output of the VCO feeds into the divider block which allows an optional divide by 2 to be added into the loop. This extra divide by two can be used to extend the lower range of the VCO and is only used at lower data rates. The DIV4 pin switches the extra divide by two in and out. The TEST1 pin puts the divider block into a test mode allowing an external VCO signal to be injected into the loop through the TVCOIN input. The TVCOIN and TEST1 pins are not used in normal operation. The FVCO signal is useful for (1,7) code since it acts as the 3F clock. A 3F clock is often desirable for use in the (1,7) encoder/decoder circuit.

Divider

The divider block switches in an extra divide by 3 or 4 only when the data separator is in the lock to preamble mode. Because this is an asynchronous switch of the PLL input frequency, it is desirable to leave the phase/frequency detector in the phase/frequency mode when locking to the preamble. This prevents the PLL from accidentally locking to a harmonic. To do this, the VCO frequency feeding back into the phase/frequency detector must be divided down by 3 to match the preamble frequency. The VM5317 requires a 3T preamble field which is common for (1,7) RLL code. There is always a divide by two added to the divide by 3, hence a total division of 6.

Data Standardizer

Although the DELDATAO and DIVOUT signals contain the data and clock information needed, DELDATAO is still bit shifted data and must be synchronized with respect to the clock DIVOUT. The data standardizer performs this function. It places the bit shifted data into a bit window and outputs data synchronized to the clock. DELDATAI and DIVOUT are the bit shifted data and clock inputs to the data standardizer; SYNCDATA and SYNCCLOCK are synchronized data and clock outputs of the data standardizer. The rising edge of the clock output SYNCCLOCK is centered in the middle of the data

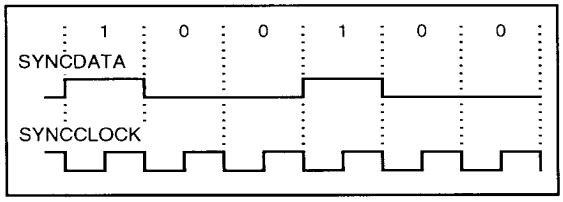


Figure 1: SYNCDATA and SYNCCLOCK Timing

output SYNCDATA. The rising edge of the clock indicates the data is valid and clocks the data bit into the decoder IC of the disk drive (see Figure 1).

PIN DESCRIPTIONS

DIGITAL INPUTS:

DIV4 (TTL): Controls whether an additional divided by 2 is put into the VCO output path. The extra divide by two is used to extend the lower frequency range of the VCO.

DIV4	*MODE*
0	FVCO = VCO freq /2; DIVOUT = VCO freq /4
1	FVCO = VCO freq; DIVOUT = VCO freq /2

DELSEL (TTL): Selects the range for the internal delay line. To determine the logic state for DELSEL, find the REFOSC frequency for the desired data rate; then refer to the table below.

DELSEL	*Delay Range*	*REFOSC Frequency Range*
0	25.0ns to 45.0ns	11.25MHz to 20MHz
1	15.0ns to 25.0ns	20MHz to 33MHz

TEST1 (TTL): Allows the user to break the phase-locked loop and inject an external VCO signal into the divider block through the TVCOIN test input.

TEST1	*MODE*
0	Break PLL loop, inject external VCO signal through TVCOIN
1	Normal operation, closed loop

DIVIN (ECL): Clock input to the data standardizer. Under normal operation, it is driven directly by the DIVOUT ECL output.

DELDATAI (ECL): Data input to the data standardizer. Under normal operation, it is driven directly by the DELDATAO ECL output.

TEST4 (TTL): Allows the user to put the phase detector into a phase-frequency mode when the PLL is in the low gain tracking mode. This enables the DC pump down current to be measured in low gain (which is impossible under normal circuit conditions).

TEST4	*MODE*
0	Phase-frequency mode at all times.
1	Normal operation

RDATA (ECL): Raw data input to the data separator. Data comes from the Pulse Detector Circuit. The input is active on the rising edge. The minimum pulse width is 5ns.

TVCOIN (ECL): This is the test VCO input which allows the user to inject an external VCO signal into the loop when the TEST1 input is in the proper state.

REFOSC (ECL): This is the reference oscillator signal which must be running at all times. The internal delay time is generated from the REFOSC frequency. The REFOSC frequencies for the different data rates and codes are:

DATA RATE (Mbit/s)	*REFOSC frequency (MHz)* 1/2 (2,7)	2/3 (1,7)
22	—	33
15	30	22.5
10	20	15
7.5	15	11.25

REFOSC minimum pulse width high and low: 5ns.

READ and SETPLLN (TTL): These control pins determine the mode of operation for the data separator.

READ	*SETPLL*	*MODE*
0	X	Phase/freq lock to REFOSC, fast PLL tracking
1	1	Phase/freq lock to 3T/4T sync field, fast PLL tracking.
1	0	Phase lock to data, slow PLL tracking.

(see Figure 2).

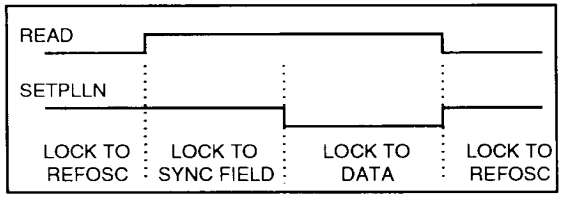


Figure 2: READ and SETPLLN Timing

DIGITAL OUTPUTS:

PRESET (ECL): This is a test point which is asserted whenever the phase detector is enabled for a phase comparison. This output toggles only when reading data in the slow PLL tracking mode.

FVCO (ECL): This is the VCO frequency output or the VCO frequency divided down by two, depending on the logic state of the DIV4 programming input.

DATA RATE (Mbit/s)	*FVCO frequency (MHz)* 1/2 (2,7)	2/3 (1,7)
22	—	66
15	60	45
10	40	30
7.5	30	22.5

The FVCO output serves as the 3F clock when using the 2/3 (1,7) code.

DIVOUT (ECL): This is the VCO frequency output divided down by two or four, depending on the logic state of the DIV4 programming input. DIVOUT is the PLL clock recovered from the input data stream.

DELDATAO (ECL): This is the delayed data which has passed through the internal delay line. When the PLL is locked, the rising edges of DELDATAO and DIVOUT are phase coherent.

SYNCDATA (ECL): This is the synchronized data that has been placed in a bit cell window. The SYNCDATA signal is synchronized to the SYNCCLOCK signal.

SYNCCLOCK (ECL): This is the clock synchronized to the SYNCDATA signal. The rising edge of SYNCCLOCK indicates that the data on SYNCDATA is valid.

UP (ECL): This is a test signal which indicates when the phase detector is commanding the charge pump to source current into the filter node.

DOWN (ECL): This is a test signal which indicates when the phase detector is commanding the charge pump to sink current out of the filter node.

ANALOG SIGNALS:

LGREXT: This pin is tied to +12V through an external resistor which determines the magnitude of the low gain charge pump current. The maximum low gain current allowed is 200μA.

LGREXT resistor (kΩ)	*Low Gain Charge Pump Current (μA)*
39.5	200
79.0	100

HGREXT: This pin is tied to +12V through an external resistor which determines the magnitude of the high gain charge pump current. The maximum high gain current allowed is 2.0mA.

HGREXT resistor (kΩ)	*High Gain Charge Pump Current (mA)*
3.9	2.0
7.8	1.0

FCAP: This is the filter node for delay line PLL. A lead-lag filter referenced to ground is tied to this pin. The voltage on this pin ranges from 1.5 to 3.0 volts.

VCOIN: This is the voltage control input to the VCO which is normally driven by the charge pump output IOUT. A lead-lag filter is also attached to stabilize the PLL. The VCOIN input voltage range is 4.5 to 7.5 volts. The VCO center frequency should be adjusted for each data rate so the VCOIN voltage is nominally at 6 volts.

IOUT: This is the charge pump output which sources or sinks current at the filter node.

BWSW: This is a filter reference pin which can act as a voltage reference or a high impedance. It allows a component to be switched in or out of the lead-lag filter, thus changing the loop response. When in the voltage source mode, BWSW tracks the voltage of BWREF.

VCOREXT: This pin is tied to +12V through an external resistor which determines the VCO center frequency. The table below shows VCO center frequency vs. external resistance.

VCO center frequency vs. VCOREXT resistor value:

DIV4	*VCOREXT (kΩ)*	*Freq at FVCO (MHz)*	*Freq at DIVOUT (MHz)*
0	2.0	30	15
0	2.7	25	12.5
0	4.0	20	10
1	2.0	60	30
1	2.7	50	25
1	4.0	40	20

(VCOIN = 6.0 V)

VOLTAGE SUPPLIES:

VCC: +5V for internal CML digital logic.

VCC1: Analog +5V.

VCC2: +5V for emitter follower collectors in Delay PLL.

VCC4: +5V for collector of DIVOUT ECL output.

VCC5: +5V for collector of DELDATAO ECL output.

VCC7: +5V for collectors of PRESET and FVCO ECL outputs.

VDD: Quiet analog +12V.

VDD1: Noisy analog +12V.

VEE: Digital ground for internal CML logic.

VEE1: Analog ground.

VEE2: Digital ground for emitter followers in Delay PLL.

VEE3: Analog ground for VCO block.

SPECIFICATIONS

VCO Center Frequency: Externally adjustable from 40MHz to 66MHz.

VCO Range: From $0.7 \bullet f_c$ to $1.3 \bullet f_c$, where f_c is the VCO center frequency.

VCO Gain: 10^7 rad/second/volt (15.9 MHz/V). The gain is constant to within ± 20% over the VCO range.

Window Edge Resolution and Window Centering: Window shift less than 1.0ns.

POWER SUPPLIES

SUPPLY	*MIN*	*TYP*	*MAX*	*UNITS*
VEE		0		V
VCC	+4.5	+5.0	+5.5	
VDD	+10.8	+12.0	+13.2	

Maximum Power Dissipation at 25°C = 1380mW

PHASE DETECTOR/CHARGE PUMP GAIN Kp

	HIGH GAIN	*LOW GAIN*
Kp (max)	2.0 mA/rad	0.2 mA/rad

The charge pump gain is linear to within ± 10% over the total operating range. The high gain to low gain ratio is externally controlled for ratios up to 20:1.

ELECTRICAL CHARACTERISTICS Absolute maximum TTL input = 7.0V. TTL inputs will float to a logic high if left unconnected.

ALS TTL Signals
All ALS TTL compatible inputs conform to the following DC parametric specifications, T_A = 25°C.

PARAMETER		*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Inputs	I_{IH}	V_{CC} = 5.5V; V_{IN} = 2.7V			20	µA
		V_{CC} = 5.5V; V_{IN} = 7.0V			100	µA
	I_{IL}	V_{CC} = 5.5V; V_{IN} = 0.5V			–0.6	mA
	V_{IH}		2.0V			V
	V_{IL}				0.8	V

ECL SIGNALS: All inputs and outputs denoted as ECL are +5 Volt referenced MECL 10KH compatible and track with the V_{CC} (+5) supply voltage. The following DC specifications assume V_{CC} is +5.0 Volts.

	T = 0°C		T = 25°C		T = 70°C		
PARAMETER	*MIN*	*MAX*	*MIN*	*MAX*	*MIN*	*MAX*	*UNIT*
V_{OH}	3.98	4.16	4.02	4.19	4.08	4.265	V
V_{OL}	3.05	3.37	3.05	3.37	3.05	3.37	V
V_{IH}	3.83	4.16	3.87	4.19	3.93	4.265	V
V_{IL}	3.05	3.52	3.05	5.52	3.05	3.55	V
I_{INH}		250		250		250	µA
I_{INL}		250		250		250	µA

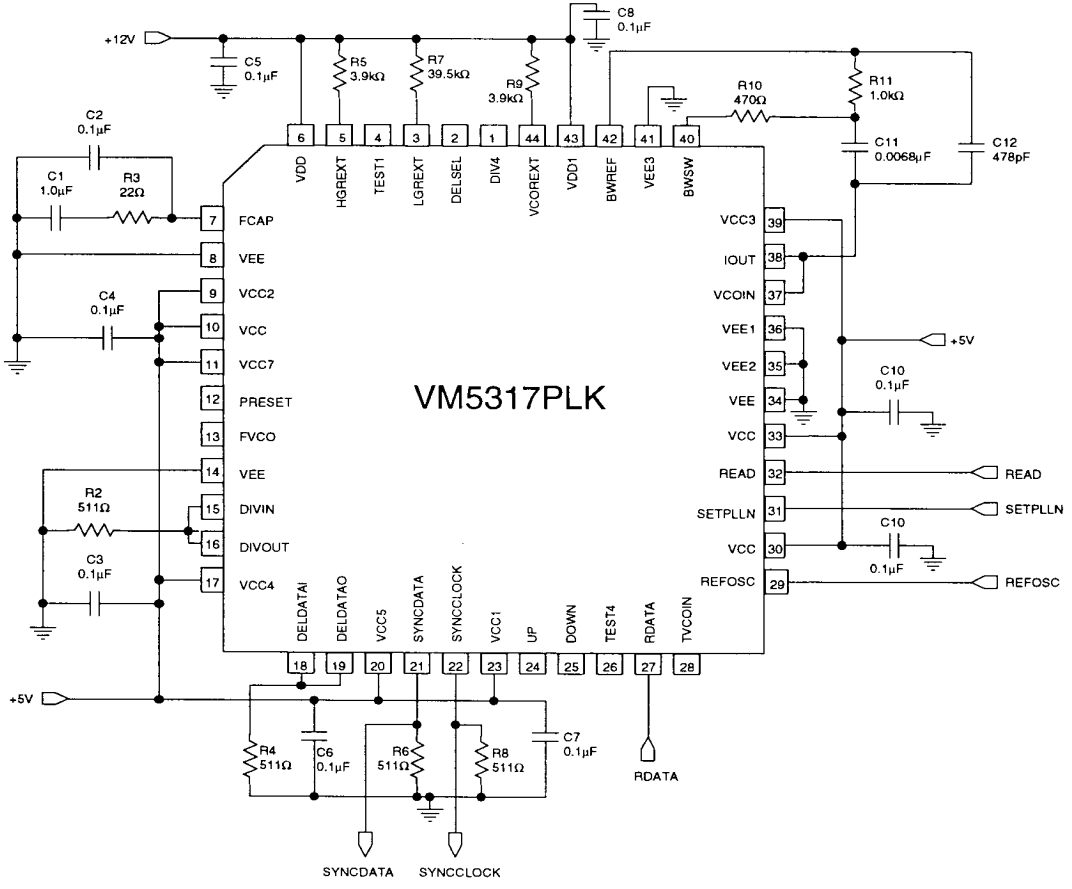
Note: Outputs are terminated into 511Ω to ground. ECL inputs will float to a logic low if left unconnected.

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

The data separator is inherently a sensitive circuit, and thus circuit performance can be degraded significantly without careful attention to board layout. These guidelines should be followed:

1. VCC and VDD supply bypass filtering should be liberal and as close to the supply pins as possible. Ideally, a bypass capacitor should be soldered directly to each supply pin. The electrical lead length of the bypass capacitors between the supply and ground pins should be minimized to reduce lead inductance. Only high quality capacitors should be used.
2. Use the main digital ground plane for all grounding associated with the device.
3. Locate all passive components associated with the chip as close to their respective device pins as possible. It is extremely critical that the PLL filters be very tightly spaced. Chip capacitors and resistors work very well for these filters.
4. For best performance, the chip pins should be soldered directly to the printed circuit board. If a socket must be used, a low profile, low resistance, forced-insertion type socket is recommended.
5. Allow any unused digital outputs to float, unconnected to any other traces.
6. Very fast ECL edge rates should be avoided. Rise/fall times of approximately 2.0ns work well.

TYPICAL APPLICATION



Note: This application board schematic is set up for 10Mbit/s using (2,7) code. The reference oscillator frequency is a 20MHz ECL signal. A charge pump gain ratio of 10:1 has been chosen.