

262,144-word × 1 bit High Speed CMOS Static RAM

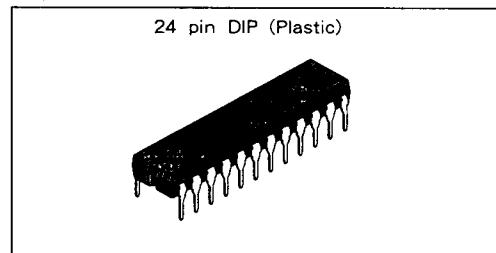
Description

CXK51256P is 262,144-word × 1 bit high speed CMOS static RAM organized as 262,144-word by 1 bit and operates from a single 5V supply.

This device is suitable for use in high speed and low power applications.

Features

- Fast access time (Access time) :
CXK51256P-35 35ns (Max.)
CXK51256P-45 45ns (Max.)
CXK51256P-55 55ns (Max.)
- Low power consumption (operation) :
100mW (Typ.)
- Single + 5V supply : 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Separate data input and output.
- Three-state output.
- Directly TTL compatible : All input and output.
- High density : 300mil 24 pin plastic package



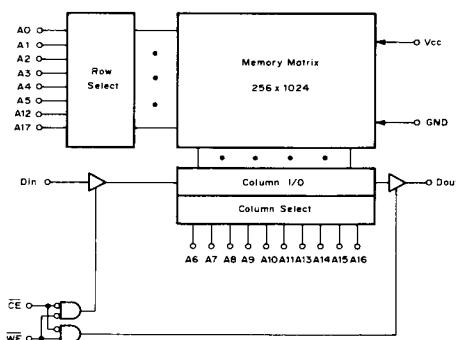
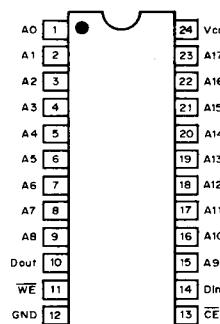
24 pin DIP (Plastic)

Function

262,144-word × 1 bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration
(Top View)****Pin Description**

Symbol	Description
A0 to A17	Address input
Din	Data input
Dout	Data output
CE	Chip enable input
WE	Write enable input
Vcc	+ 5V Power supply
GND	Ground

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Voltage applied to output	V _{OUT}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{OPR}	0 to + 70	°C
Storage temperature	T _{STG}	- 55 to + 150	°C
Soldering temperature	T _{SOLDER}	260 • 10	°C • sec

*Note) V_{CC}, V_{IN}, V_{OUT} min = - 3.5V for pulse width less than 20ns.

Truth Table

C _E	W _E	Mode	Data out	V _{CC} Current
H	X	Not selected	High Z	I _{S81} , I _{S82}
L	H	Read	Data out	I _{C1} , I _{C2}
L	L	Write	High Z	I _{C1} , I _{C2}

X : "H" or "L"

DC Recommended Operating Conditions

T_A = 0 to + 70°C, GND = 0V

Item	Symbol	Min.	Typ.* ¹	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3* ²	—	0.8	V

Note) *1. V_{CC} = 5V, T_A = 25°C

*2. V_{IL} min = - 3.0V for pulse width less than 20ns.

Electrical Characteristics**DC and operating characteristics**V_{CC} = 5V ± 10 %, GND = 0V, Ta = 0 to + 70°C

Item	Symbol	Test condition	- 35/45/55			Unit
			Min.	Typ.	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC} V _{CC} = 5.5V	- 1	—	1	μA
Output leakage current	I _{LO}	CĒ = V _{IH} V _{OUT} = GND to V _{CC}	- 1	—	1	μA
Operating power supply current	I _{CC1}	CĒ = V _{IL} , I _{OUT} = 0mA, V _{IN} = V _{IH} /V _{IL}	—	20	45	mA
Average operating current	I _{CC2}	Cycle = Min., Duty = 100 % I _{OUT} = 0mA	—	55	85	mA
Standby current	I _{SB1}	CĒ ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	2	mA
	I _{SB2}	CĒ = V _{IH}	—	15	30	mA
Output high voltage	V _{OH}	I _{OH} = - 4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

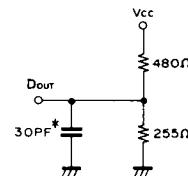
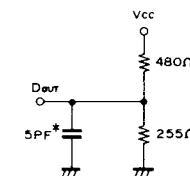
I/O capacitance

Ta = 25 °C, f = 1MHz

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V	—	7	pF

Note) This parameter is sampled and is not 100 % tested.**AC characteristics****• AC test conditions**V_{CC} = 5V ± 10 %, Ta = 0 to + 70°C

Item	Condition
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _R = 5ns
Input fall time	t _F = 5ns
Input and output timing reference level	1.5V
Output load	Fig. 1

Output Load (1)**Output Load (2)****

* Including scope and jig

** For tLz, thz, tow, twhz

Fig. 1

Read cycle

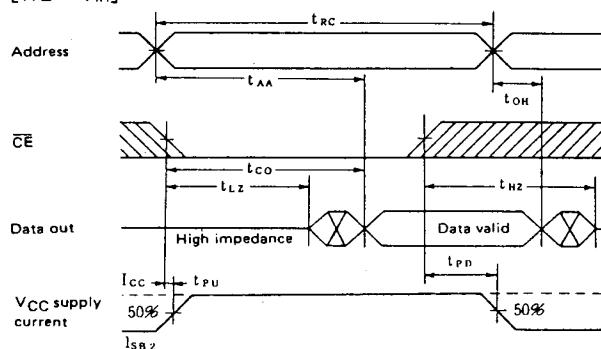
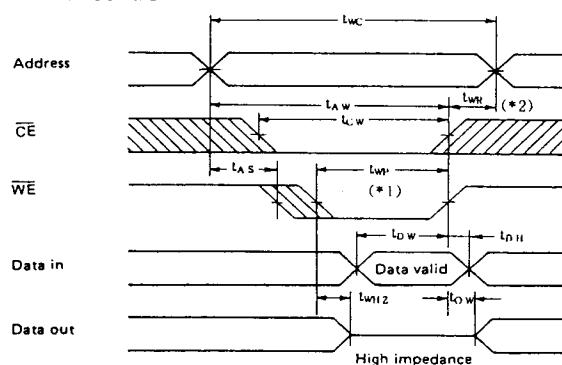
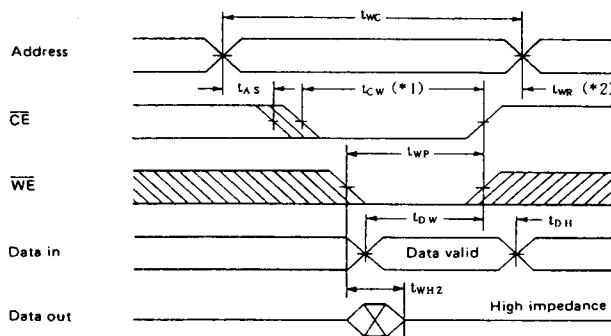
Item	Symbol	- 35		- 45		- 55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	35	—	45	—	55	—	ns
Address access time	t _{AA}	—	35	—	45	—	55	ns
Chip enable access time (CE)	t _{CO}	—	35	—	45	—	55	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE)	t _{LZ} *	5	—	5	—	5	—	ns
Chip disable to output in high Z	t _{HZ} *	0	20	0	20	0	25	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	30	—	30	—	30	ns

* Note) Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.
This parameter is sampled and is not 100% tested.

Write cycle

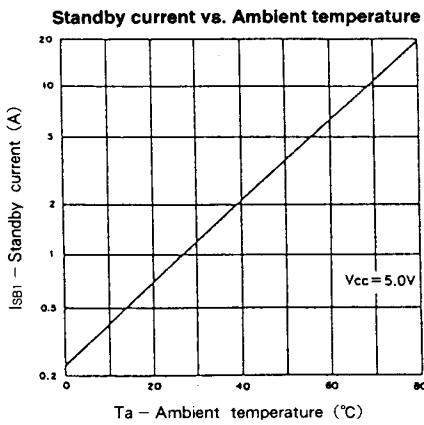
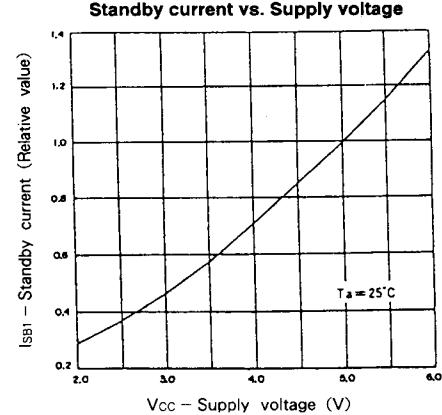
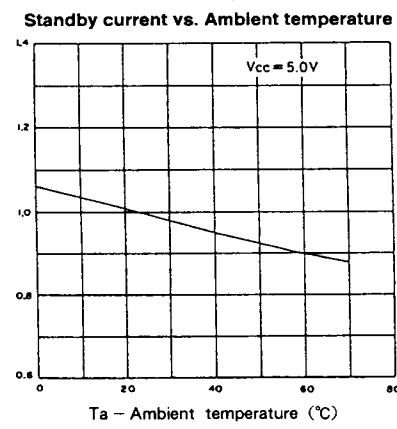
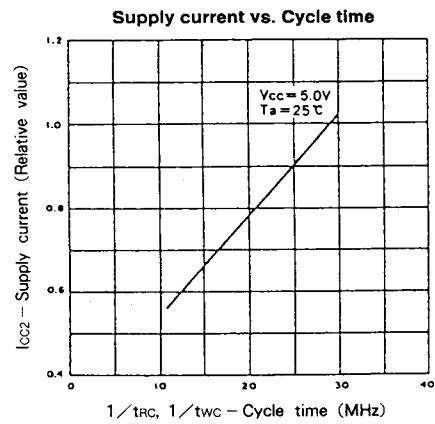
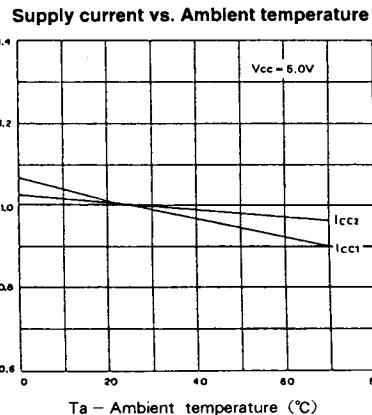
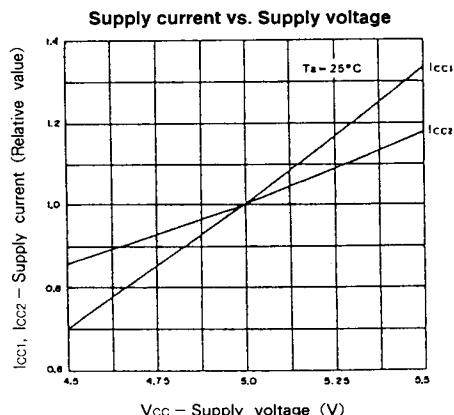
Item	Symbol	- 35		- 45		- 55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t _{AW}	30	—	35	—	45	—	ns
Chip enable to end of write	t _{CW}	30	—	35	—	45	—	ns
Data to write time overlap	t _{DW}	20	—	25	—	25	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	25	—	25	—	35	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	20	0	20	0	25	ns

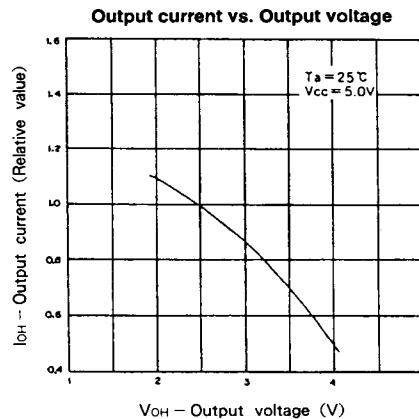
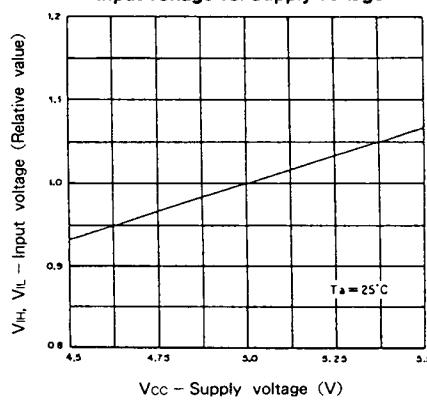
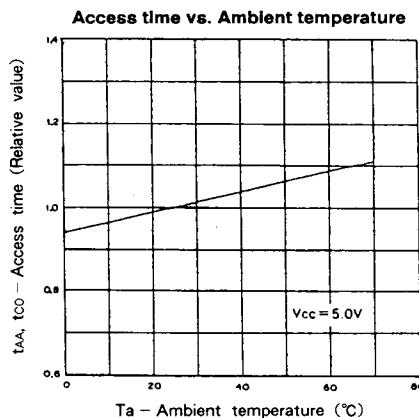
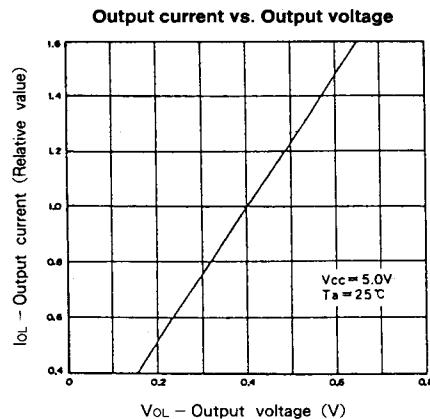
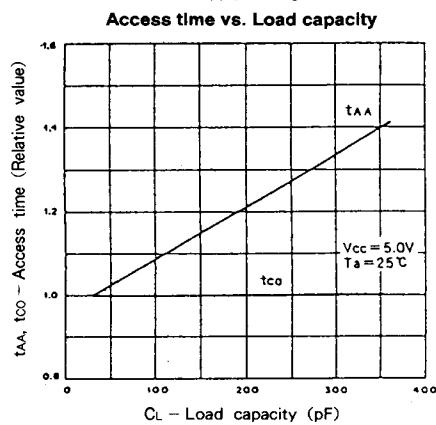
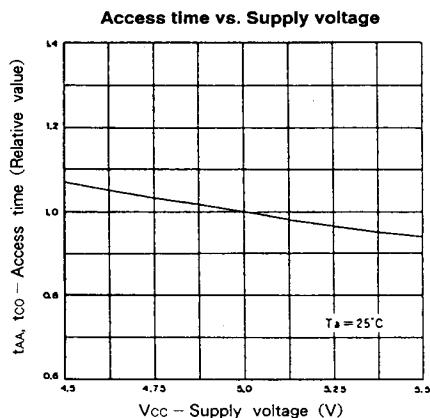
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This parameter is sampled and is not 100% tested.

Timing Waveform**1) Read cycle [$\overline{WE} = V_{IH}$]****2) Write cycle****• Write cycle 1 : \overline{WE} control****• Write cycle 2 : \overline{CE} control***** Note)**

1. A write occurs during the low overlap of \overline{CE} and \overline{WE} .
2. t_{WR} is measured from the earlier of \overline{CE} or \overline{WE} going high to the end of write cycle.

Example of Representative Characteristics





Package Outline Unit : mm

24 pin DIP (Plastic) 300mil 1.5g

