SONY

CXK581000ATM/AYM/AM -10LLB

131072-word × 8-bit High Speed CMOS Static RAM

Description

The CXK581000ATM/AYM/AM is a high speed CMOS static RAM organized as 131072 words by 8 bits.

A polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

Special feature are low power consumption, high speed and broad package line-up.

The CXK581000ATM/AYM/AM is a suitable RAM for portable equipment with battery back up.

Features

- Wide supply voltage range operation: 2.7 to 5.5V
- Fast access time: (Access time)
  - 3V Operation 150ns (Max.)
  - 5V Operation 100ns (Max.)
- Low standby current
  - 3V Operation 14μA (Max.)
  - 5V Operation 20μA (Max.)
- Low voltage data retention: 2.0 V (Min.)
- Broad package line-up

  CXK581000ATM/AYM

  8mm × 20mm 32 pin TSOP package

  CXK581000AM

  525mil 32 pin SOP package

Function

131072 word × 8 bit static RAM

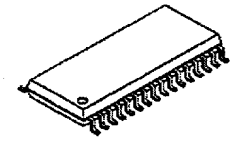
Structure

Silicon gate CMOS IC

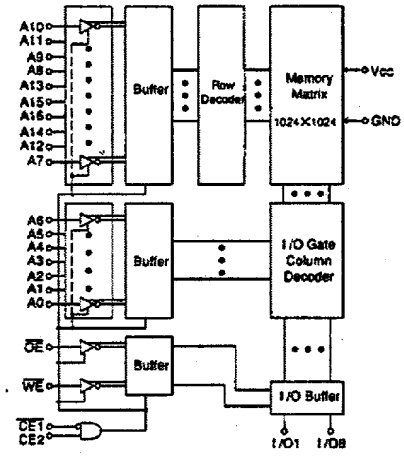
CXK581000ATM
32 pin TSOP (Plastic)

CXK581000AYM
32 pin TSOP (Plastic)

CXK581000AM
32 pin SOP (Plastic)

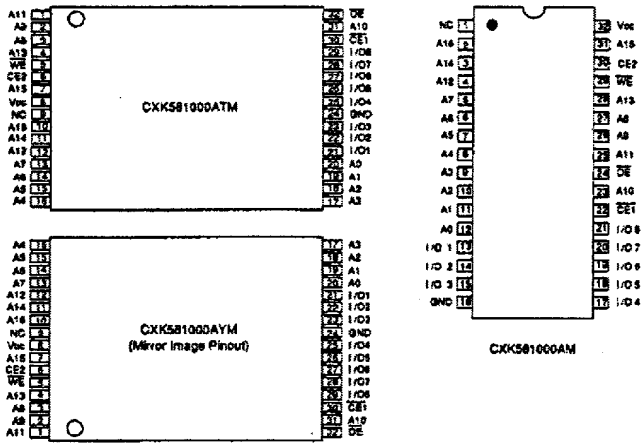


Block Diagram



E94411-TE

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings (Ta=25°C, GND=0 V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5 to +7.0	V
Input voltage	VIN	−0.5* to Vcc+0.5	
Input and output voltage	VI/O	−0.5* to Vcc+0.5	
Allowable power dissipation	PD	0.7	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	
Soldering temperature	Tsolder	235 · 10	°C · s

*VIN VI/O=−3.0 V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	Vcc current
H	×	×	×	Not selected	High Z	ISB1, ISB2
×	L	×	×	Not selected	High Z	ISB1, ISB2
L	H	H	H	Output disable	High Z	ICC1, ICC2, ICC3
L	H	L	H	Read	Data out	ICC1, ICC2, ICC3
L	H	×	L	Write	Data in	ICC1, ICC2, ICC3

×: "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0 V)

Item	Symbol	Vcc=5V±10%			Vcc=2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	VIH	2.2	—	Vcc+0.3	2.2	—	Vcc+0.3	
Input low voltage	VIL	−0.3*	—	0.8	−0.3*	—	0.4	

*VIL=−3.0 V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics (GND=0 V, Ta=0 to +70°C)

Item	Symbol	Test conditions		Vcc=3V±10%			Vcc=5V±10%			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		−1	—	1	−1	—	1	µA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to Vcc		−1	—	1	−1	—	1	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH} V_{IN}=V_{IH} or V_{IL} I_{OUT}=0mA		—	0.5	1.3	—	7	15	mA
Average operating current	I_{CC2}	Min. cycle duty=100% I_{OUT}=0mA		—	14	23	—	35	60	mA
	I_{CC3}	Cycle time 1µs duty=100% I_{OUT}=0mA $\overline{CE1}$≦0.2V CE2≧Vcc−0.2V V_{IL}≦0.2V V_{IH}≧Vcc−0.2V		—	3	7	—	10	20	mA
Standby current	I_{SB1}	CE2≦0.2V or $\overline{CE1}$≧Vcc−0.2V	0 to +70°C	—	—	14	—	—	20	µA
			0 to +40°C	—	—	2.8	—	—	4	µA
		CE2≧Vcc−0.2V	+25°C	—	0.4	1.4	—	0.7	2	µA
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	0.06	0.3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH}=−1.0mA		2.2	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Ta=25°C

I/O capacitance (Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	8	

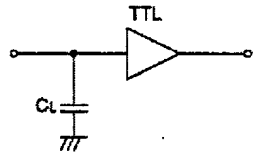
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions (V_{CC}=2.7 to 5.5V, Ta=0 to +70°C)

Item	Conditions	
	V_{CC}=3V±10%	V_{CC}=5V±10%
Input pulse high level	V_{IH}=2.2 V	V_{IH}=2.2 V
Input pulse low level	V_{IL}=0.4 V	V_{IL}=0.8 V
Input rise time	tr=5ns	tr=5ns
Input fall time	tf=5ns	tf=5ns
Input and output reference level	1.5 V	1.5 V
Output load conditions	C_L*=100pF, 1TTL	C_L*=100pF, 1TTL

• Test circuit



* CL includes scope and jig capacitances.

• Read cycle ($\overline{WE}$="H")

Item	Symbol	Vcc=3V±10%		Vcc=5V±10%		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	tRC	150	—	100	—	ns
Address access time	tAA	—	150	—	100	
Chip enable access time ($\overline{CE1}$)	tCO1	—	150	—	100	
Chip enable access time (CE2)	tCO2	—	150	—	100	
Output enable to output valid	tOE	—	70	—	50	
Output hold from address change	tOH	15	—	15	—	
Chip enable to output in low Z ($\overline{CE1}$, CE2)	tLZ1,tLZ2	10	—	10	—	
Output enable to output in low Z ($\overline{OE}$)	tOLZ	5	—	5	—	
Chip disable to output in high Z ($\overline{CE1}$, CE2)	tHZ1*,tHZ2*	—	50	—	35	
Output disable to output in high Z ($\overline{OE}$)	tOHZ*	—	50	—	35	

* tHZ1, tHZ2 and tOHZ are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

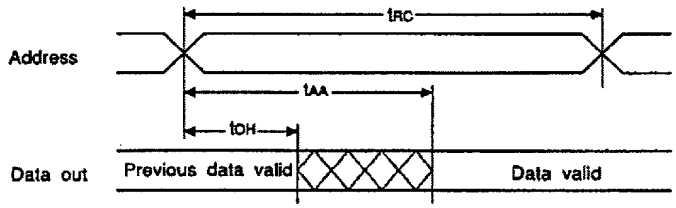
• Write cycle

Item	Symbol	Vcc=3V±10%		Vcc=5V±10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	tWC	150	—	100	—	ns
Address valid to end of write	tAW	100	—	70	—	
Chip enable to end of write	tCW	100	—	70	—	
Data to write time overlap	tDW	60	—	40	—	
Data hold from write time	tDH	0	—	0	—	
Write pulse width	tWP	90	—	70	—	
Address setup time	tAS	0	—	0	—	
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	
Write recovery time ($\overline{CE1}$, CE2)	tWR1	0	—	0	—	
Output active from end of write	tOW	10	—	10	—	
Write to output in high Z	tWHZ*	—	30	—	30	

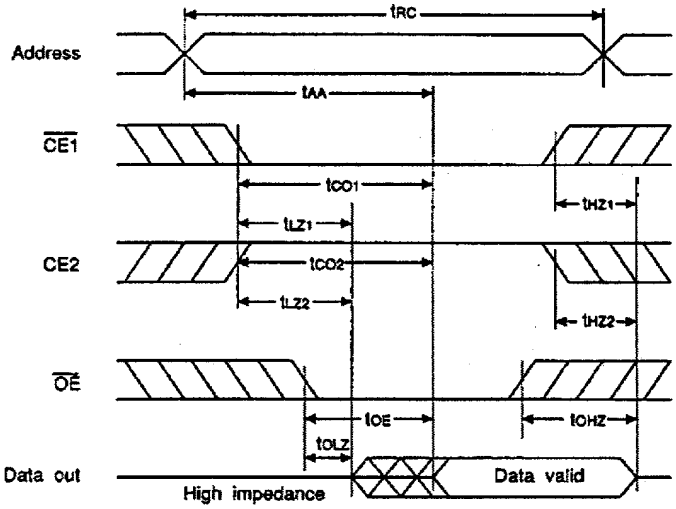
* tWHZ is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

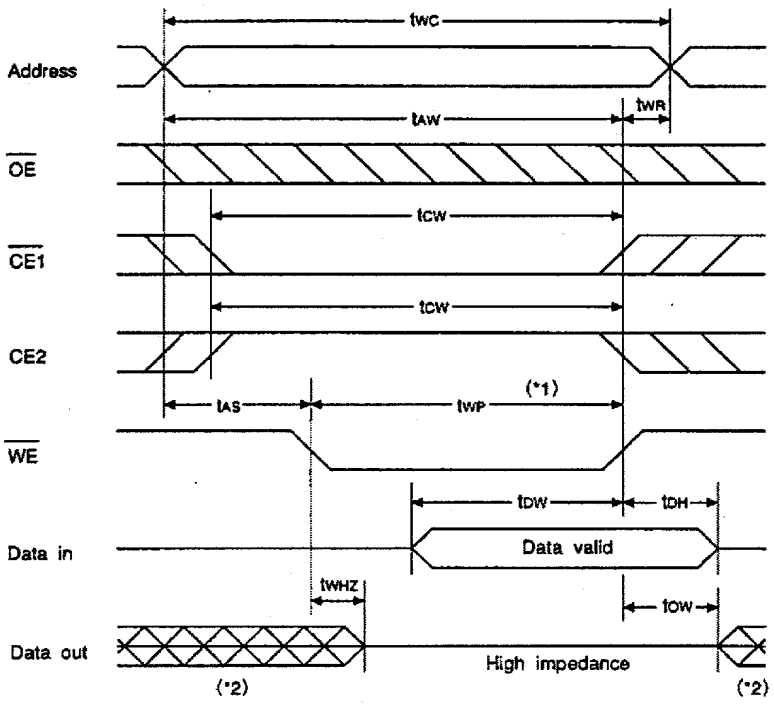
• Read cycle (1): $\overline{CE1}$=$\overline{OE}$=VIL, CE2=VIH, $\overline{WE}$=VIH



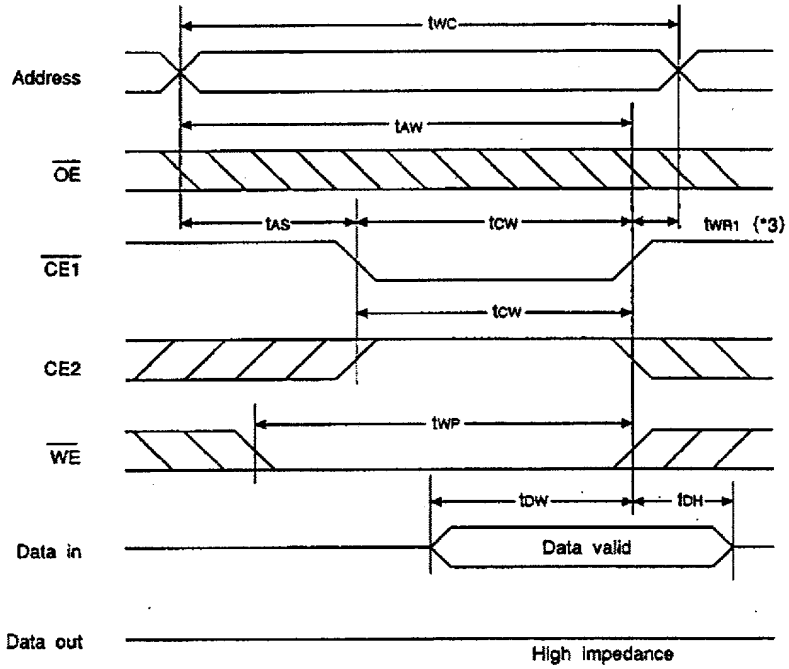
• Read cycle (2): $\overline{WE}$=VIH



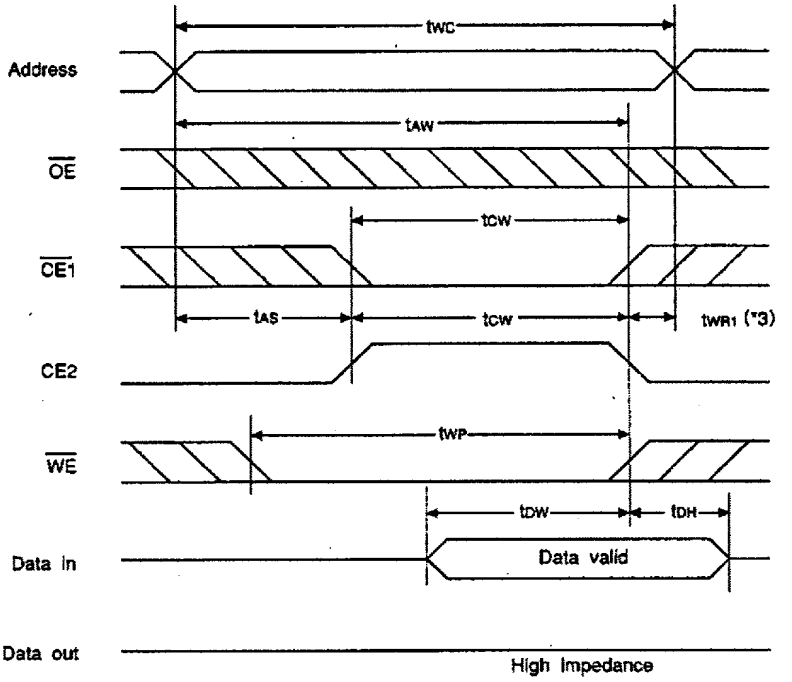
• Write cycle (1): $\overline{WE}$ control



• Write cycle (2): $\overline{CE1}$ control



• Write cycle (3): CE2 control



Note)

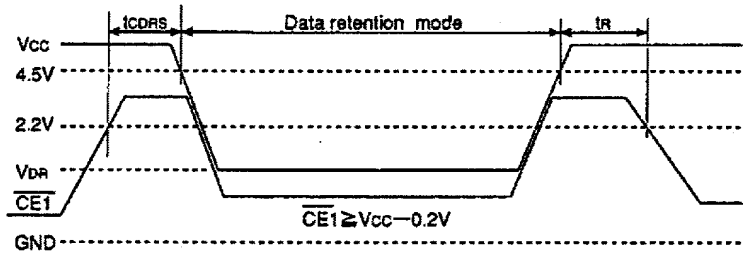
*1 Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

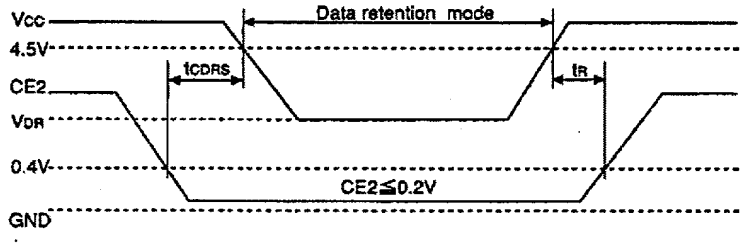
*3 t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data retention waveform

• Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



• Low supply voltage data retention waveform (2) (CE2 control)



Data Retention Characteristics (Ta=0 to 70°C)

Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	*1		2.0	—	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0 V*1	0 to +70°C	—	—	12	μA
			0 to +40°C	—	—	2.4	
			+25°C	—	0.4	1.2	
	I_{CCDR2}	V_{CC}=2.0 to 5.5 V*1		—	0.7*2	20	
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t_R			5	—	—	ms

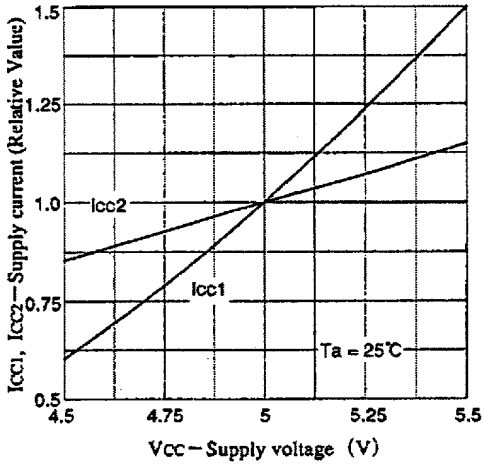
Note)

*1 $\overline{CE1}$≧Vcc−0.2 V, CE2≧Vcc−0.2 V [$\overline{CE1}$ control] or CE2≦0.2 V [CE2 control]

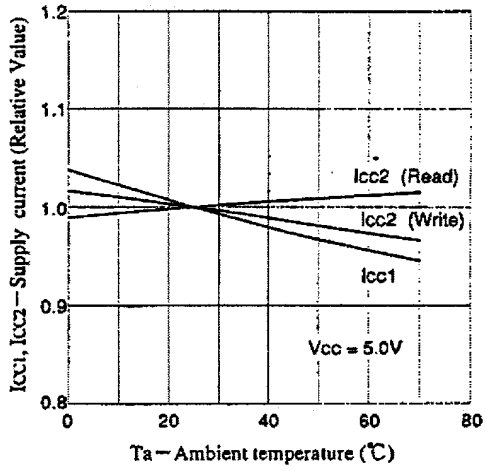
*2 Vcc=5 V, Ta=25°C

Example of Representative Characteristics

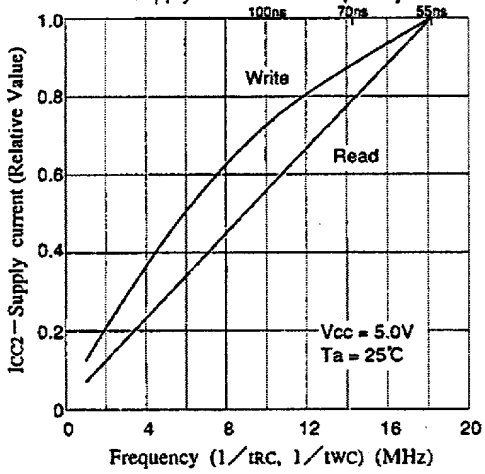
Supply current vs. Supply voltage



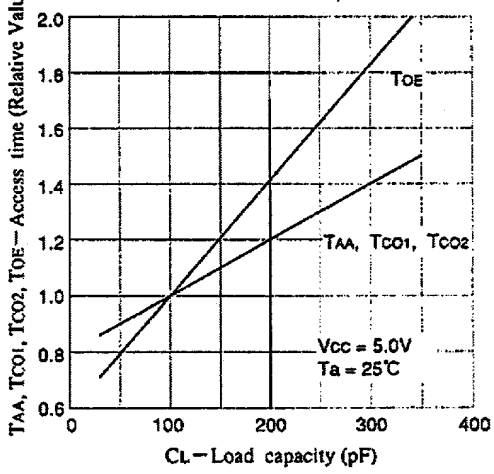
Supply current vs. Ambient temperature



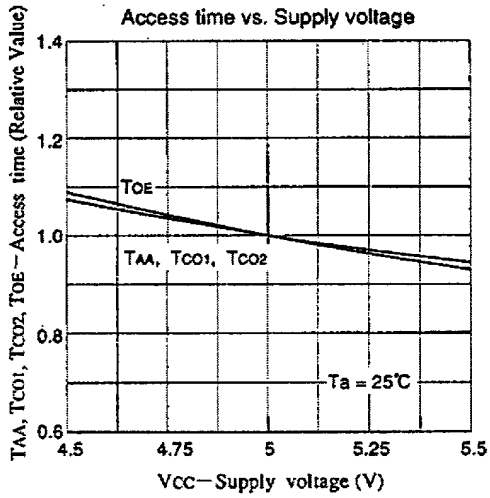
Supply current vs. Frequency



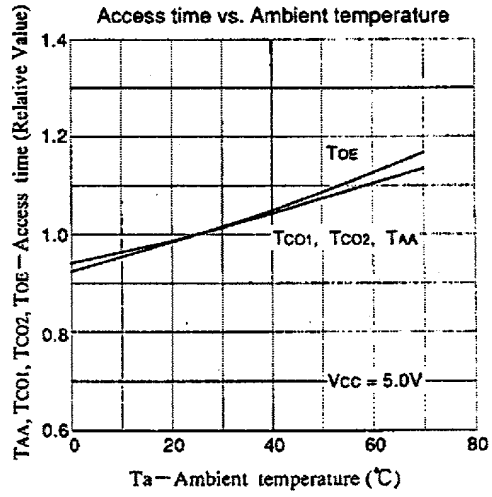
Access time vs.Load capacitance



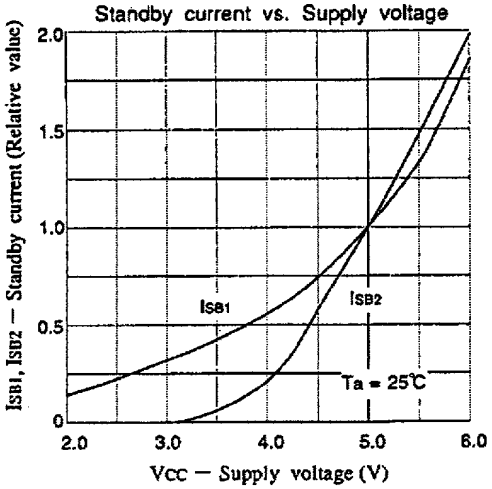
Access time vs. Supply voltage



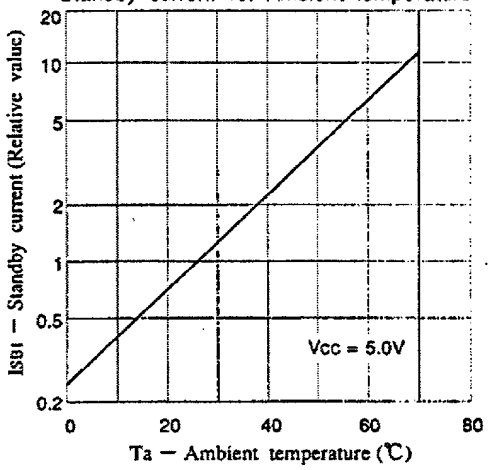
Access time vs. Ambient temperature



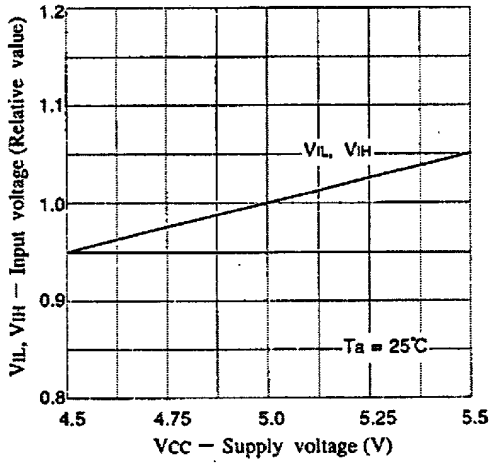
Standby current vs. Supply voltage



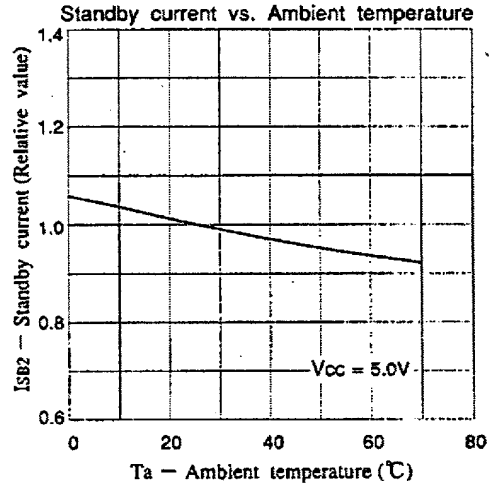
Standby current vs. Ambient temperature



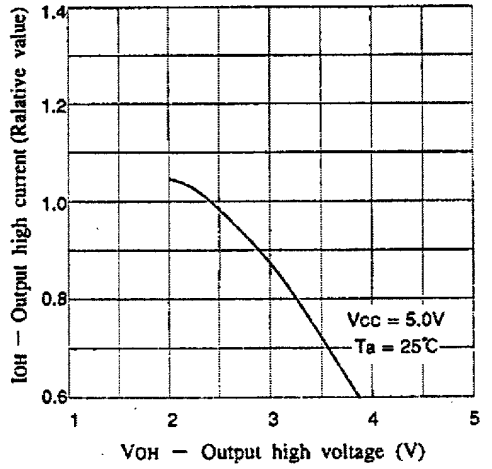
Input voltage level vs. Supply voltage



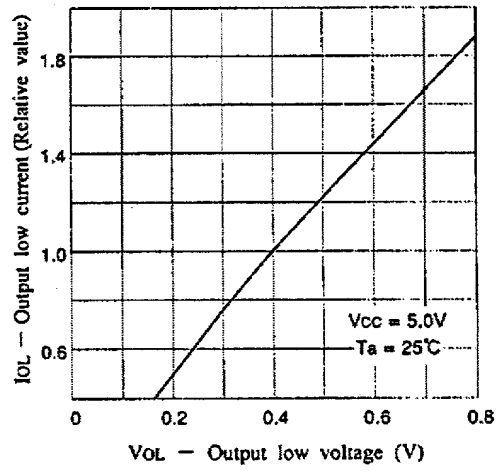
Standby current vs. Ambient temperature



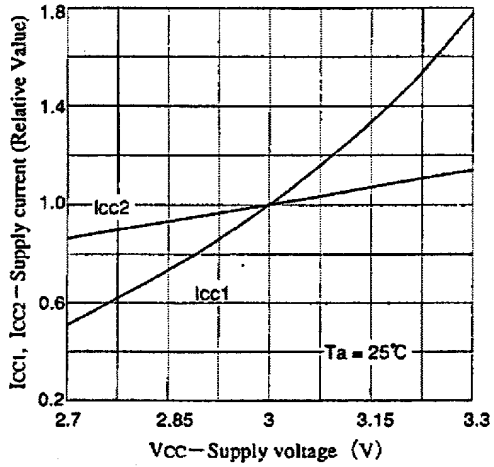
Output high current vs. Output high voltage



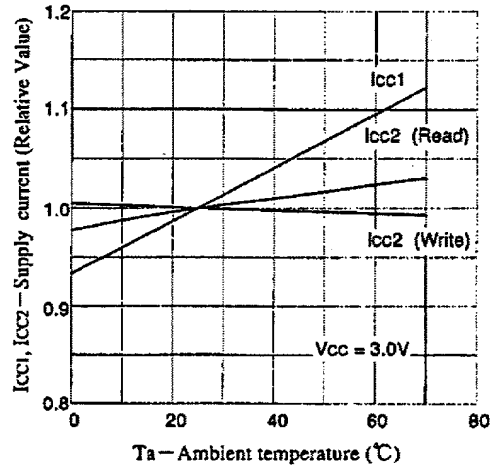
Output low current vs. Output low voltage



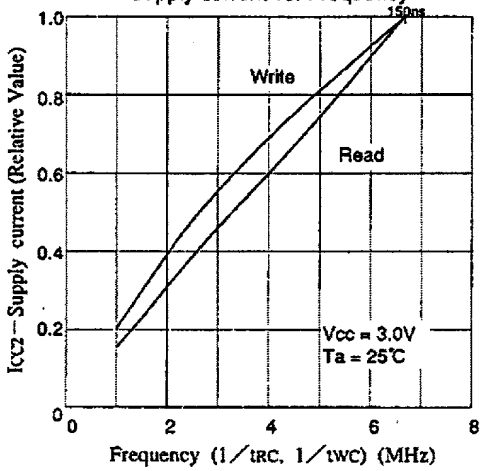
Supply current vs. Supply voltage



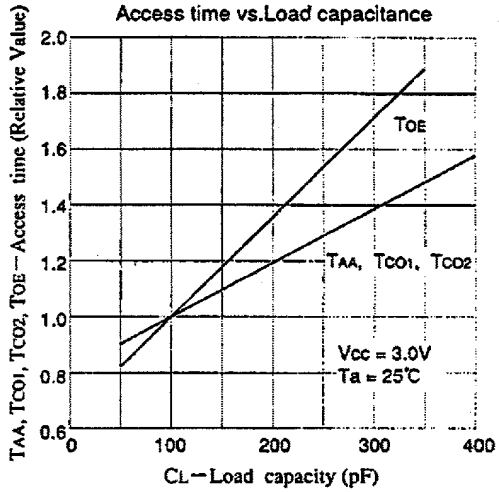
Supply current vs. Ambient temperature



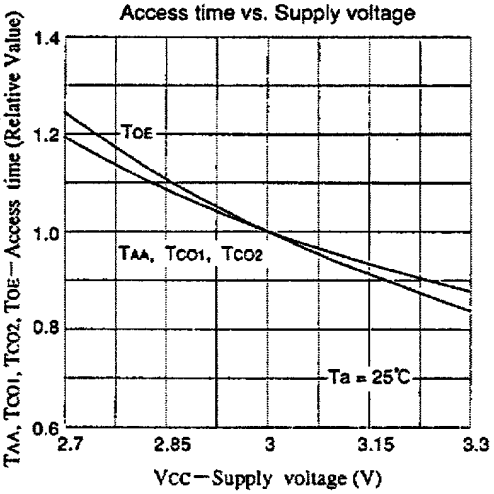
Supply current vs. Frequency



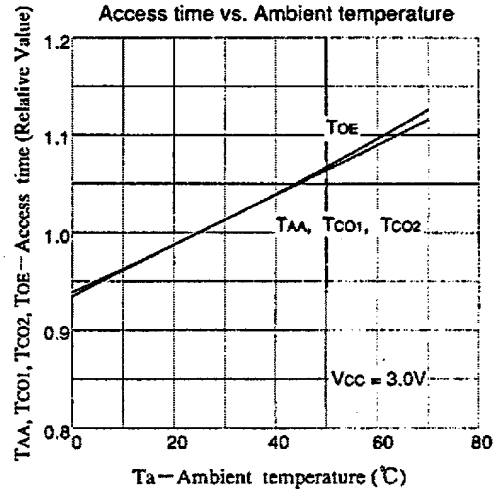
Access time vs.Load capacitance



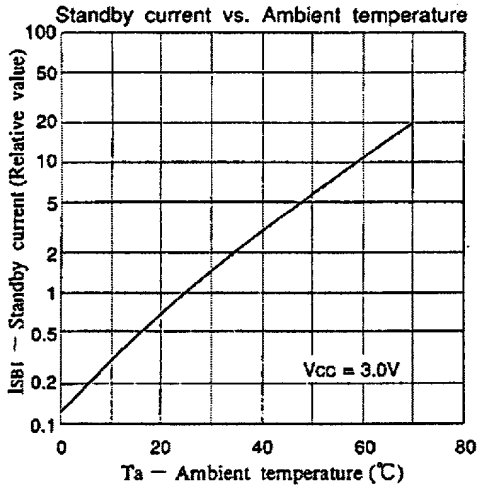
Access time vs. Supply voltage



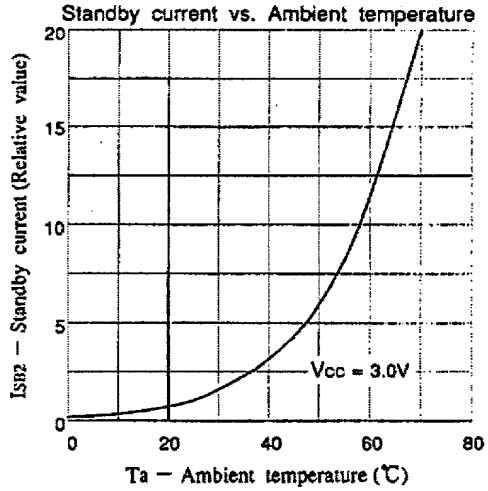
Access time vs. Ambient temperature



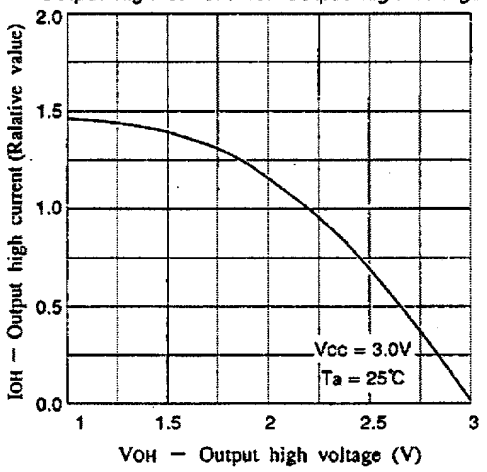
Standby current vs. Ambient temperature



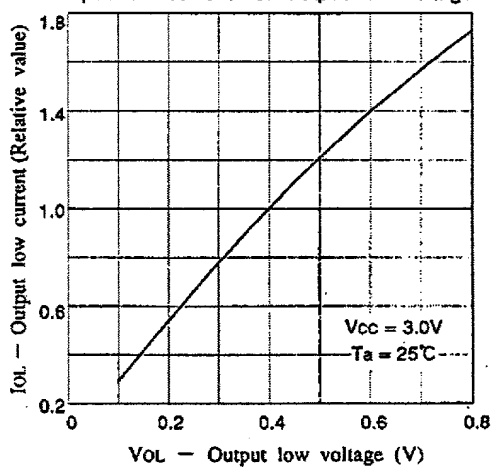
Standby current vs. Ambient temperature



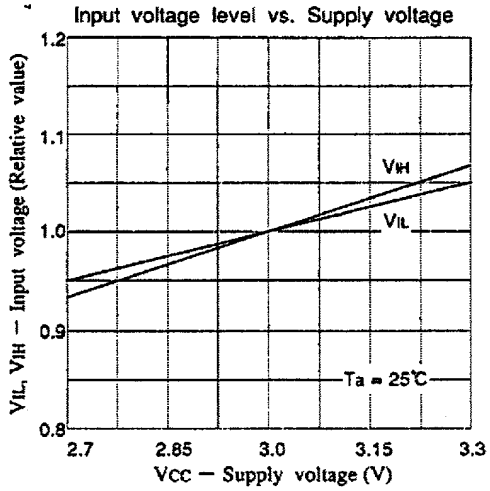
Output high current vs. Output high voltage



Output low current vs. Output low voltage



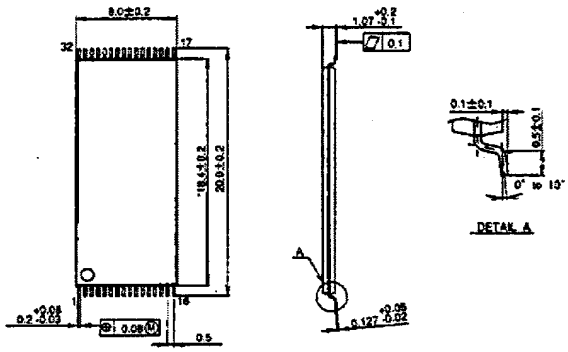
Input voltage level vs. Supply voltage



Package Outline Unit : mm

CXK581000ATM

32PIN TSOP(PLASTIC)



NOTE : *NOT INCLUDE MOLD FINS.

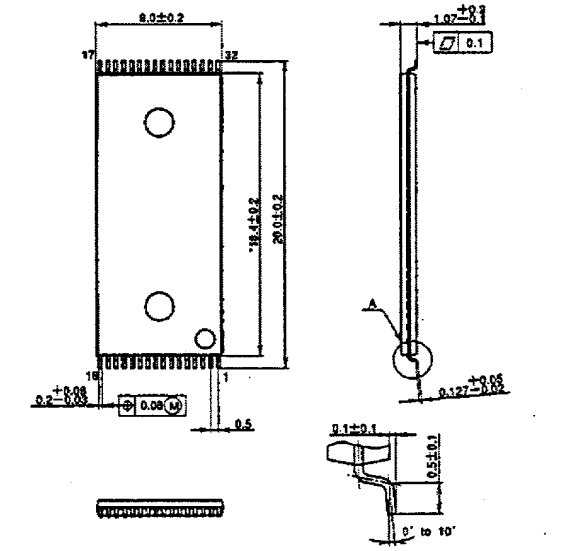
PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01
EIAJ CODE	TSOP032-P-0820-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g

CXK581000AYM

32PIN TSOP(PLASTIC)



NOTE>Dimension "e" does not include mold protrusion.

PACKAGE STRUCTURE

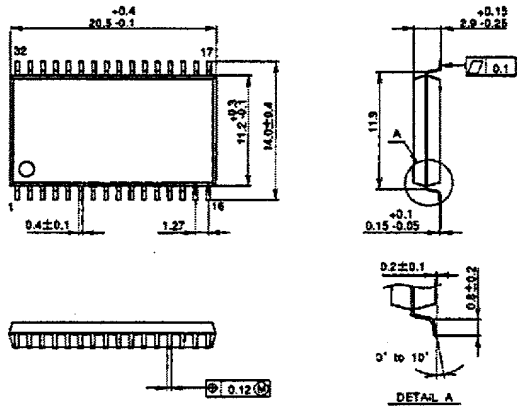
SONY CODE	TSOP-32P-L01R
EIAJ CODE	TSOP032-P-0820-B
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g

Package Outline Unit : mm

CXK581000AM

32PIN SOP(PLASTIC) 525MIL



PACKAGE STRUCTURE

SONY CODE	SOP-32P-L02
EIAJ CODE	*SOP032-P-0525-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.2g