

131,072-word × 8-bit High-Speed CMOS Static RAM

Description

The CXK581000ATM/AYM/AM/AP are high speed CMOS static RAMs organized as 131,072-words-by-8-bits.

A polysilicon TFT cell technology realizes extremely low stand-by current and higher data retention stability.

Special features are low power consumption, high speed and a broad package line-up.

The CXK581000ATM/AYM/AM/AP are suitable RAMs for portable equipment with battery backup.

Features

- Extended operating temperature range: (−25°C to +85°C)
- Fast access time: −70LLX 70ns (max.)
−10LLX 100ns (max.)
- Low standby current: 40μA (max.)
- Low data retention current: 24μA (max.)
- Single +5V supply: +5V ± 10%
- Low voltage data retention: 2.0V (min.)
- Broad package line-up

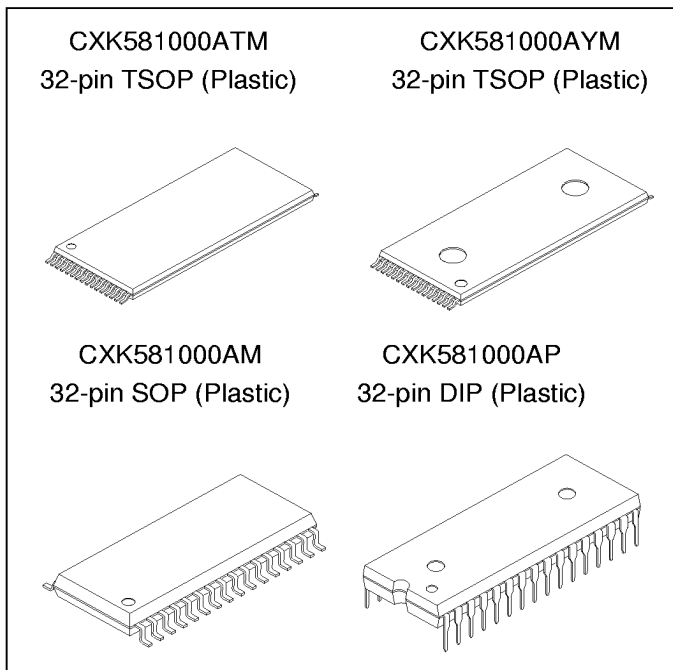
ATM/AYM	8mm × 20mm 32 pin TSOP pkg.
AM	525mil 32 pin SOP package
AP	600mil 32 pin DIP package

Functions

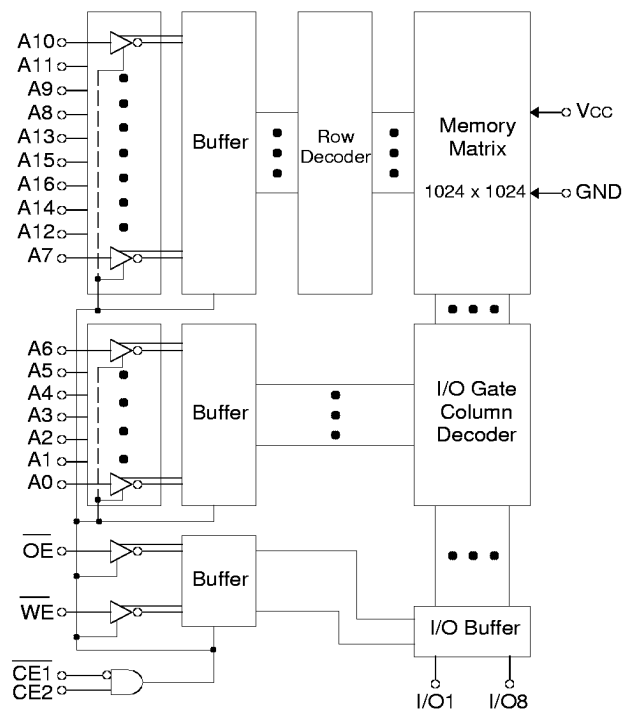
131072 word × 8 bit static RAM

Structure

Silicon gate CMOS IC

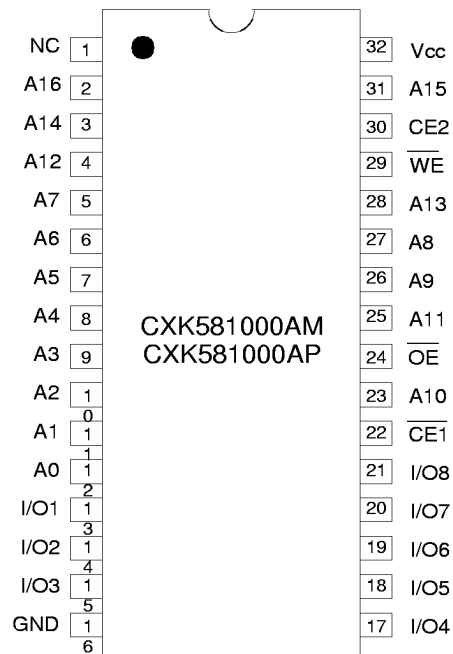
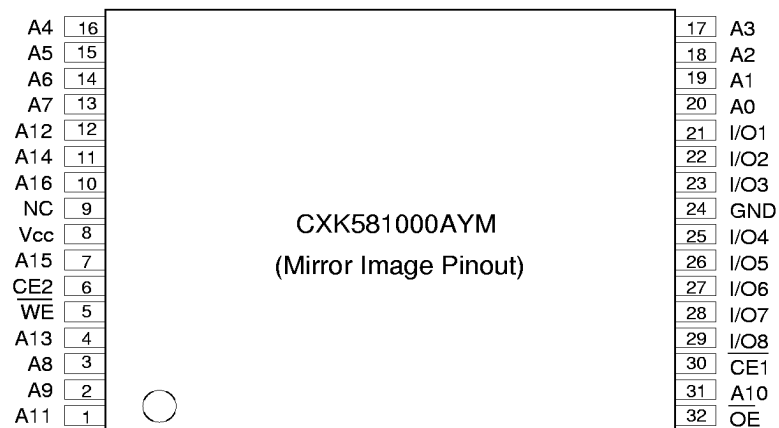
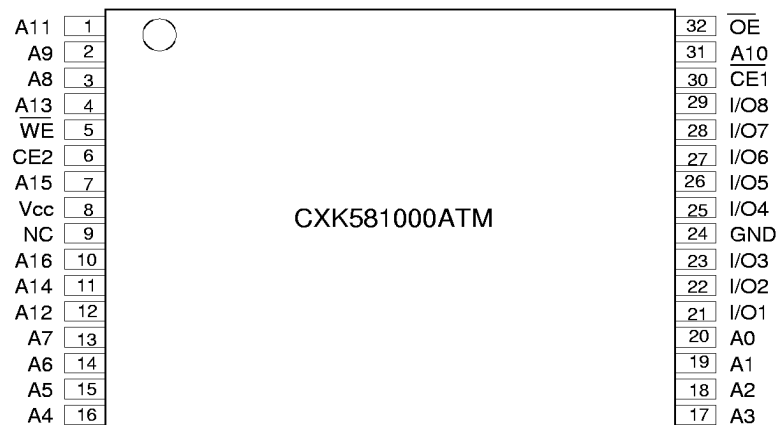


Block Diagram



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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = +25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V _{CC}		−0.5 to +7.0	V
Input voltage	V _{IN}		−0.5* to V _{CC} +0.5	
Input and output voltage	V _{I/O}		−0.5* to V _{CC} +0.5	
Allowable power dissipation	P _D	CXK581000AP	1.0	W
		CXK581000ATM/AYM/AM	0.7	
Operating temperature	T _{opr}		−25 to +85	°C
Storage temperature	T _{stg}		−55 to +150	
Soldering temperature	T _{solder}	CXK581000AP	260 • 10	°C • s
		CXK581000ATM/AYM/AM	235 • 10	

*V_{IN} V_{I/O} = −3.0V min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O Pin	V _{CC} Current
H	×	×	×	Not selected	High Z	ISB1, ISB2
×	L	×	×	Not selected	High Z	ISB1, ISB2
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	×	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

x: "H" or "L"

DC Recommended Operating Conditions

(Ta = −25 to +85°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.4	—	V _{CC} +0.3	
Input low voltage	V _{IL}	−0.3*	—	0.6	

*V_{IL} = −3.0V min. for pulse width less than 50ns.

Electrical Characteristics

• DC Characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = -25 to +85°C)

Item	Symbol	Test Conditions		Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}		-1	—	1	μA
Output leakage current	I _{LO}	$\overline{\text{CE}}1 = V_{IH}$ or $\text{CE}2 = V_{IL}$ or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$ V _{I/O} = GND to V _{CC}		-1	—	1	
Operating power supply current	I _{CC1}	$\overline{\text{CE}}1 = V_{IL}$, $\text{CE}2 = V_{IH}$ V _{IN} = V _{IH} or V _{IL} I _{OUT} = 0mA		—	7	15	mA
Average operating current	I _{CC2}	Min. cycle duty = 100% I _{OUT} = 0mA	70LLX	—	40	80	
			10LLX	—	35	60	
	I _{CC3}	Cycle time 1μs duty = 100% I _{OUT} = 0mA $\overline{\text{CE}}1 \leq 0.2V$ $\text{CE}2 \geq V_{CC}-0.2V$ $V_{IL} \leq 0.2V$ $V_{IH} \geq V_{CC}-0.2V$		—	10	20	
Standby current	I _{SB1}	$\text{CE}2 \leq 0.2V$ or $\overline{\text{CE}}1 \geq V_{CC}-0.2V$ $\text{CE}2 \geq V_{CC}-0.2V$	-25 to +85°C	—	—	40	μA
			-25 to +70°C	—	—	20	
			-25 to +40°C	—	—	4	
			+25°C	—	0.7	2	
	I _{SB2}	$\overline{\text{CE}}1 = V_{IH}$ or $\text{CE}2 = V_{IL}$		—	0.6	3	mA
Output high voltage	V _{OH}	I _{OH} = -1.0mA		2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA		—	—	0.4	

* V_{CC} = 5V, T_a = +25°C**I/O Capacitance**(T_a = +25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	

(Note) This parameter is sampled and is not 100% tested.

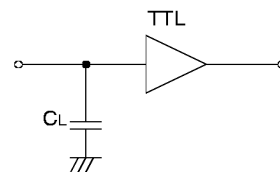
AC Characteristics

- AC Test Conditions (V_{CC} = 5V ± 10%, T_a = -25 to +85°C)

Item	Conditions
Input pulse high level	V _{IH} = 2.4V
Input pulse low level	V _{IL} = 0.6V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	C _L * = 100pF, 1TTL

* C_L includes scope and jig capacitances.

- Test Circuit



• Read Cycle ($\overline{WE} = "H"$)

Item	Symbol	-70LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	100	—	ns
Address access time	t _{AA}	—	70	—	100	
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	70	—	100	
Chip enable access time (CE2)	t _{CO2}	—	70	—	100	
Output enable to output valid	t _{OE}	—	40	—	50	
Output hold from address change	t _{OH}	10	—	10	—	
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ}	5	—	5	—	
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	—	25	—	35	
Output disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	—	25	—	35	

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

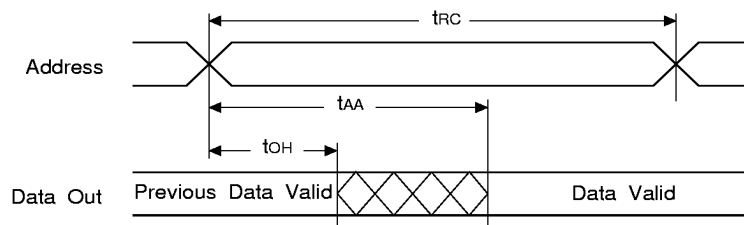
• Write Cycle

Item	Symbol	-70LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	100	—	ns
Address valid to end of write	t _{AW}	60	—	70	—	
Chip enable to end of write	t _{CW}	60	—	70	—	
Data to write time overlap	t _{DW}	30	—	40	—	
Data hold from write time	t _{DH}	0	—	0	—	
Write pulse width	t _{WP}	50	—	70	—	
Address setup time	t _{AS}	0	—	0	—	
Write recovery time ($\overline{WE}$)	t _{WR}	5	—	5	—	
Write recovery time ($\overline{CE1}$, CE2)	t _{WR1}	0	—	0	—	
Output active from end of write	t _{OW}	10	—	10	—	
Write to output in high Z	t _{WHZ} *	—	25	—	30	

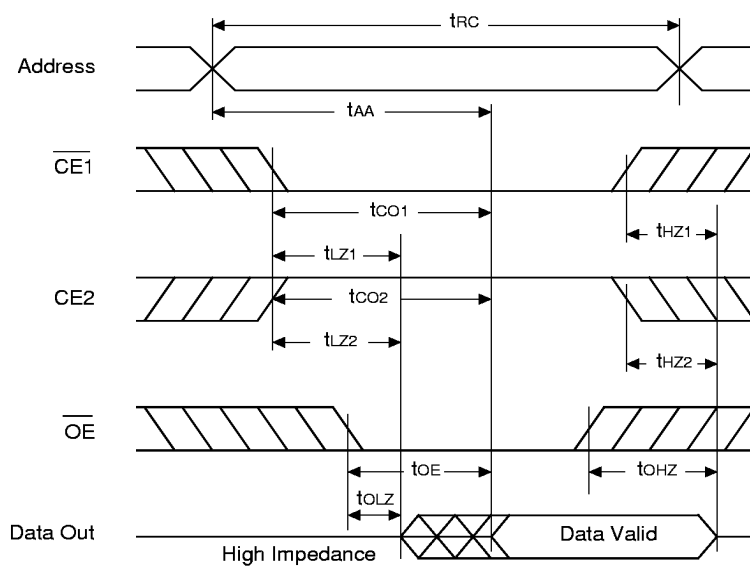
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

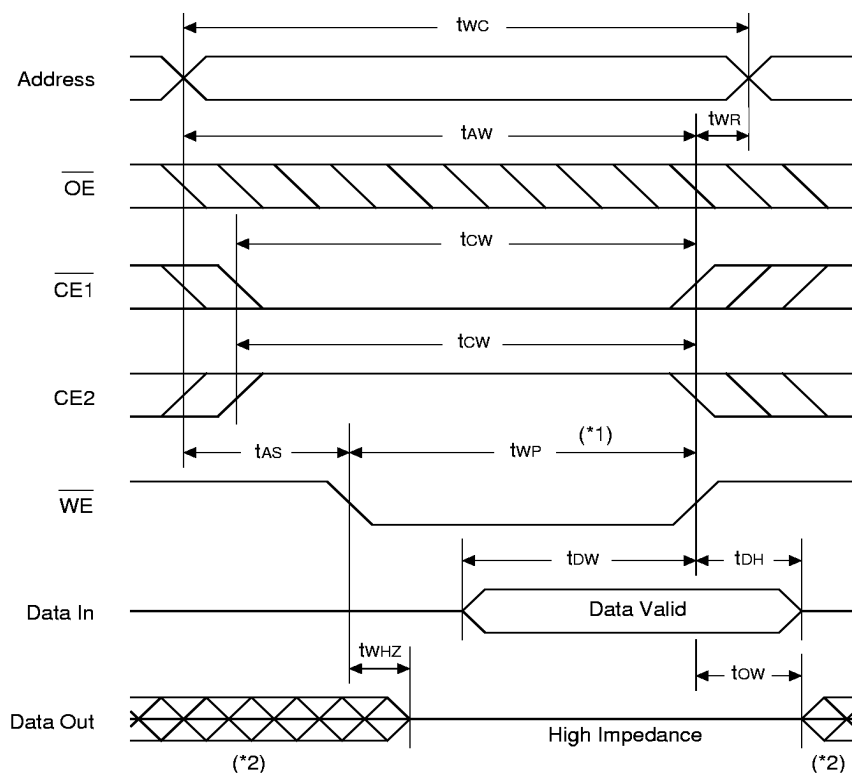
- Read Cycle (1): $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



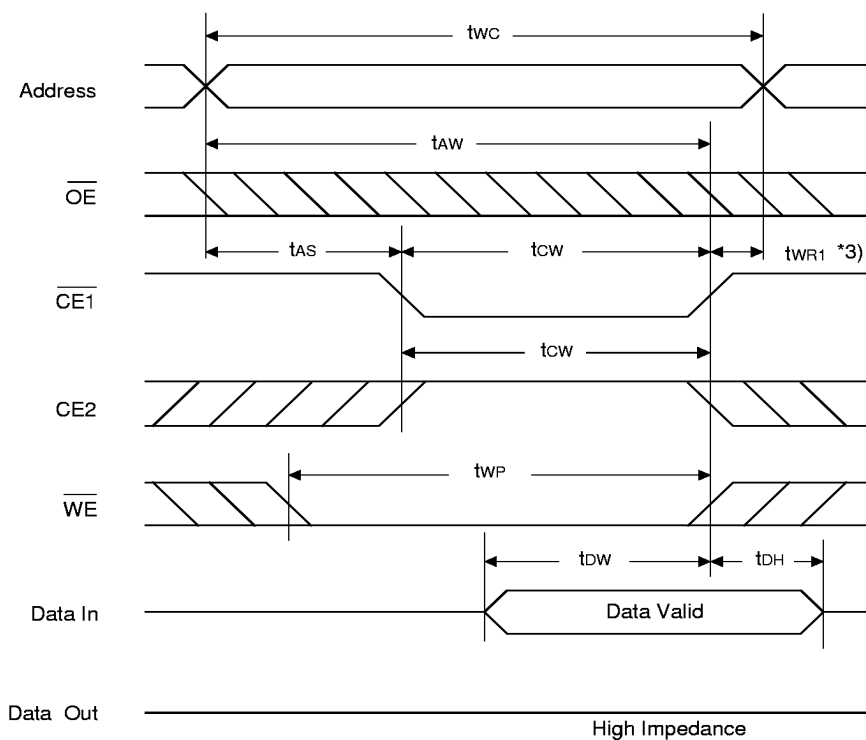
- Read Cycle (2): $\overline{WE} = V_{IH}$



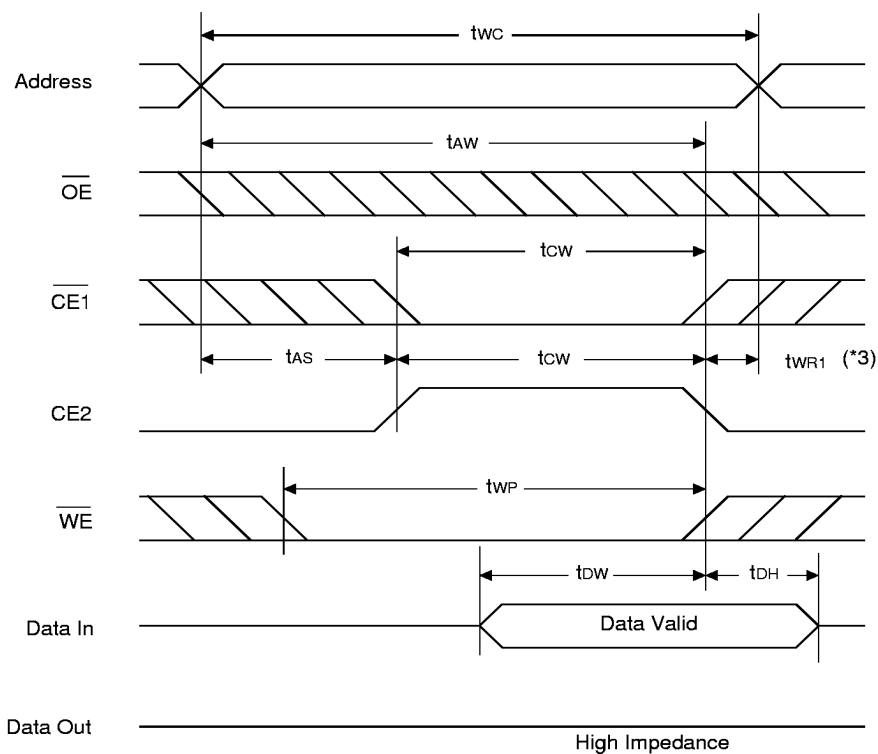
• Write Cycle (1): $\overline{\text{WE}}$ Control



• Write Cycle (2): $\overline{\text{CE1}}$ Control



• Write Cycle (3): CE2 Control



Notes)

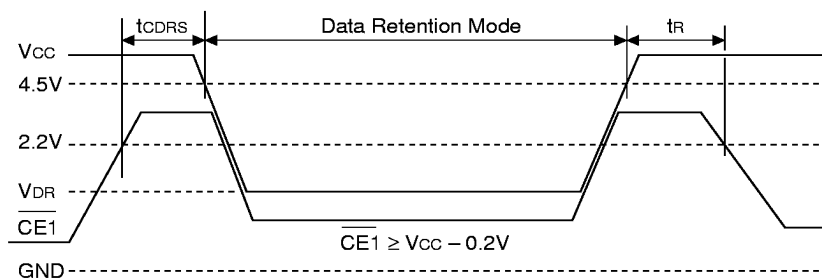
*1 Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

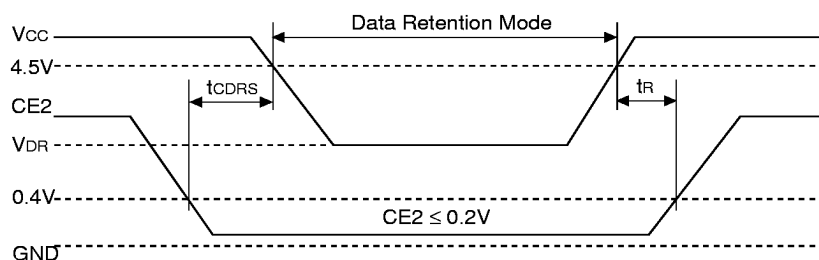
*3 t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Waveform

- Low supply voltage data retention waveform (1) ($\overline{\text{CE1}}$ Control)



- Low supply voltage data retention waveform (2) (CE2 Control)



Data Retention Characteristics

($T_a = -25$ to $+85^\circ\text{C}$)

Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	*1		2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V^{*1}$	-25 to $+85^\circ\text{C}$	—	—	24	μA
			-25 to $+70^\circ\text{C}$	—	—	12	
			-25 to $+40^\circ\text{C}$	—	—	2.4	
			$+25^\circ\text{C}$	—	0.4	1.2	
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V^{*1}$		—	0.7^{*2}	40	
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t_R			5	—	—	ms

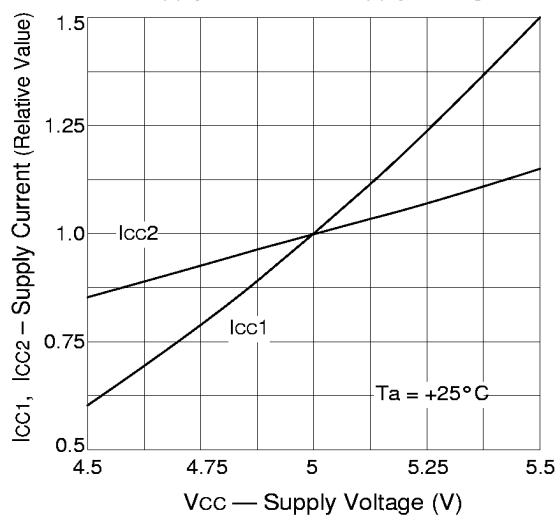
Notes)

*1 $\overline{\text{CE1}} \geq V_{CC} - 0.2V$, $\text{CE2} \geq V_{CC} - 0.2V$ [$\overline{\text{CE1}}$ control] or $\text{CE2} \leq 0.2V$ [CE2 control]

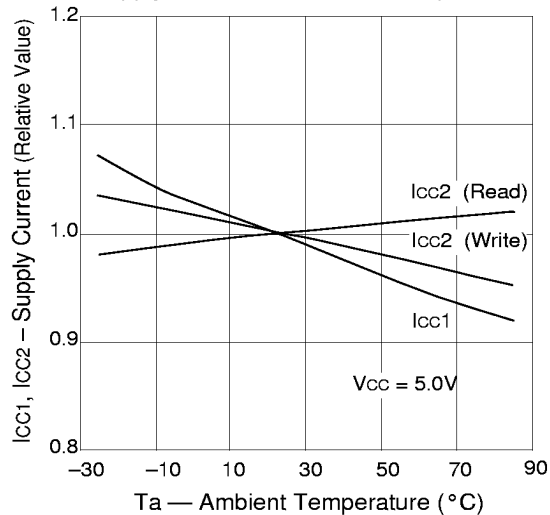
*2 $V_{CC} = 5V$, $T_a = +25^\circ\text{C}$

Example of Representative Characteristics

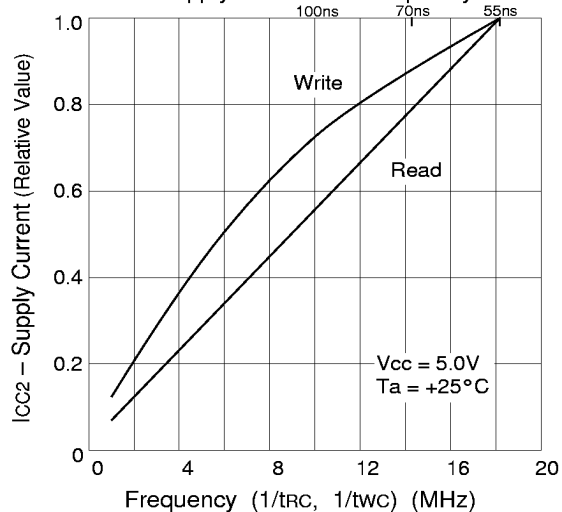
Supply Current vs. Supply Voltage



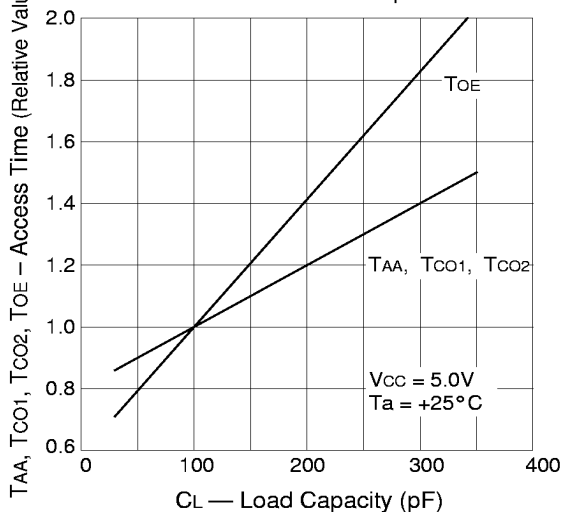
Supply Current vs. Ambient Temperature



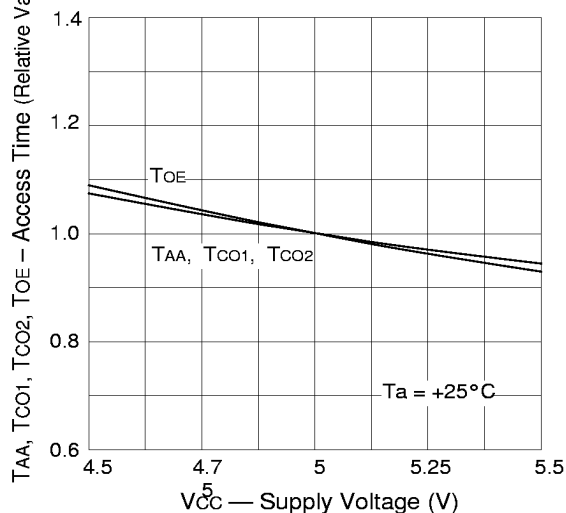
Supply Current vs. Frequency



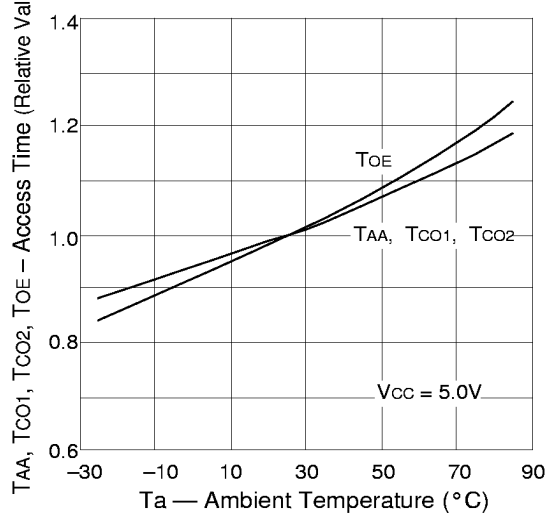
Access Time vs. Load Capacitance

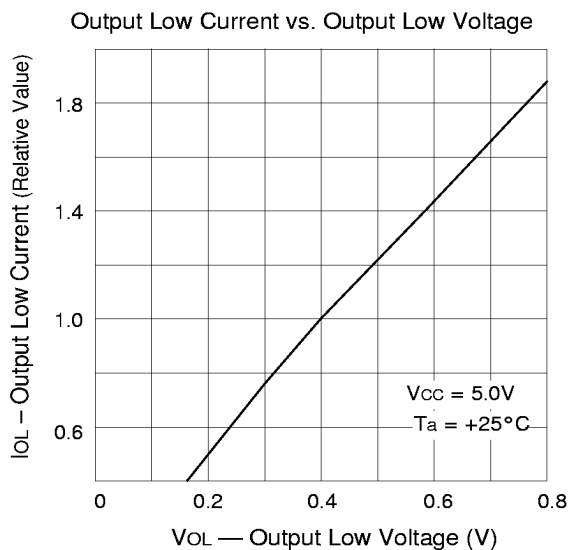
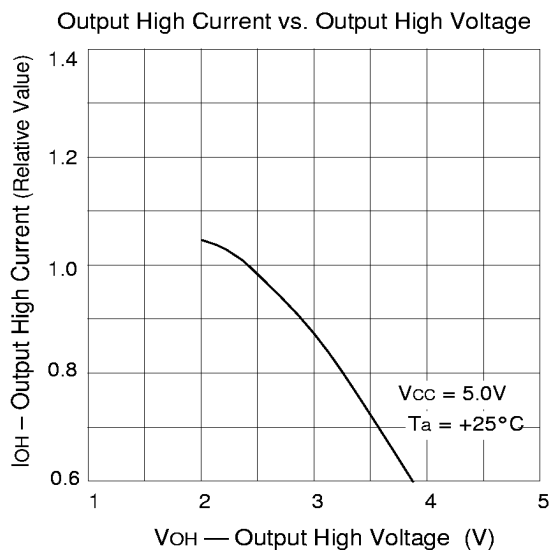
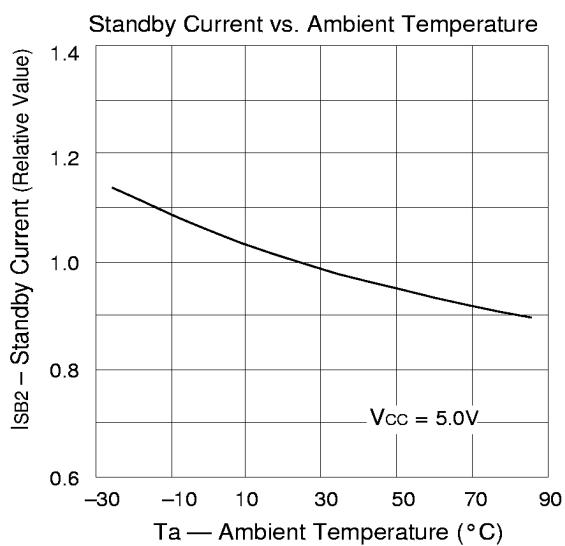
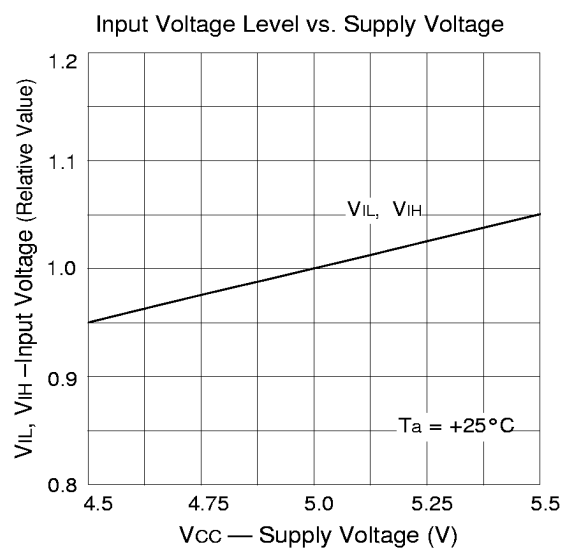
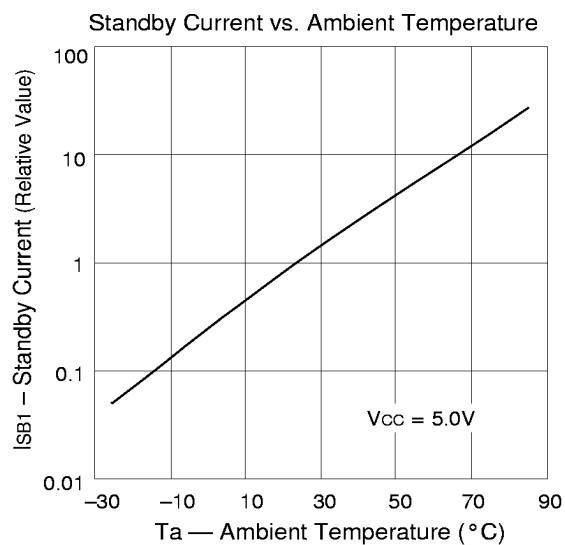
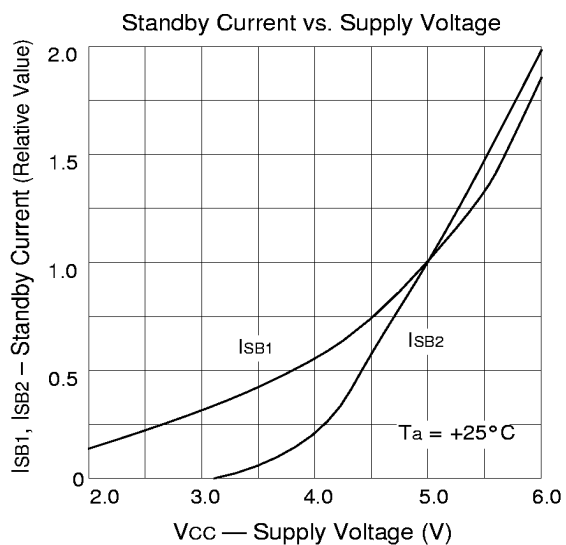


Access Time vs. Supply Voltage



Access Time vs. Ambient Temperature

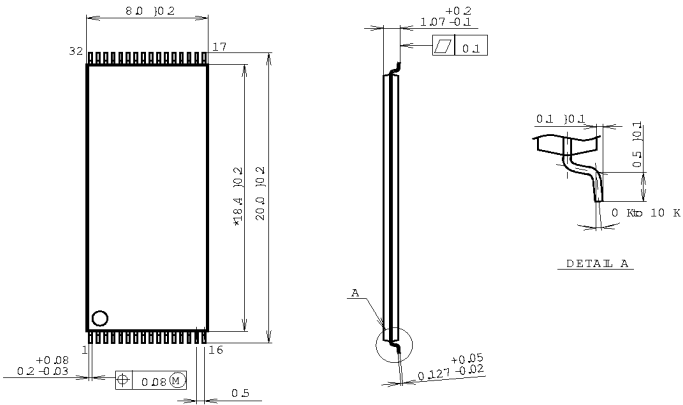




Package Outline Unit : mm

CXK581000ATM

32PIN TSOP (PLASTIC)



NOTE : *NOT INCLUDE MOLD FNS.

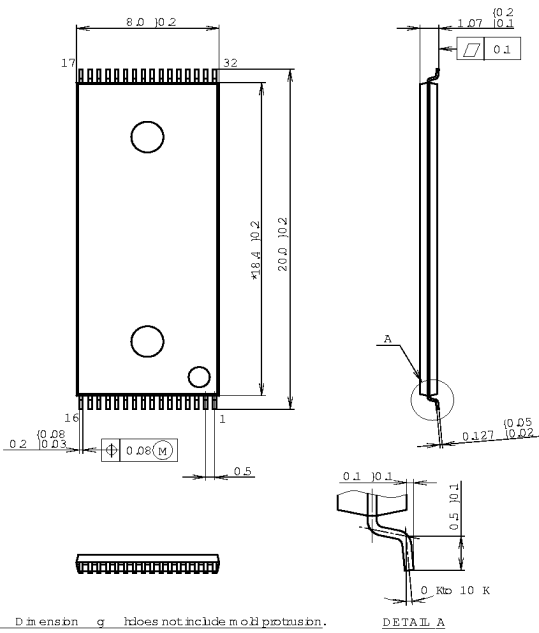
PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01
EAJ CODE	TSOP032-P-0820-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g

CXK581000AYM

32PIN TSOP (PLASTIC)



NOTE : Dimension g does not include mold protrusion.

DETAIL A

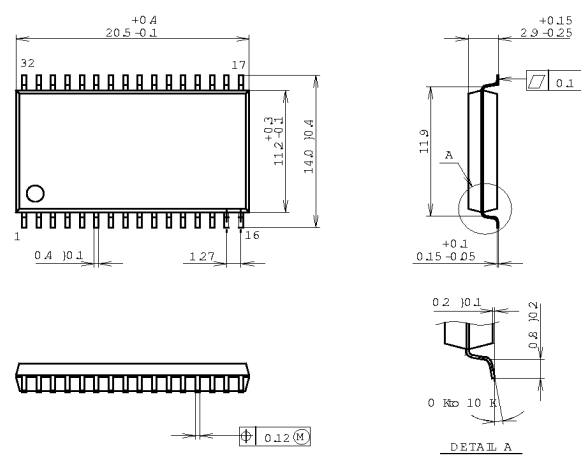
PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01R
EAJ CODE	TSOP032-P-0820-B
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g

Package Outline Unit : mm
CXK581000AM

32PIN SOP (PLASTIC) 525MIL

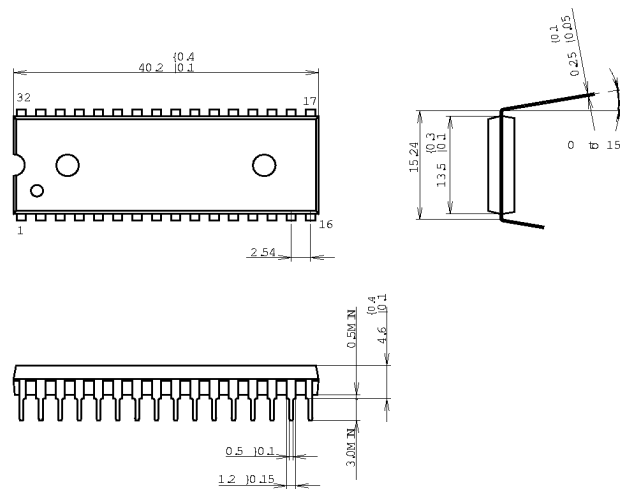


PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.2

SONY CODE	SOP-32P-L02
EAJ CODE	*SOP032P-0525-A
JEDEC CODE	

CXK581000AP

32PIN DIP (PLASTIC) 600MIL



PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	4.5g

SONY CODE	DIP-32P-01
EAJ CODE	*DIP32P-0600-A
JEDEC CODE	