

# SONY

## CXK581000BTM/BYM/BM/BP -55LL/70LL/10LL

### 131072-word × 8-bit High Speed CMOS Static RAM

#### Description

The CXK581000BTM/BYM/BM/BP is a high speed CMOS static RAM organized as 131072 words by 8 bits.

Special feature are low power consumption, high speed and broad package line-up.

The CXK581000BTM/BYM/BM/BP is a suitable RAM for portable equipment with battery back up.

#### Features

- Fast access time:

| CXK581000BTM/BYM/BM/BP | (Access time) |
|------------------------|---------------|
| -55LL                  | 55ns (Max.)   |
| -70LL                  | 70ns (Max.)   |
| -10LL                  | 100ns (Max.)  |

- Low standby current: 20 $\mu$ A (Max.)
- Low data retention current: 12 $\mu$ A (Max.)
- Single +5V supply: 5V  $\pm$  10%
- Low power data retention: 2.0V (Min.)
- Broad package line-up

#### CXK581000BTM/BYM

8mm  $\times$  20mm 32 pin TSOP package

CXK581000BM 525mil 32 pin SOP package

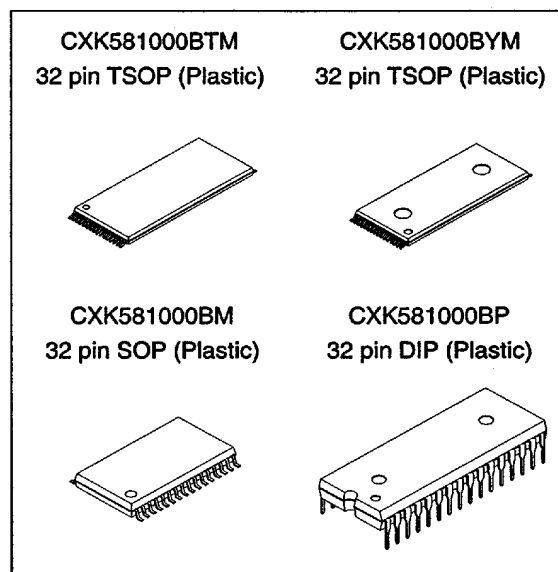
CXK581000BP 600mil 32 pin DIP package

#### Function

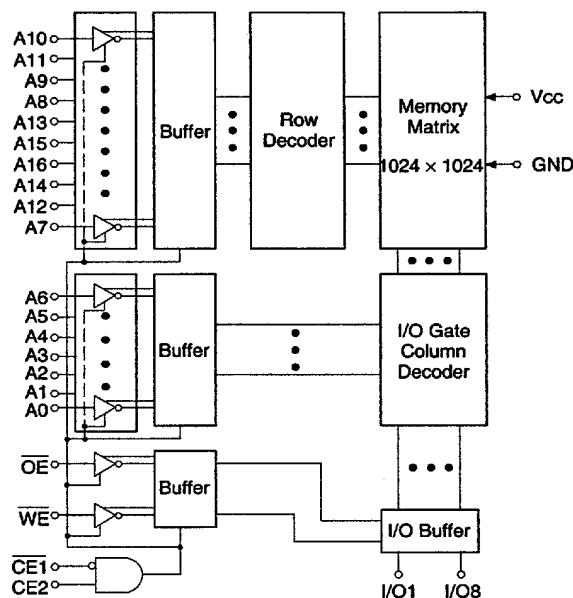
131072-word  $\times$  8-bit static RAM

#### Structure

Silicon gate CMOS IC

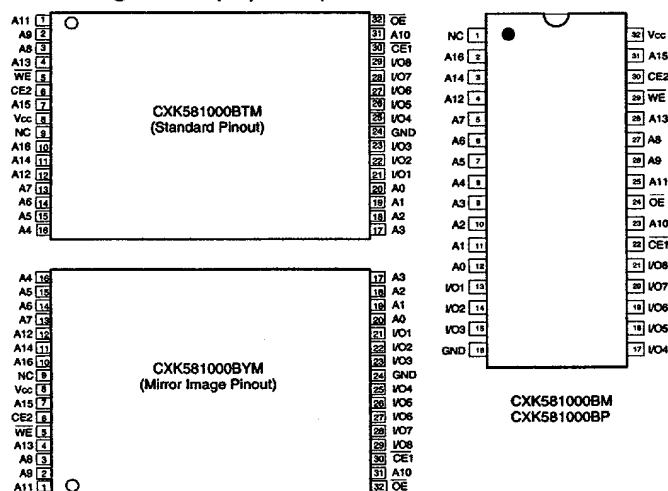


#### Block Diagram



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## Pin Configuration (Top View)



## Pin Description

| Symbol                 | Description            |
|------------------------|------------------------|
| A0 to A16              | Address input          |
| I/O1 to I/O8           | Data input output      |
| $\overline{CE1}$ , CE2 | Chip enable 1, 2 input |
| WE                     | Write enable input     |
| $\overline{OE}$        | Output enable input    |
| Vcc                    | Power supply           |
| GND                    | Ground                 |
| NC                     | No connection          |

## Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

| Item                        | Symbol              |                     | Rating                          | Unit   |
|-----------------------------|---------------------|---------------------|---------------------------------|--------|
| Supply voltage              | V <sub>CC</sub>     |                     | −0.5 to +7.0                    | V      |
| Input voltage               | V <sub>IN</sub>     |                     | −0.5*1 to V <sub>CC</sub> + 0.5 |        |
| Input and output voltage    | V <sub>I/O</sub>    |                     | −0.5*1 to V <sub>CC</sub> + 0.5 |        |
| Allowable power dissipation | P <sub>D</sub>      | CXK581000BP         | 1.0                             | W      |
|                             |                     | CXK581000BTM/BYM/BM | 0.7                             |        |
| Operating temperature       | T <sub>opr</sub>    |                     | 0 to +70                        | °C     |
| Storage temperature         | T <sub>stg</sub>    |                     | −55 to +150                     |        |
| Soldering temperature       | T <sub>solder</sub> | CXK581000BP         | 260 · 10                        | °C · s |
|                             |                     | CXK581000BTM/BYM/BM | 235 · 10                        |        |

\*1 V<sub>IN</sub>, V<sub>IO</sub> = -3.0V Min. for pulse width less than 50ns.

## Truth Table

| $\overline{CE1}$ | CE2 | $\overline{OE}$ | WE | Mode           | I/O pin  | Vcc Current                                            |
|------------------|-----|-----------------|----|----------------|----------|--------------------------------------------------------|
| H                | x   | x               | x  | Not selected   | High Z   | I <sub>SB1</sub> , I <sub>SB2</sub>                    |
| x                | L   | x               | x  | Not selected   | High Z   | I <sub>SB1</sub> , I <sub>SB2</sub>                    |
| L                | H   | H               | H  | Output disable | High Z   | I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub> |
| L                | H   | L               | H  | Read           | Data out | I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub> |
| L                | H   | x               | L  | Write          | Data in  | I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub> |

x: "H" or "L"

**DC Recommended Operating Conditions** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $\text{GND} = 0\text{V}$ )

| Item               | Symbol   | Min.        | Typ. | Max.           | Unit |
|--------------------|----------|-------------|------|----------------|------|
| Supply voltage     | $V_{CC}$ | 4.5         | 5.0  | 5.5            | V    |
| Input high voltage | $V_{IH}$ | 2.2         | —    | $V_{CC} + 0.3$ |      |
| Input low voltage  | $V_{IL}$ | $-0.3^{*1}$ | —    | 0.8            |      |

\*1  $V_{IL} = -3.0\text{V}$  Min. for pulse width less than 50ns.

**Electrical Characteristics****• DC Characteristics**

( $V_{CC} = 5\text{V} \pm 10\%$ ,  $\text{GND} = 0\text{V}$ ,  $T_a = 0$  to  $+70^\circ\text{C}$ )

| Item                           | Symbol           | Test conditions                                                                                                                                                                                                                   |            | Min. | Typ.*2 | Max. | Unit |
|--------------------------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------|--------|------|------|
| Input leakage current          | I <sub>LI</sub>  | V <sub>IN</sub> = GND to V <sub>CC</sub>                                                                                                                                                                                          |            | -1   | —      | 1    | μA   |
| Output leakage current         | I <sub>LO</sub>  | $\overline{\text{CE1}} = \text{V}_{\text{IH}}$ or $\text{CE2} = \text{V}_{\text{IL}}$ or<br>$\text{OE} = \text{V}_{\text{IH}}$ or $\overline{\text{WE}} = \text{V}_{\text{IL}}$<br>V <sub>I/O</sub> = GND to V <sub>CC</sub>      |            | -1   | —      | 1    |      |
| Operating power supply current | I <sub>CC1</sub> | $\overline{\text{CE1}} = \text{V}_{\text{IL}}$ , $\text{CE2} = \text{V}_{\text{IH}}$<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>I <sub>OUT</sub> = 0mA                                                            |            | —    | 7      | 15   | mA   |
| Average operating current      | I <sub>CC2</sub> | Min. cycle<br>duty = 100%<br>I <sub>OUT</sub> = 0mA                                                                                                                                                                               | -55LL      | —    | 45     | 90   |      |
|                                |                  |                                                                                                                                                                                                                                   | -70LL      | —    | 40     | 70   |      |
|                                |                  |                                                                                                                                                                                                                                   | -10LL      | —    | 35     | 60   |      |
|                                | I <sub>CC3</sub> | Cycle time 1μs<br>duty = 100%<br>I <sub>OUT</sub> = 0mA<br>$\overline{\text{CE1}} \leq 0.2\text{V}$<br>$\text{CE2} \geq \text{V}_{\text{CC}} - 0.2\text{V}$<br>V <sub>IL</sub> ≤ 0.2V<br>V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2V |            | —    | 10     | 20   |      |
| Standby current                | I <sub>SB1</sub> | $\text{CE2} \leq 0.2\text{V}$<br>or { $\overline{\text{CE1}} \geq \text{V}_{\text{CC}} - 0.2\text{V}$<br>$\text{CE2} \geq \text{V}_{\text{CC}} - 0.2\text{V}$                                                                     | 0 to +70°C | —    | —      | 20   | μA   |
|                                |                  |                                                                                                                                                                                                                                   | 0 to +40°C | —    | —      | 4    |      |
|                                |                  |                                                                                                                                                                                                                                   | +25°C      | —    | 0.7    | 2    |      |
|                                | I <sub>SB2</sub> | $\overline{\text{CE1}} = \text{V}_{\text{IH}}$ or $\text{CE2} = \text{V}_{\text{IL}}$                                                                                                                                             |            | —    | 0.6    | 3    | mA   |
| Output high voltage            | V <sub>OH</sub>  | I <sub>OH</sub> = -1.0mA                                                                                                                                                                                                          |            | 2.4  | —      | —    | V    |
| Output low voltage             | V <sub>OL</sub>  | I <sub>OL</sub> = 2.1mA                                                                                                                                                                                                           |            | —    | —      | 0.4  |      |

\*2  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$

## I/O Capacitance

(Ta = 25°C, f = 1MHz)

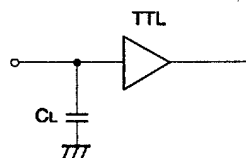
| Item              | Symbol           | Test conditions       | Min. | Typ. | Max. | Unit |
|-------------------|------------------|-----------------------|------|------|------|------|
| Input capacitance | C <sub>IN</sub>  | V <sub>IN</sub> = 0V  | —    | —    | 7    | pF   |
| I/O capacitance   | C <sub>I/O</sub> | V <sub>I/O</sub> = 0V | —    | —    | 8    |      |

Note) This parameter is sampled and is not 100% tested.

## AC Characteristics

• AC test conditions (V<sub>CC</sub> = 5V ± 10%, Ta = 0 to +70°C)

| Item                             |       | Conditions                      |
|----------------------------------|-------|---------------------------------|
| Input pulse high level           |       | V <sub>IH</sub> = 2.2V          |
| Input pulse low level            |       | V <sub>IL</sub> = 0.8V          |
| Input rise time                  |       | t <sub>r</sub> = 5ns            |
| Input fall time                  |       | t <sub>f</sub> = 5ns            |
| Input and output reference level |       | 1.5V                            |
| Output load conditions           | -55LL | C <sub>L</sub> *1 = 30pF, 1TTL  |
|                                  | -70LL | C <sub>L</sub> *1 = 100pF, 1TTL |
|                                  | -10LL |                                 |



\*1 C<sub>L</sub> includes scope and jig capacitances.

• Read cycle ( $\overline{WE} = "H"$ )

| Item                                                          | Symbol                     | -55LL |      | -70LL |      | -10LL |      | Unit |
|---------------------------------------------------------------|----------------------------|-------|------|-------|------|-------|------|------|
|                                                               |                            | Min.  | Max. | Min.  | Max. | Min.  | Max. |      |
| Read cycle time                                               | $t_{RC}$                   | 55    | —    | 70    | —    | 100   | —    | ns   |
| Address access time                                           | $t_{AA}$                   | —     | 55   | —     | 70   | —     | 100  |      |
| Chip enable access time ( $\overline{CE1}$ )                  | $t_{CO1}$                  | —     | 55   | —     | 70   | —     | 100  |      |
| Chip enable access time ( $CE2$ )                             | $t_{CO2}$                  | —     | 55   | —     | 70   | —     | 100  |      |
| Output enable to output valid                                 | $t_{OE}$                   | —     | 30   | —     | 40   | —     | 50   |      |
| Output hold from address change                               | $t_{OH}$                   | 15    | —    | 15    | —    | 15    | —    |      |
| Chip enable to output in low Z ( $\overline{CE1}$ , $CE2$ )   | $t_{LZ1}$ , $t_{LZ2}$      | 10    | —    | 10    | —    | 10    | —    |      |
| Output enable to output in low Z ( $\overline{OE}$ )          | $t_{OLZ}$                  | 5     | —    | 5     | —    | 5     | —    |      |
| Chip disable to output in high Z ( $\overline{CE1}$ , $CE2$ ) | $t_{HZ1}$ , $t_{HZ2}^{*1}$ | —     | 25   | —     | 25   | —     | 35   |      |
| Output disable to output in high Z ( $\overline{OE}$ )        | $t_{OHZ}^{*1}$             | —     | 25   | —     | 25   | —     | 35   |      |

\*1  $t_{HZ1}$ ,  $t_{HZ2}$  and  $t_{OHZ}$  are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

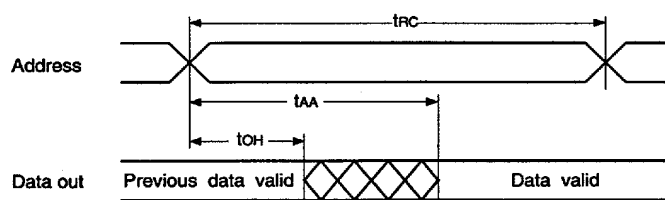
## • Write cycle

| Item                                    | Symbol         | -55LL |      | -70LL |      | -10LL |      | Unit |
|-----------------------------------------|----------------|-------|------|-------|------|-------|------|------|
|                                         |                | Min.  | Max. | Min.  | Max. | Min.  | Max. |      |
| Write cycle time                        | $t_{WC}$       | 55    | —    | 70    | —    | 100   | —    | ns   |
| Address valid to end of write           | $t_{AW}$       | 50    | —    | 60    | —    | 70    | —    |      |
| Chip enable to end of write             | $t_{CW}$       | 50    | —    | 60    | —    | 70    | —    |      |
| Data to write time overlap              | $t_{DW}$       | 25    | —    | 30    | —    | 40    | —    |      |
| Data hold from write time               | $t_{DH}$       | 0     | —    | 0     | —    | 0     | —    |      |
| Write pulse width                       | $t_{WP}$       | 40    | —    | 50    | —    | 70    | —    |      |
| Address setup time                      | $t_{AS}$       | 0     | —    | 0     | —    | 0     | —    |      |
| Write recovery time ( $\overline{WE}$ ) | $t_{WR}$       | 0     | —    | 0     | —    | 0     | —    |      |
| Write recovery time ( $CE1$ , $CE2$ )   | $t_{WR1}$      | 0     | —    | 0     | —    | 0     | —    |      |
| Output active from end of write         | $t_{OW}$       | 10    | —    | 10    | —    | 10    | —    |      |
| Write to output in high Z               | $t_{WHZ}^{*2}$ | —     | 25   | —     | 25   | —     | 30   |      |

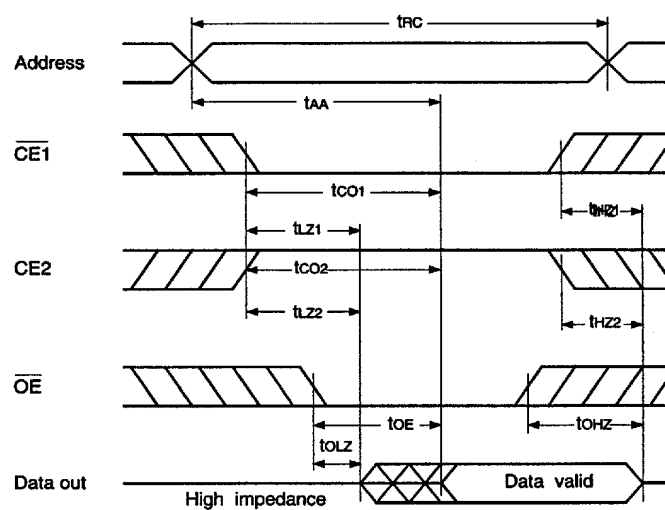
\*2  $t_{WHZ}$  is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

## Timing Waveform

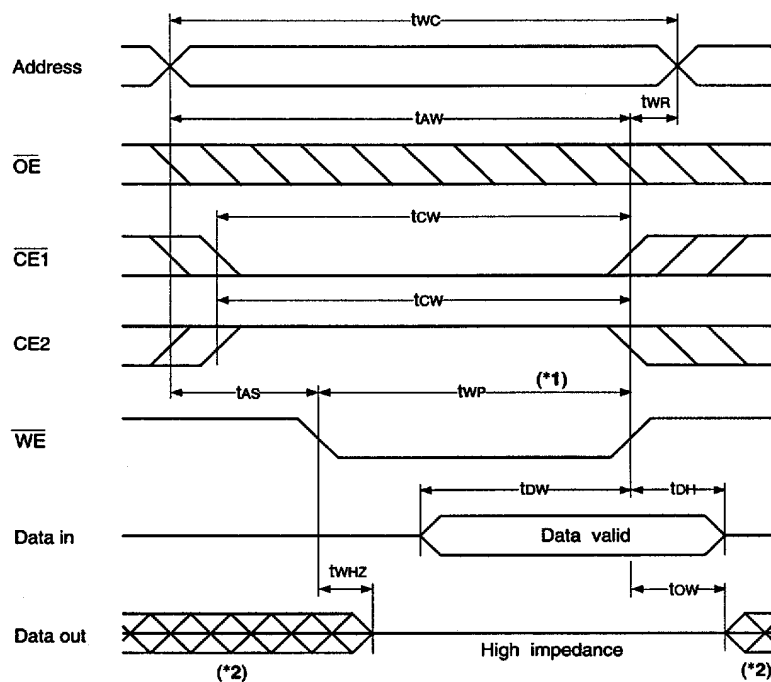
- Read cycle (1) :  $\overline{CE1} = \overline{OE} = V_{IL}$ ,  $CE2 = V_{IH}$ ,  $\overline{WE} = V_{IH}$



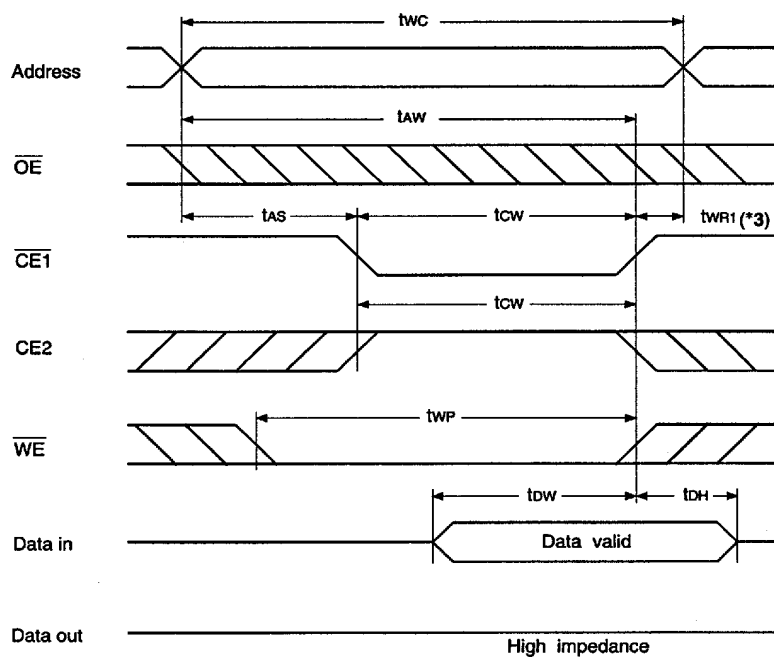
- Read cycle (2) :  $\overline{WE} = V_{IH}$



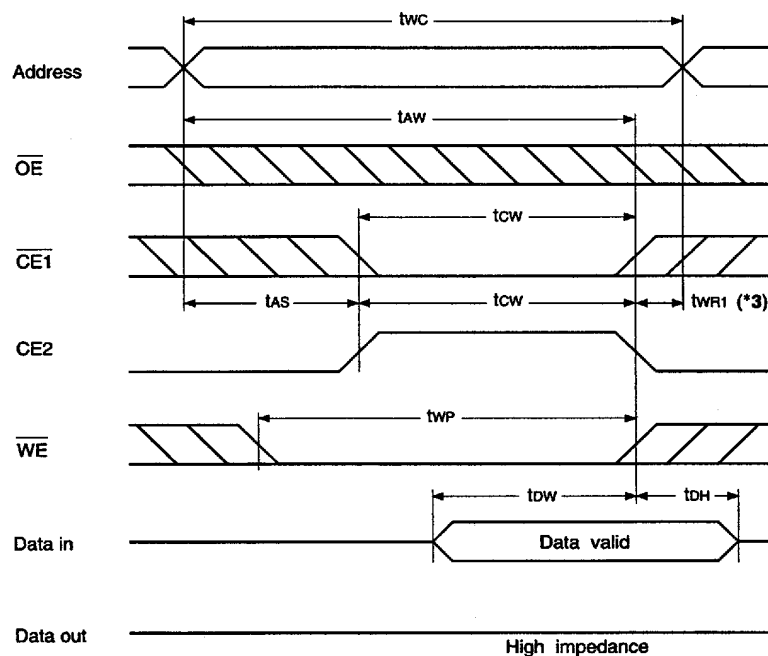
• Write cycle (1) :  $\overline{WE}$  control



• Write cycle (2) :  $\overline{CE1}$  control



• Write cycle (3) : CE2 control

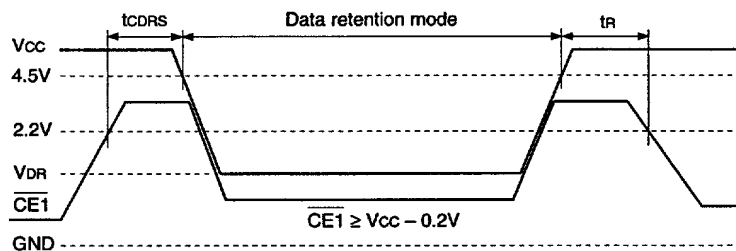


\*1 Write is executed when both  $\overline{CE1}$  and  $\overline{WE}$  are at low and CE2 is at high simultaneously.

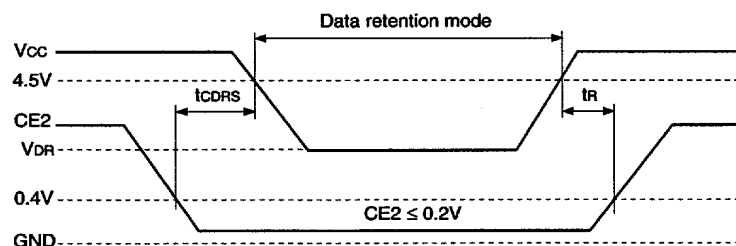
\*2 Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

\*3  $t_{WR1}$  is tested from either the rising edge of  $\overline{CE1}$  or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

## Data Retention Waveform

• Low supply voltage data retention waveform (1) :  $\overline{CE1}$  control

## • Low supply voltage data retention waveform (2) : CE2 control



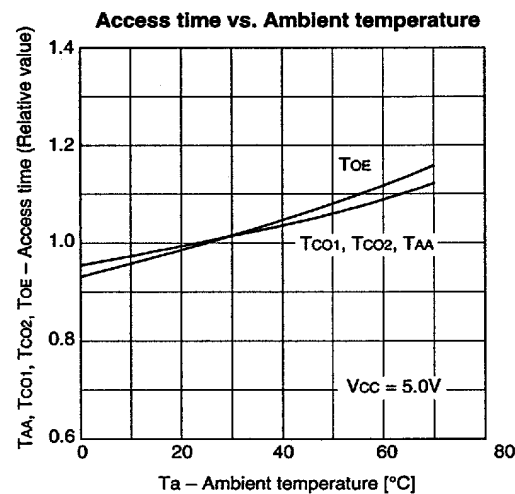
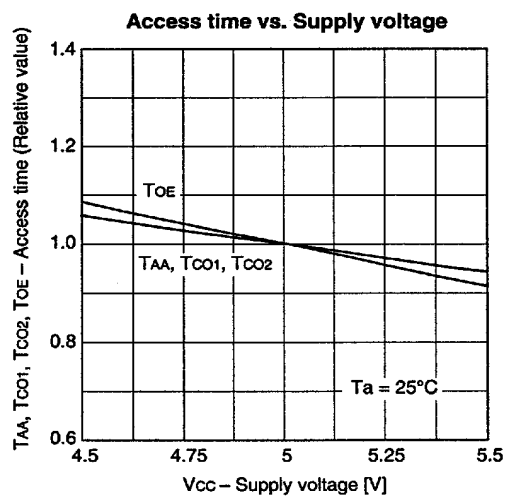
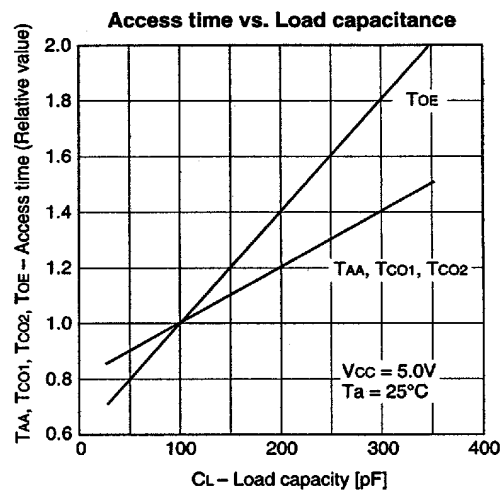
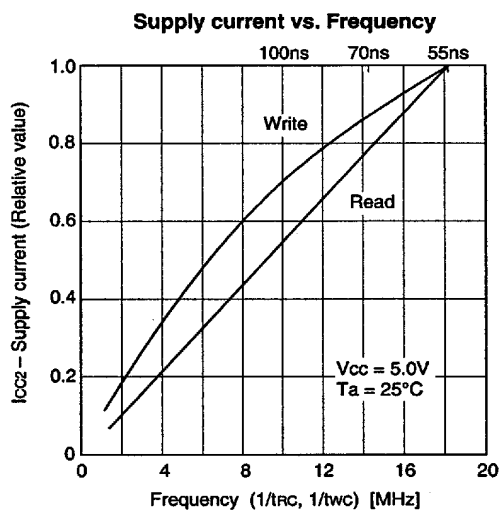
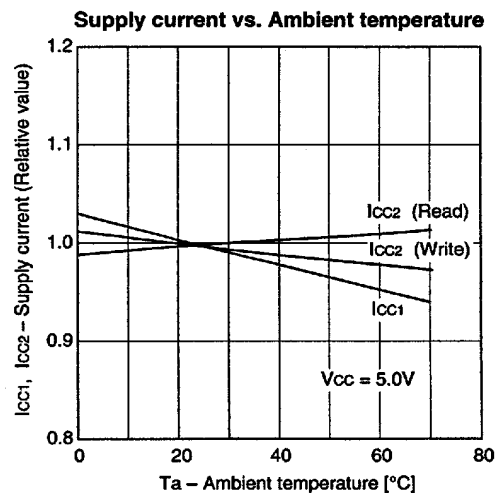
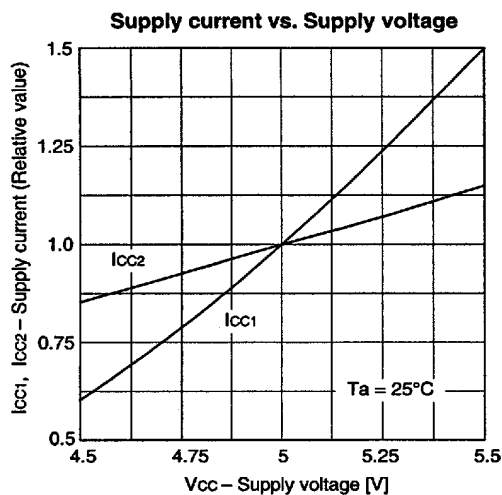
## Data Retention Characteristics

(Ta = 0 to +70°C)

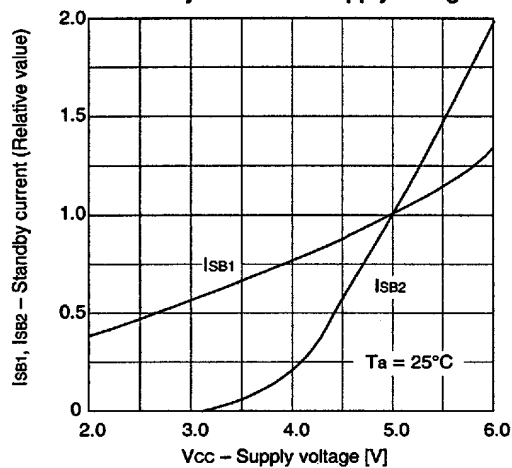
| Item                      | Symbol             | Test conditions                     |            | Min. | Typ.  | Max. | Unit |
|---------------------------|--------------------|-------------------------------------|------------|------|-------|------|------|
| Data retention voltage    | V <sub>DR</sub>    | *1                                  |            | 2.0  | —     | 5.5  | V    |
| Data retention current    | I <sub>CCDR1</sub> | V <sub>CC</sub> = 3.0V*1            | 0 to +70°C | —    | —     | 12   | μA   |
|                           |                    |                                     | 0 to +40°C | —    | —     | 2.4  |      |
|                           |                    |                                     | +25°C      | —    | 0.4   | 1.2  |      |
|                           | I <sub>CCDR2</sub> | V <sub>CC</sub> = 2.0 to 5.5V*1     |            | —    | 0.7*2 | 20   |      |
| Data retention setup time | t <sub>CDRS</sub>  | Chip disable to data retention mode |            | 0    | —     | —    | ns   |
| Recovery time             | t <sub>R</sub>     |                                     |            | 5    | —     | —    | ms   |

\*1  $\overline{CE1} \geq V_{CC} - 0.2V$ ,  $\overline{CE2} \geq V_{CC} - 0.2V$  ( $\overline{CE1}$  control) or  $\overline{CE2} \leq 0.2V$  ( $\overline{CE2}$  control)\*2 V<sub>CC</sub> = 5V, Ta = 25°C

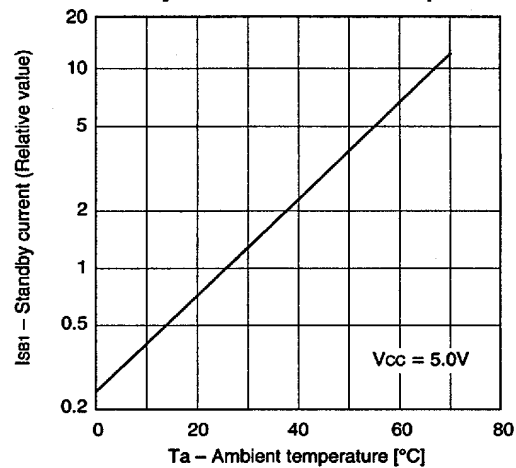
## Example of Representative Characteristics



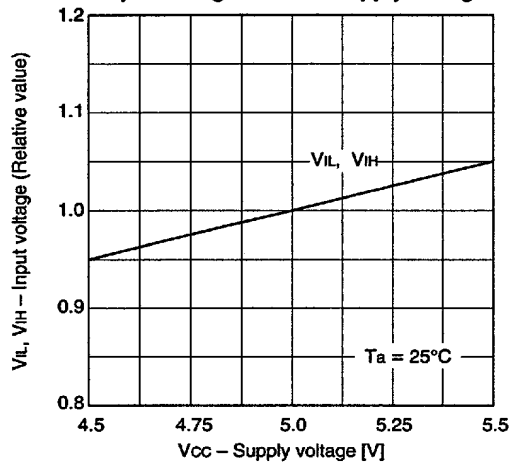
Standby current vs. Supply voltage



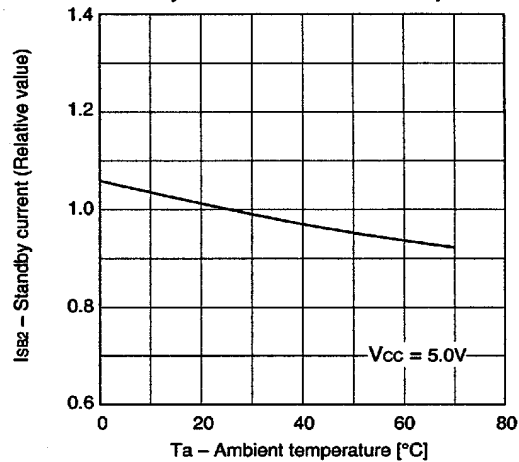
Standby current vs. Ambient temperature



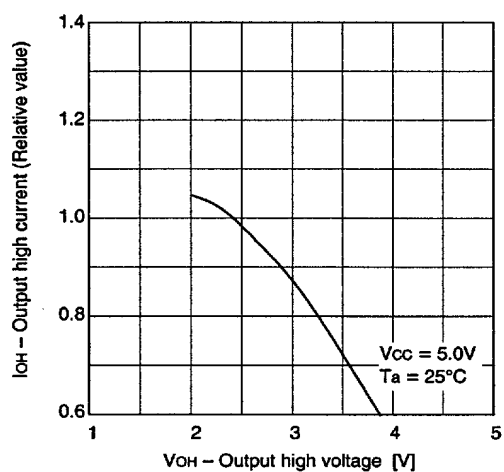
Input voltage level vs. Supply voltage



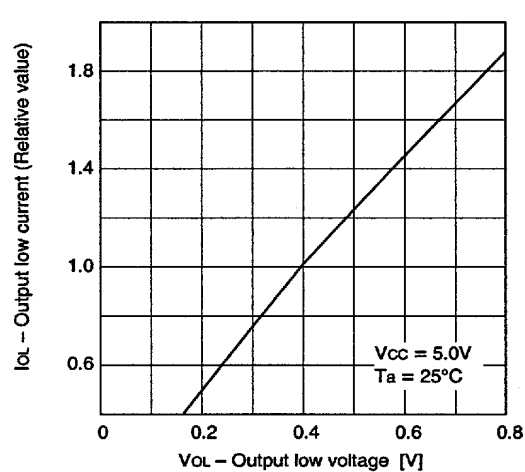
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



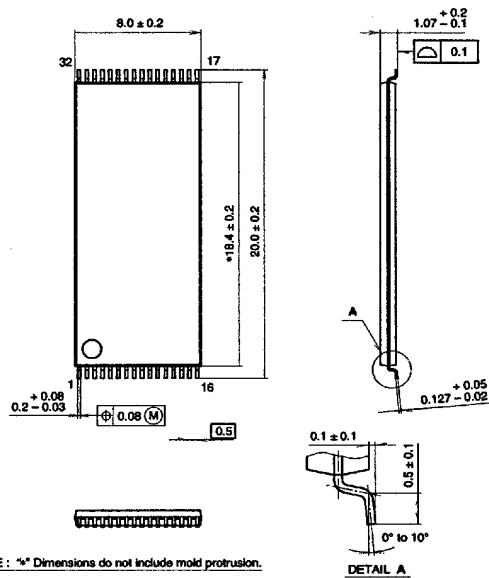
Output low current vs. Output low voltage



## Package Outline Unit: mm

## CXK581000BTM

## 32PIN TSOP (PLASTIC)



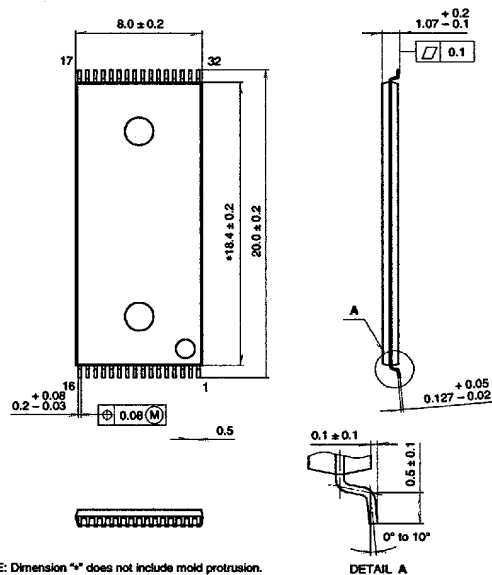
## PACKAGE STRUCTURE

|            |                |
|------------|----------------|
| SONY CODE  | TSOP-32P-L01   |
| EIAJ CODE  | TSOP032-P-0820 |
| JEDEC CODE |                |

|                  |                |
|------------------|----------------|
| PACKAGE MATERIAL | EPOXY RESIN    |
| LEAD TREATMENT   | SOLDER PLATING |
| LEAD MATERIAL    | 42 ALLOY       |
| PACKAGE WEIGHT   | 0.3g           |

## CXK581000BYM

## 32PIN TSOP (PLASTIC)



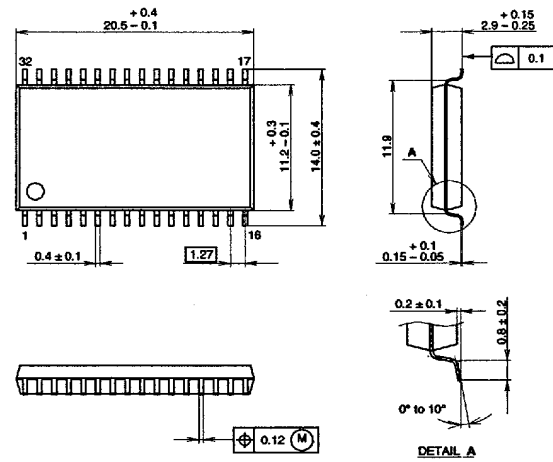
## PACKAGE STRUCTURE

|            |                  |
|------------|------------------|
| SONY CODE  | TSOP-32P-L01R    |
| EIAJ CODE  | TSOP032-P-0820-B |
| JEDEC CODE |                  |

|                  |                |
|------------------|----------------|
| PACKAGE MATERIAL | EPOXY RESIN    |
| LEAD TREATMENT   | SOLDER PLATING |
| LEAD MATERIAL    | 42 ALLOY       |
| PACKAGE WEIGHT   | 0.3g           |

CXK581000BM

32PIN SOP (PLASTIC)

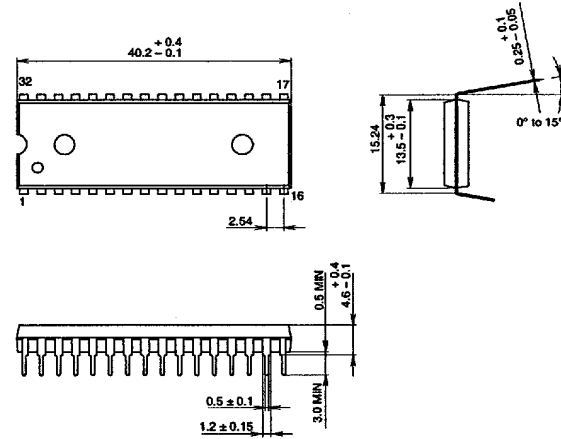


|            |               |
|------------|---------------|
| SONY CODE  | SOP-32P-L02   |
| EIAJ CODE  | SOP032-P-0525 |
| JEDEC CODE |               |

|                   |                |
|-------------------|----------------|
| PACKAGE STRUCTURE |                |
| PACKAGE MATERIAL  | EPOXY RESIN    |
| LEAD TREATMENT    | SOLDER PLATING |
| LEAD MATERIAL     | 42 ALLOY       |
| PACKAGE WEIGHT    | 1.2g           |

CXK581000BP

32PIN DIP (PLASTIC) 600mil



|            |                 |
|------------|-----------------|
| SONY CODE  | DIP-32P-01      |
| EIAJ CODE  | +DIP32-P-0600-A |
| JEDEC CODE |                 |

|                   |                      |
|-------------------|----------------------|
| PACKAGE STRUCTURE |                      |
| PACKAGE MATERIAL  | EPOXY / PHENOL RESIN |
| LEAD TREATMENT    | SOLDER PLATING       |
| LEAD MATERIAL     | 42 ALLOY             |
| PACKAGE WEIGHT    | 4.5g                 |