SONY

CXK58257BTM/BYM/BP/BM -55LL/70LL/10LL

32768-word x 8-bit High Speed CMOS Static RAM

Description

The CXK58257BTM/BYM/BP/BM is 262,144 bits high speed CMOS static RAM organized as 32768-words by 8 bits.

A polysilicon TFT cell technology realized extermely low stand-by current and higher data retention stability.

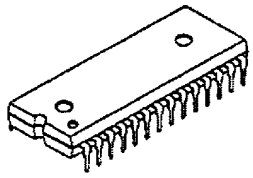
Special feature are operating on a single 5V supply, low power consumption, high speed and broad package line-up.

the CXK58257BTM/BYM/BP/BM is a suitable RAM for portable equipment with battery back up.

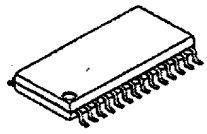
CXK58257BTM
28 pin TSOP (Plastic)

CXK58257BYM
28 pin TSOP (Plastic)

CXK58257BP
28 pin 600mil DIP (Plastic)



CXK58257BM
28 pin SOP (Plastic)



Features

- Wide supply voltage operation: 4.5V to 5.5V
- Fast access time:

CXK58257BTM/BYM/BP/BM	(Access time)
-55LL	55ns (Max.)
-70LL	70ns (Max.)
-10LL	100ns (Max.)

- Low power

CXK58257BTM/BYM/BP/BM	
-55LL/70LL/10LL	5µA (Max.)

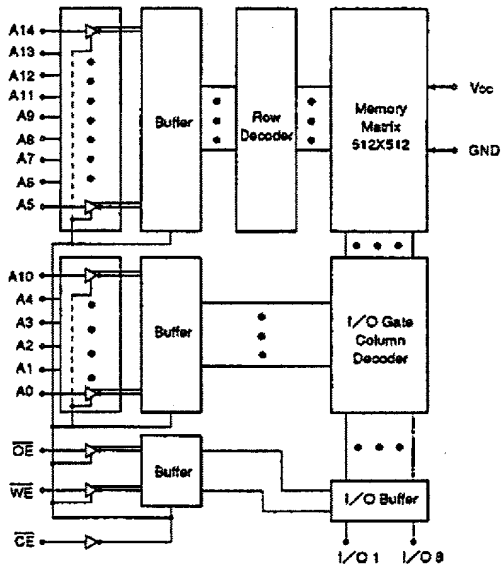
- Low power data retention current:

CXK58257BTM/BYM/BP/BM	
-55LL/70LL/10LL	3µA (Min.)

- Direct TTL compatible: All inputs and outputs
- Data retention voltage: 2.0V (Min.)
- Available in many packages

CXK58257BTM/BYM	8mm x 13.4mm 28 pin TSOP Package
CXK58257BM	450mil 28 pin SOP Package
CXK58257BP	600mil 28 pin DIP Package

Block Diagram



Function

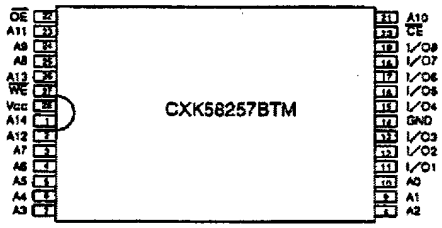
32768-word x 8 bit static RAM

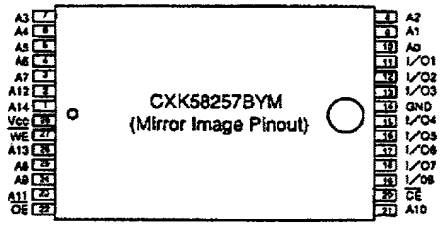
Structure

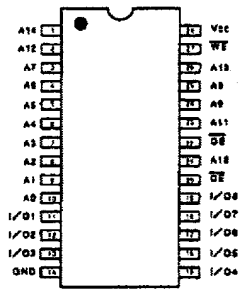
Silicon gate CMOS IC

E93919B63—ST

Pin Configuration (Top View)







CXK58257BP
CXK58257BM

Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Ityem	Symbol		Rating	Unit
Supply voltage	Vcc		−0.5 to +7.0	V
Input voltage	V_{IN}		−0.5* to Vcc + 0.5	
Input and output voltage	$V_{I/O}$		−0.5* to Vcc + 0.5	
Allowable power dissipation	P_D	CXK58257BP	1.0	W
		CXK58257BTM/BYM/BM	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		−55 to +150	
Soldering temperature · time	Tsolder	CXK58257BP	260 · 10	°C · s
		CXK58257BTM/BYM/BM	235 · 10	

* V_{IN}, $V_{I/O}$ = −3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}

×: "H" or "L"

DC Recommended Operation Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc + 0.3	
Input low voltage	V_{IL}	−0.3*	—	0.8	

* V_{IL} = −3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics (Vcc = 5V ±10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test Conditions		Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to Vcc		–0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to Vcc		–0.5	—	0.5	µA
Operation power supply current	I_{CC1}	$\overline{CE}$ = V_{IL} V_{IN} = V_{IH} or V_{IL} I_{OUT} = 0mA		—	3	10	mA
Average operating current	I_{CC2}	Min. cycle duty = 100% I_{OUT} = 0mA	55LL	—	45	70	mA
			70LL	—	40	50	
			10LL	—	33	50	
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc – 0.2V	0 to +70°C	—	—	5	µA
			0 to +40°C	—	—	1	
			+25°C	—	0.2	0.5	
	I_{SB2}	$\overline{CE}$ = V_{IH}		—	0.4	2	mA
Output high voltage	V_{OH}	I_{OH} = –1.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V

* Vcc = 5V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	8	pF

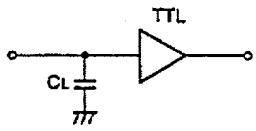
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions (Vcc = 5V ±10%, Ta = 0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH} = 2.2V
Input pulse low level		V_{IL} = 0.8V
Input rise time		tr = 5ns
Input fall time		tf = 5ns
Input and output reference level		1.5V
Output load conditions	-55LL	C_L* = 30pF, 1TTL
	-70LL -10LL	C_L* = 100pF, 1TTL

* C_L includes scope and jig capacitances.



• **Read cycle** ($\overline{WE}$ = "H")

Item	Symbol	-55LL		-70LL		-10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	55	—	70	—	100	—	ns
Address access time	t_{AA}	—	55	—	70	—	100	
Chip enable access time	t_{CO}	—	55	—	70	—	100	
Output enable to output valid	t_{OE}	—	30	—	40	—	50	
Output hold from address change	t_{OH}	15	—	20	—	20	—	
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	10	—	10	—	10	—	
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	—	20	—	25	—	30	
Output enable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	20	—	25	—	30	

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

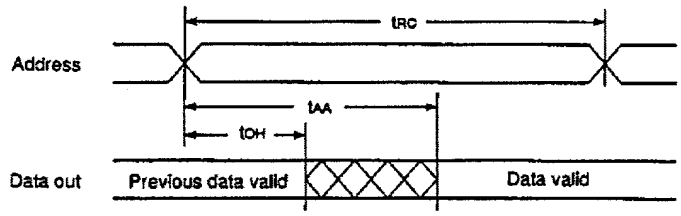
• **Write cycle**

Item	Symbol	-55LL		-70LL		-10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	55	—	70	—	100	—	ns
Address valid to end of write	t_{AW}	50	—	60	—	70	—	
Chip enable to end of write	t_{CW}	50	—	60	—	70	—	
Data to write time overlap	t_{DW}	25	—	30	—	35	—	
Data hold from write time	t_{DH}	0	—	0	—	0	—	
Write pulse width	t_{WP}	40	—	50	—	60	—	
Address setup time	t_{AS}	0	—	0	—	0	—	
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	
Output active from end of write	t_{OW}	10	—	10	—	10	—	
Write to output in high Z	t_{WHZ}*	—	20	—	25	—	25	

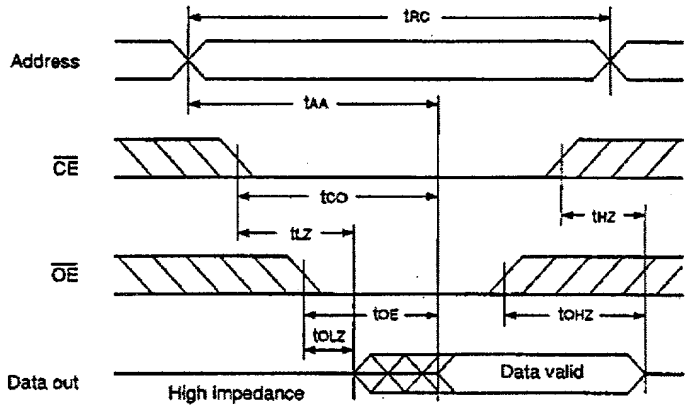
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

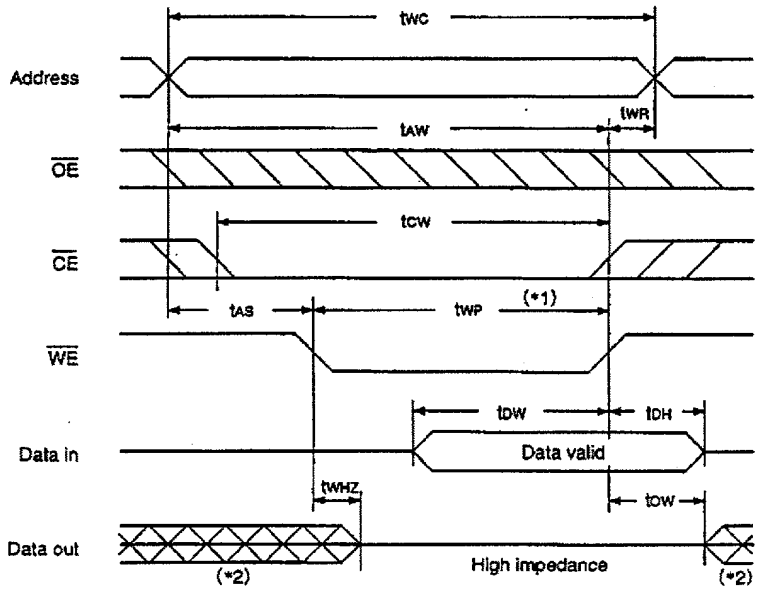
• **Read cycle (1):** $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}



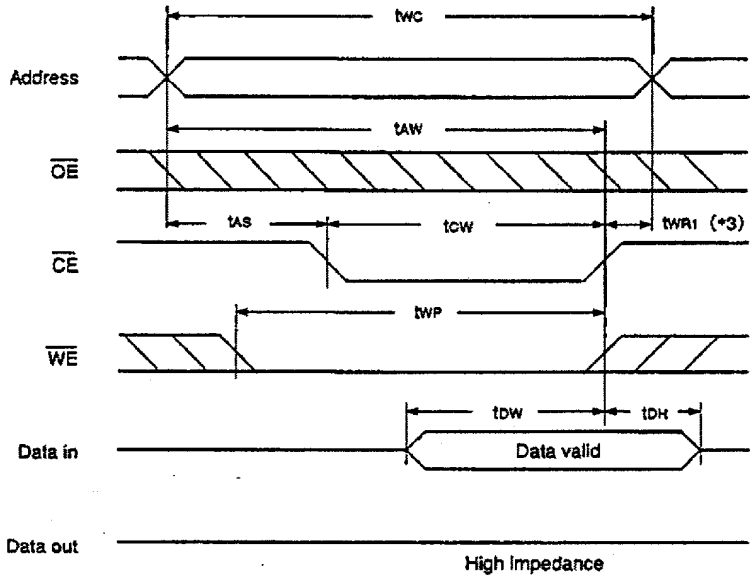
• **Read cycle (2):** $\overline{WE}$ = V_{IH}



• **Write cycle (1):** $\overline{WE}$ control



• **Write cycle (2): $\overline{CE}$ control**



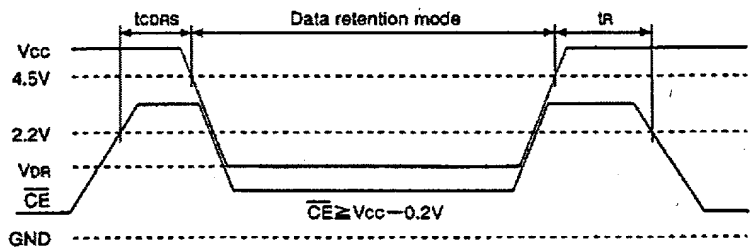
*1 Write is executed when both $\overline{CE}$ and $\overline{WE}$ are at low simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

*3 t_{WR1} is tested from the rising edge of $\overline{CE}$, until the end of the write cycle.

Data retention waveform

• Low supply voltage data retention waveform



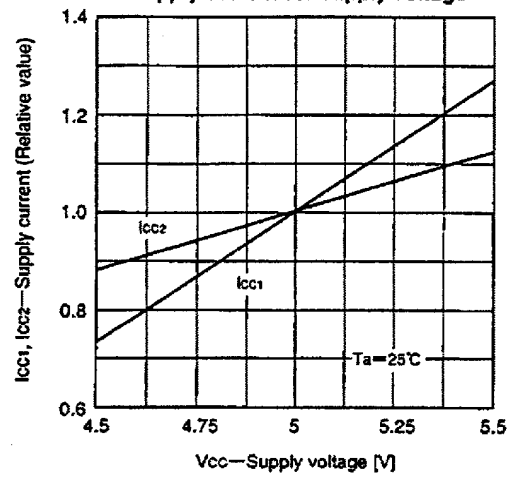
Data Retention Characteristics (Ta = 0 to +70°C)

Item	Symbol	Test condiitions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	$\overline{CE} \geqq Vcc - 0.2V$		2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc = 3.0V, $\overline{CE} \geqq 2.8V$	0 to +70°C	—	—	3	µA
			0 to +40°C	—	—	0.6	
			+25°C	—	0.1	0.3	
	I_{CCDR2}	Vcc = 2.0 to 5.5V, $\overline{CE} \geqq Vcc - 0.2V$		—	0.2*	5	
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t_R			5	—	—	ms

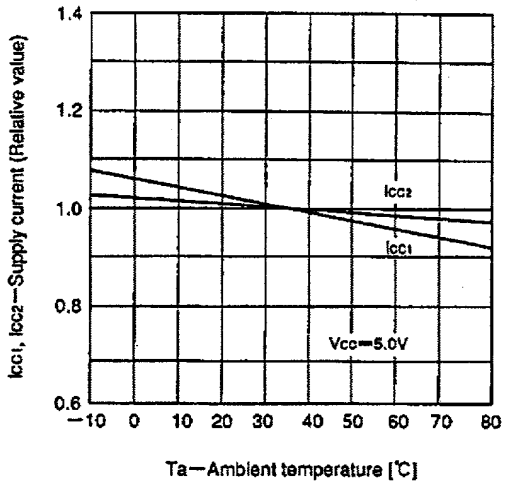
* Vcc = 5V, Ta = 25°C

Example of Representative Characteristics

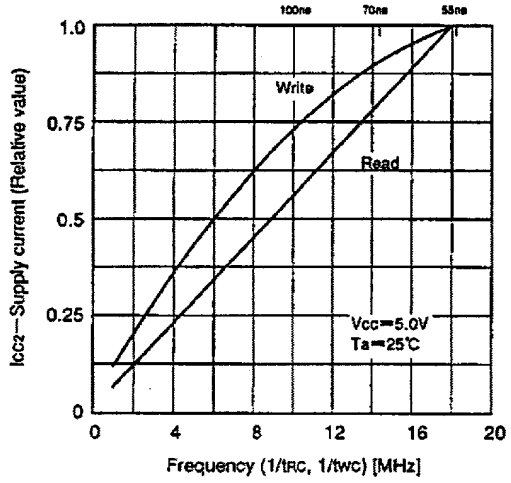
Supply current vs. Supply voltage



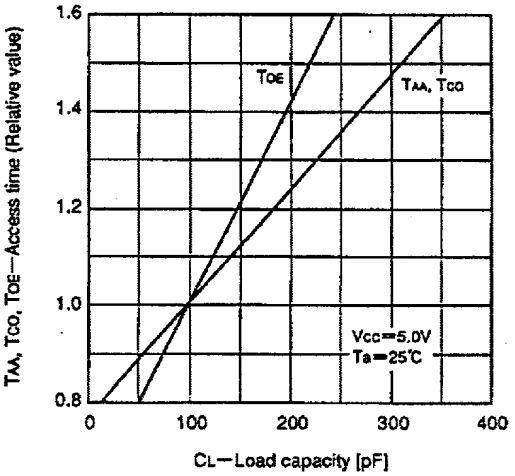
Supply current vs. Ambient temperature



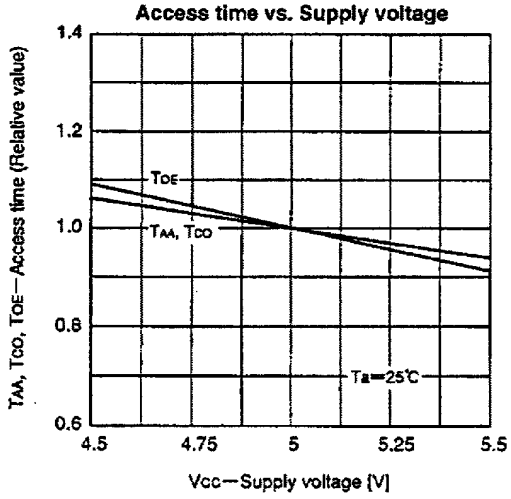
Supply current vs. Frequency



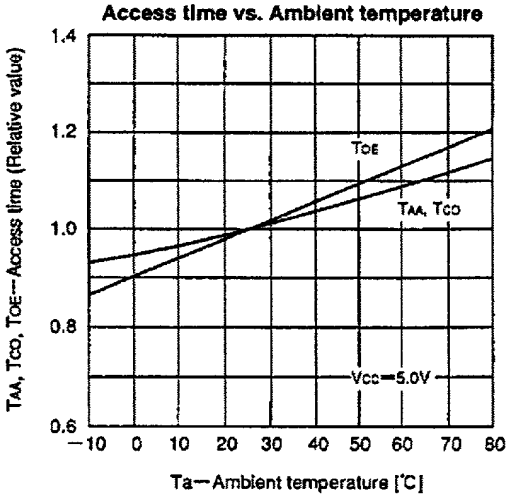
Access time vs. Load capacitance



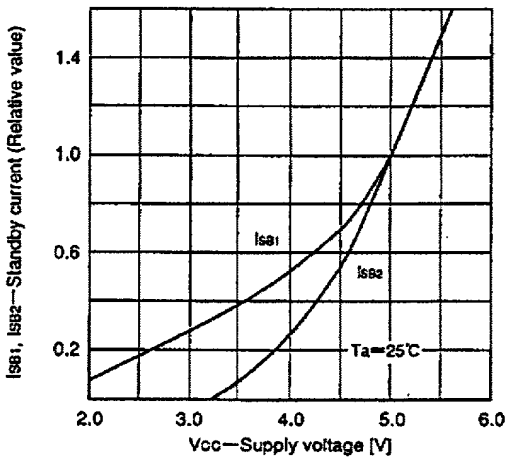
Access time vs. Supply voltage



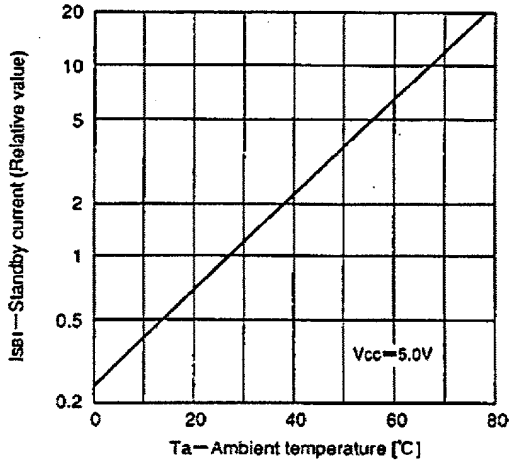
Access time vs. Ambient temperature



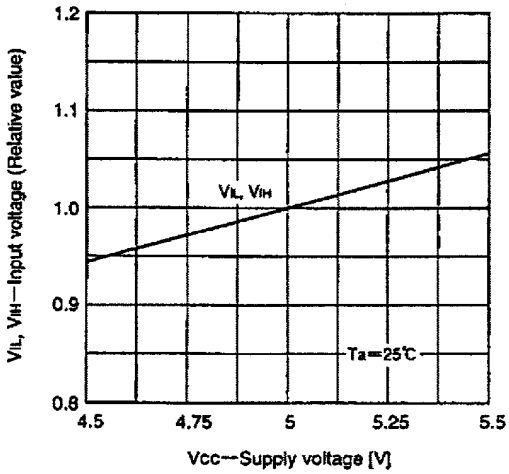
Standby current vs. Supply voltage



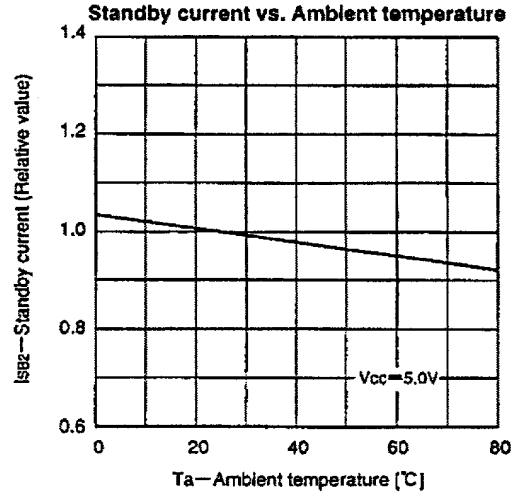
Standby current vs. Ambient temperature



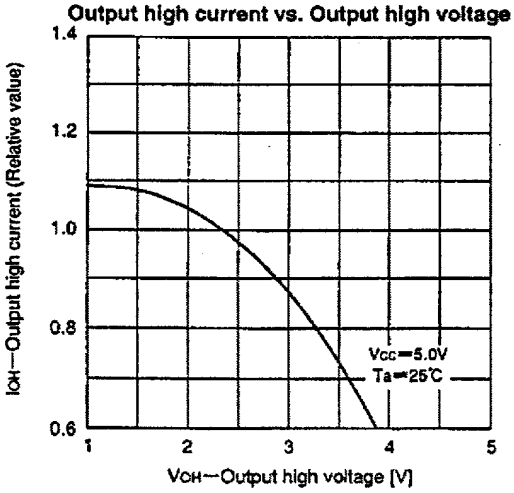
Input voltage level vs. Supply voltage



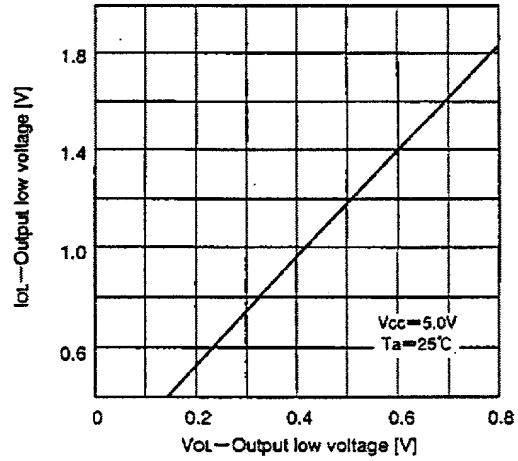
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



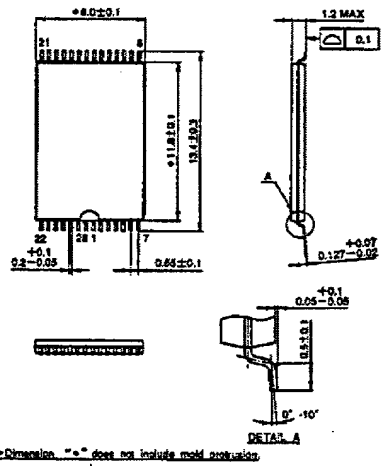
Output high current vs. Output high voltage



Package Outline Unit : mm

CXK58257BTM

28PIN TSOP (Plastic)



NOTE>Dimension "*" does not include mold protrusion.

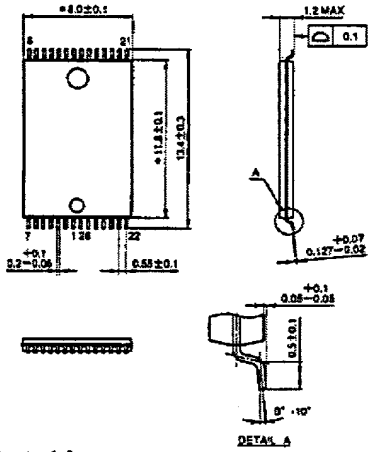
SONY CODE	TSOP-28P-L01
EIAJ CODE	TSOP028-P-0000-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.5g

CXK58257BYM

28PIN TSOP (Plastic)



NOTE>Dimension "*" does not include mold protrusion.

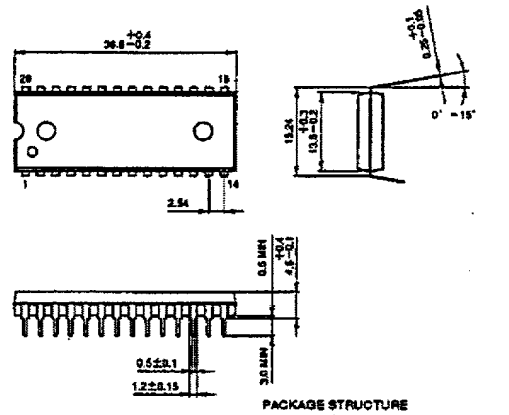
SONY CODE	TSOP-28P-L01R
EIAJ CODE	TSOP028-P-0000-B
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

CXK58257BP

28PIN DIP (PLASTIC) 600mil



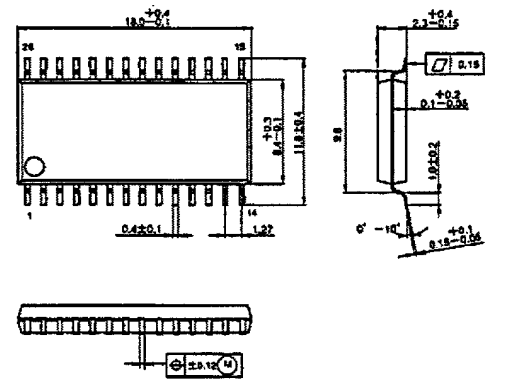
PACKAGE STRUCTURE

SONY CODE	DIP-28P-M4
EIAJ CODE	*DIP28-P-0600-D
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	4.9g

CXK58257BM

28PIN SOP (PLASTIC) 450mil



PACKAGE STRUCTURE

SONY CODE	SOP-28P-L05
EIAJ CODE	*SOP028-P-0450-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.7g