GENNUM CORPORATION

LA200 Series
LA250

SEMICUSTOM LINEAR ARRAYS DATA SHEET

ADVANTAGES OF THE SEMICUSTOM ARE:

- **custom circuitry at low cost**
- **quick turnaround**
- **high reliability**
- **design proprietorship**
- **reduced PCB size**

For complete information about Gennum linear array products, please refer to our Semicustom Design Manual. Kits and manuals are available from Gennum or your local representative.

CIRCUIT DESCRIPTION

The Gennum semicustom integrated circuits are arrays of bipolar transistors, p diffused resistors, pinch resistors, junction capacitors and Schottky diodes. The individual components on the chip are uncommitted.

The user can design his own proprietary circuit using the transistors, resistors, and capacitors available on the chip. Once the circuit is designed and tested with discrete components (provided with the design manual), the interconnection layout is generated and used to manufacture the proprietary circuit.

SEMICUSTOM BIPOLAR ARRAY COMPONENT LIST (20 V MAX. OPERATING VOLTAGE)

		LA250			LA200		
ACTIVE COMPONENTS		L A251	LA252	LA253	LA201	LA202	LA204
Small NPN	- standard	122	92	52	83	46	17
	- Schottky clamped	18	12	8	-	-	8
	- low noise	8	8	8	-	-	-
	Total	148	112	68	83	46	25
Large NPN	-Ic ≤ 100mA	-	-	2	2	2	2
	- Ic ≤ 300mA	4	4	-	-	-	-
	Total	4	4	2	2	2	2
Lateral PNP	-split collectors (2)	36	24	16	26	14	9
	-multiple collectors (6)	13	10	4	-	-	-
	Total	49	34	20	26	14	9
Zener Diode		4	4	4	1	1	1
Large Diode		2	2	2	-	-	-
PASSIVE COMPONENTS							
Junction Capacitor	- 75 pF capacitors	4	4	4	3	3	-
	- 56 pF capacitors	-	-	-	-	-	3
	Total	4	4	4	3	3	3
Various P-Diffused Resistors (total resistance)		1000 K	670 K	340 K	450 K	240 K	170 K
40 K Pinch Resistors		28	28	20	10	8	6
BONDING PADS		40	32	24	24	18	14
CHIP SIZE (mils)		150 x 144	151 x 111	92 x 111	127 x 94	78 x 94	56 x 91

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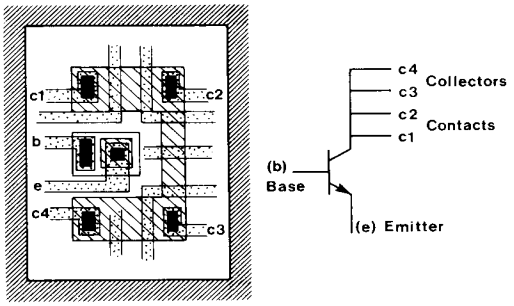
ULA COMPONENT DESCRIPTION

Legend for component drawings

Metallization | Contact | Emitter | Base and Isolation | Base and Isolation in Zener Structure | DeepCollector Diffusion

Small Emitter NPN

The most common circuit element in the array and the one around which the process is optimized is the small npn cell. Since it is the most common cell, it makes sense to include the basic structure to implement cross-unders right in the layout. This is accomplished by making use of the low resistance emitter diffusion which forms the wrap-around collector structure, so that connections made to an npn collector on the circuit schematic may be made to any of the 4 collector contacts. It is not necessary for a particular npn to be used in the circuit before it can be used to implement a cross-under, in which case the transistor collector behaves like a low value resistor. In this mode, the base and emitter contacts should be shorted together.

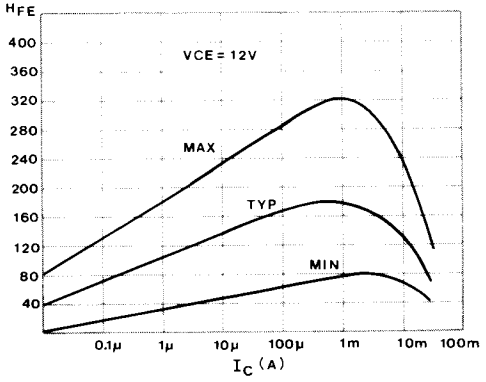


Small NPN Characteristics

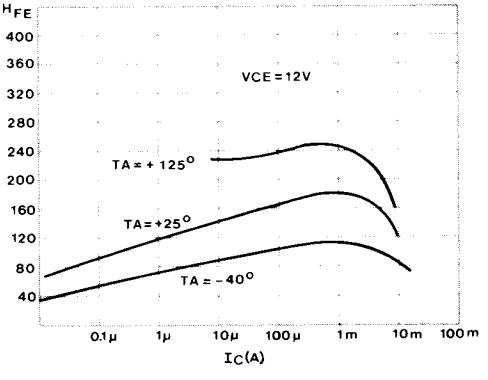
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 1 mA, V_{CE} = 12 V	80		320	
V_{BE}	I_C = 10 μA, V_{CE} = 12 V		600	640	mV
$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA		270	400	mV
	I_C = 1 mA, I_B = .1 mA		100	200	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		10		pA
I_{CBO}	V_{CB} = 12 V		5		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.5		pF
f_T	I_C = 3 mA, V_{CE} = 12 V		250		MHz

ΔV_{BE} for adjacent devices 2mV typ (5mV max)

NPN Graphs

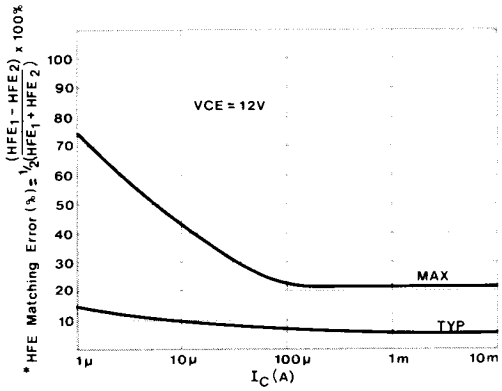


DC Current Gain vs Collector Current



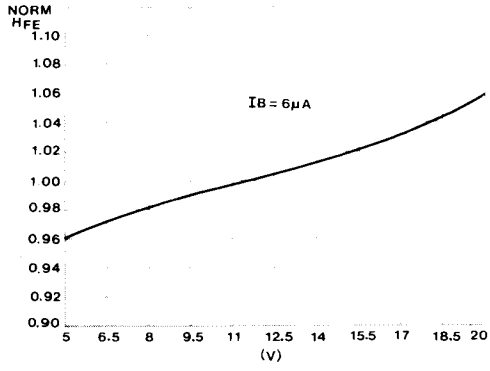
Typical DC Current Gain vs Collector Current over Temperature

NPN Graphs (continued)

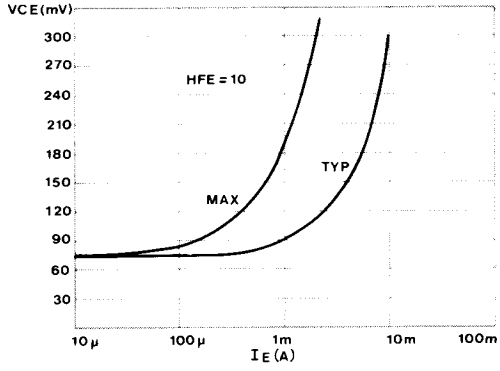


*Adjacent Devices on Array

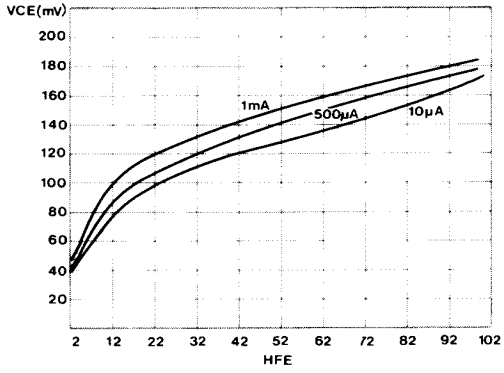
H_{FE} Matching Error (%)



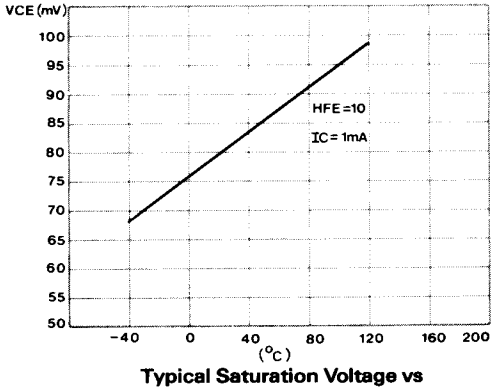
Normalized Forward Gain vs Collector Voltage



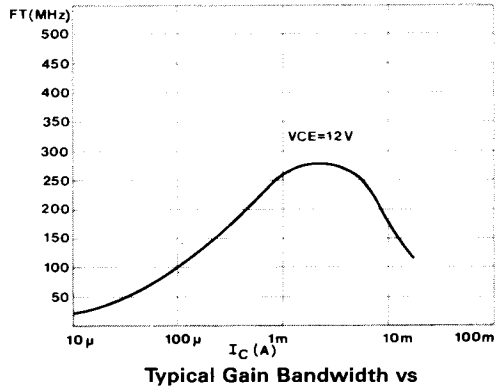
Saturation Voltage vs Emitter Current



Typical Saturation Voltage vs Forced H_{FE}

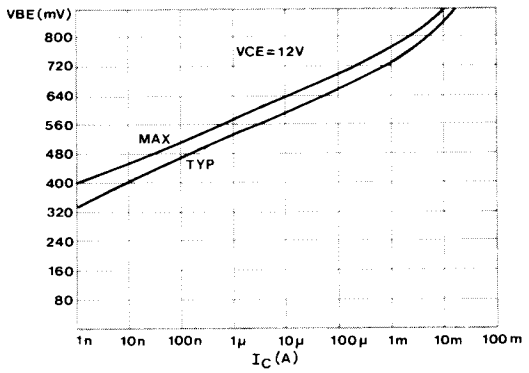


Typical Saturation Voltage vs Ambient Temperature

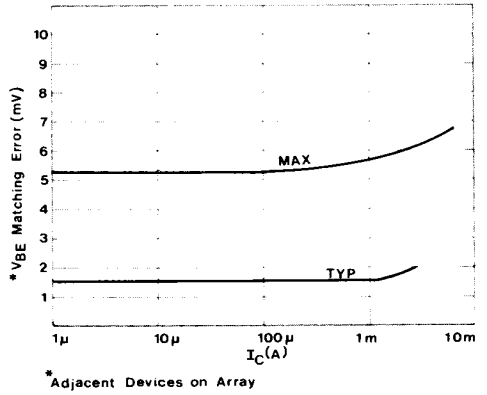


Typical Gain Bandwidth vs Collector Current

NPN Graphs (continued)



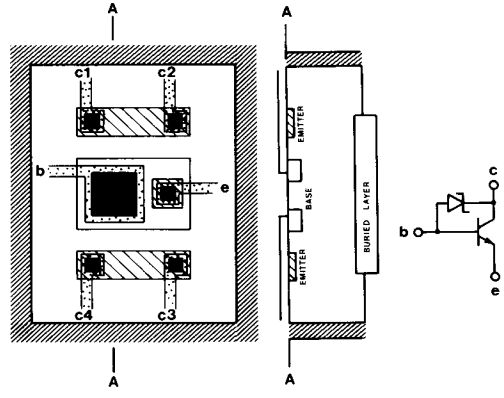
Base Emitter Voltage vs Collector Current



V_{BE} Matching Error

SCHOTTKY CLAMPED NPN

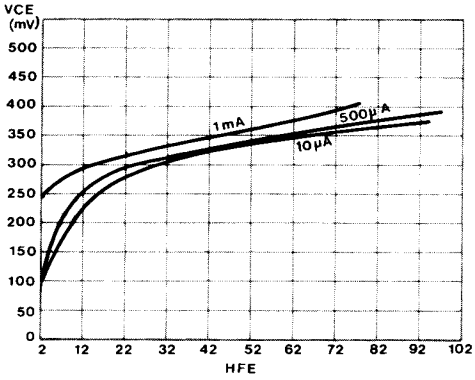
This npn transistor has an additional Schottky diode connected between its base and collector by allowingthe metal to contact the epitaxial layer through a hole in the base diffusion. This Schottky diode can prevent hard saturation when the cell is used as an npn transistor, or it may be accessed independently with the base and collector contacts. Since this transistor cell is not suitable in low saturation applications, the normal wrap-around collector has been replaced by two separate pick-ups which may still be used as low resistance cross-unders, with the resistance between the two collector pick-ups as approximately 150 Ω.



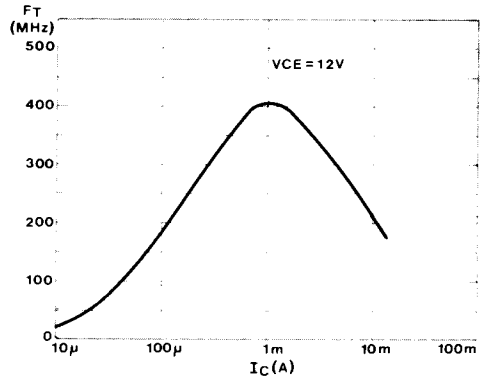
Schottky NPN Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 1 mA, V_{CE} = 12 V	80		320	
V_{BE}	I_C = 10 μA, V_{CE} = 12 V		600	640	mV
V_{BC}	I_C = -10 μA, I_B = 10 μA		410	450	mV
$V_{CE(SAT)}$	I_C = 10 μA, I_B = 1 μA	200	290		mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		200		pA
I_{CBO}	V_{CB} = 12 V		20		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.7		pF
f_T	I_C = 1 mA, V_{CE} = 12 V		400		MHz

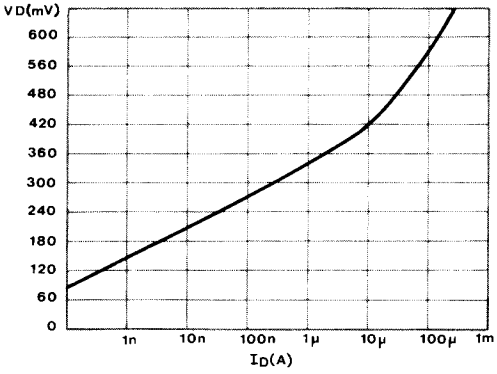
Schottky Graphs



Typical Saturation Voltage vs Forced HFE



Typical Gain Bandwidth vs Collector Current

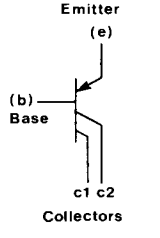


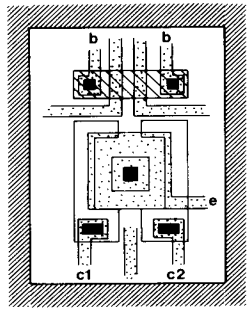
Diode Voltage vs Diode Current

Note: For characteristics not shown see section on Small Emitter NPN

SPLIT COLLECTOR PNP

The pnp transistors are of the lateral action construction with the collector split into two equal segments.
This structure may be used as a single pnp when both collectors are connected together. It may also be considered as two pnp transistors with common emitters and common bases. When considered as two transistors it can be used to implement current sources, current mirrors and area ratios on an integrated circuit.



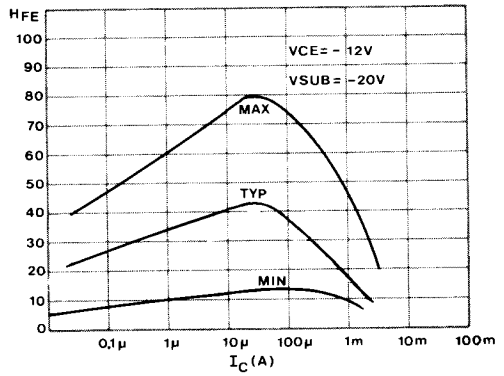


Split Collector PNP (with both collectors connected together)

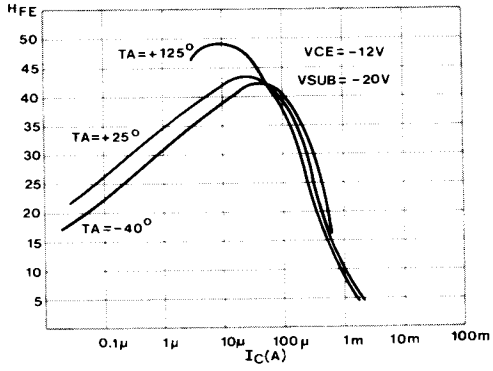
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 30 µA, V_{CE} = -12 V, V_{SUB} = -20 V	15	40		
V_{BE}	I_C = 10 µA, V_{CE} = -12 V, V_{SUB} = -20 V	540	600		mV
$V_{CE(SAT)}$	I_C = 100 µA, I_B = 50 µA, V_{SUB} = -20 V		90	120	mV
BV_{CEO}	I_C = 20 µA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 µA, I_C = 0	20	27		V
I_{CEO}	V_{CE} = -12 V		100		pA
I_{CBO}	V_{CB} = -12 V		5		pA
V_A	I_B = 10 µA, V_{CE} = -5 V and -15 V	30	42		V
C_{OB}	f = 1 kHz, V_{CB} = 0		0.96		pF
f_T	I_C = 100 µA, V_{CE} = -12 V, V_{SUB} = -20 V		3.5		MHz

ΔV_{BE} for adjacent devices 2mV typ (6mV max)

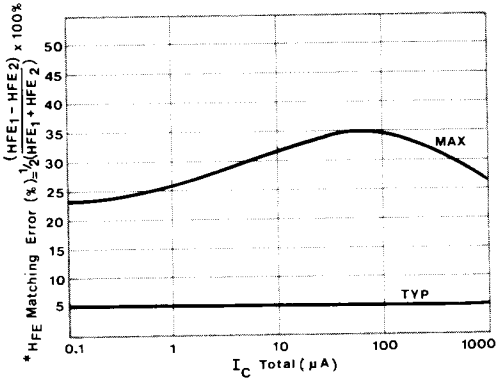
PNP Graphs



DC Current Gain vs Collector Current

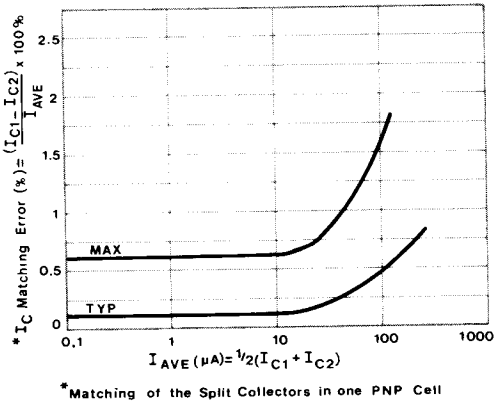


Typical DC Current Gain vs Collector Current over Temperature



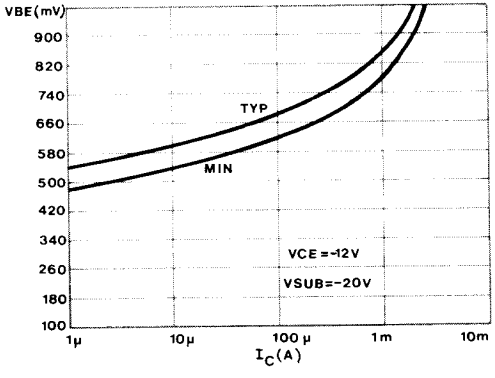
*Adjacent Devices on Array with both Collectors joined

H_{FE} Matching Error

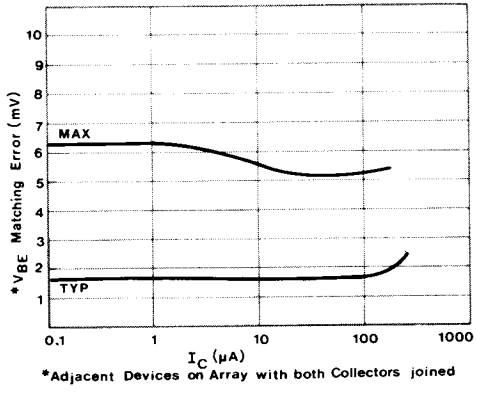


*Matching of the Split Collectors in one PNP Cell

Collector Current Matching (%)



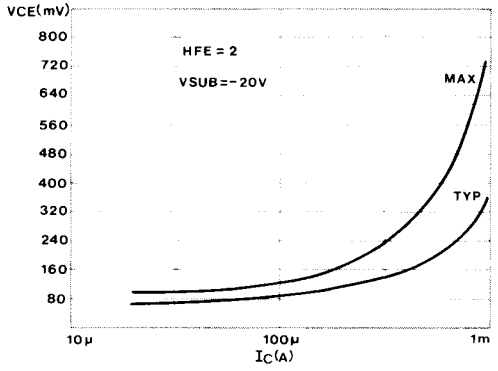
Base Emitter Voltage vs Collector Current



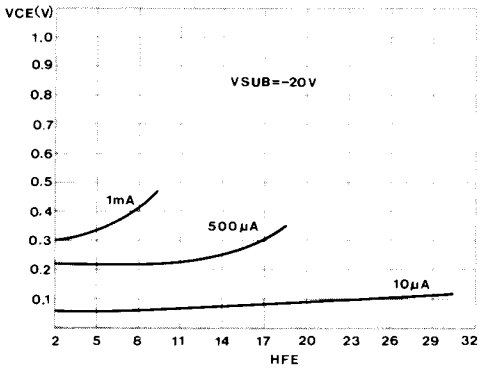
*Adjacent Devices on Array with both Collectors joined

V_{BE} Matching Error

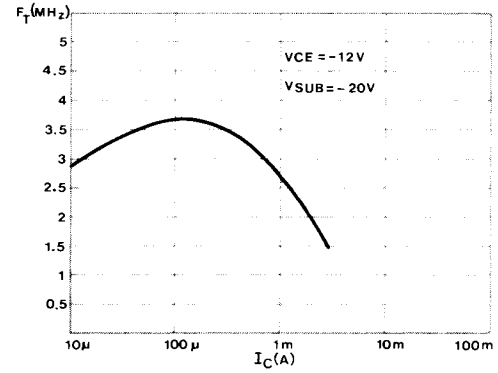
PNP Graphs (continued)



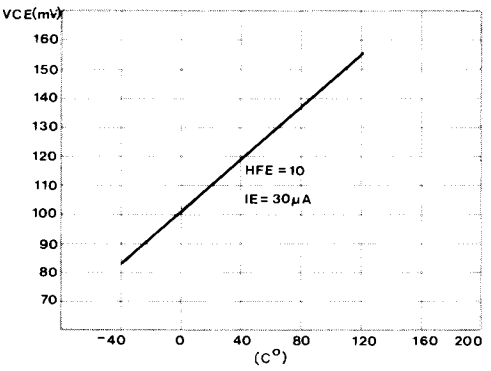
Saturation Voltage vs Emitter Current



Typical Saturation Voltage vs Forced HFE



Typical Gain Bandwidth vs Collector Current

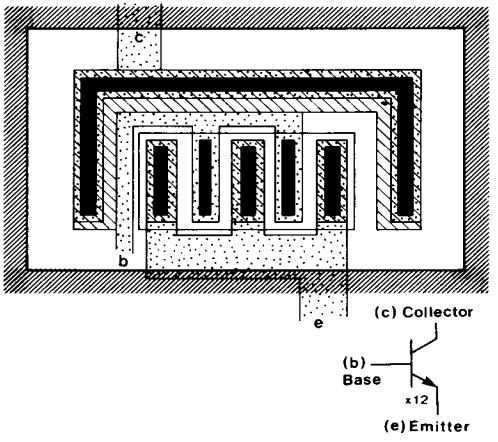


Saturation Voltage vs Ambient Temperature

LARGE NPN

This is approximately equivalent to 12 small npns connected in parallel. Since there are only two in the array, no provision has been made for cross-unders in this structure, although care has been taken to allow the base connection to be made from either side of the transistor. Note that each of these transistors can pass substantial current but the main limiting factor is probably the power being dissipated by the device. Here, the power is the product of the voltage across the transistor and the current in the collector, e.g. $P_d = V_{CE} \cdot I_C$.

This is one contribution to the overall power being dissipated on the die, which should be limited according to the chosen package.

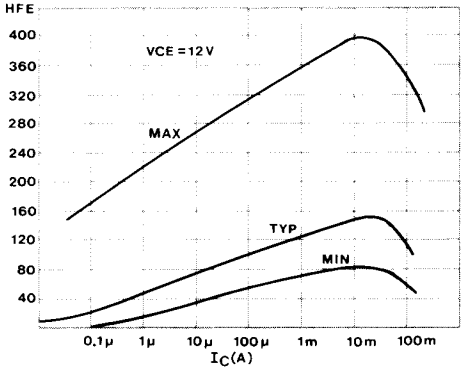


Large NPN Characteristics

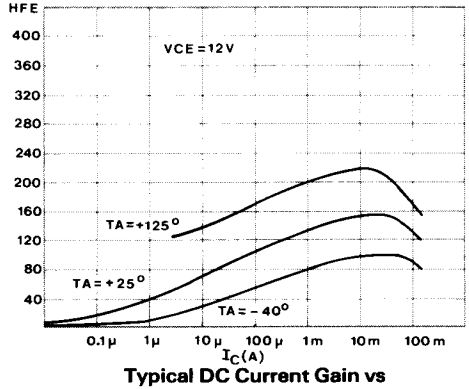
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 12 mA, V_{CE} = 12 V	80		400	
V_{BE}	I_C = 10 mA, V_{CE} = 12 V		790	850	mV
	I_C = 1 mA, V_{CE} = 12 V		680	740	mV
$V_{CE(SAT)}$	I_C = 1 mA, I_B = .1 mA		60	100	mV
	I_C = 10 mA, I_B = 1 mA		160	350	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		15		pA
I_{CBO}	V_{CB} = 12 V		30		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		10.7		pF
f_T	I_C = 18 mA, V_{CE} = 12 V		350		MHz

1mV typ (5mV max)

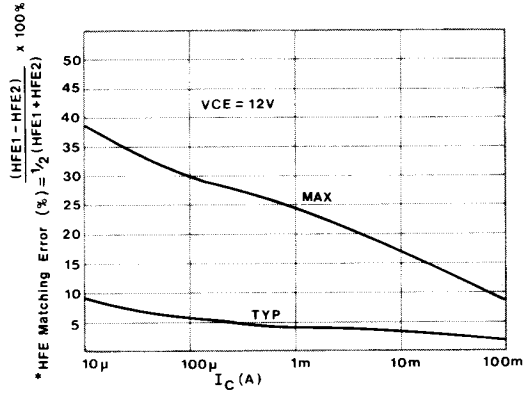
Large NPN Graphs



Typical DC Current Gain vs Collector Current

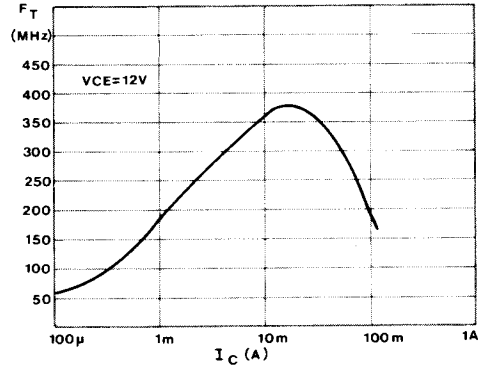


Typical DC Current Gain vs Collector Current over Temperature



*Adjacent Devices on Array

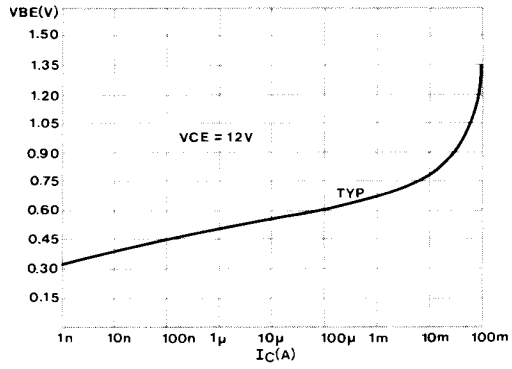
H_{FE} Matching Error



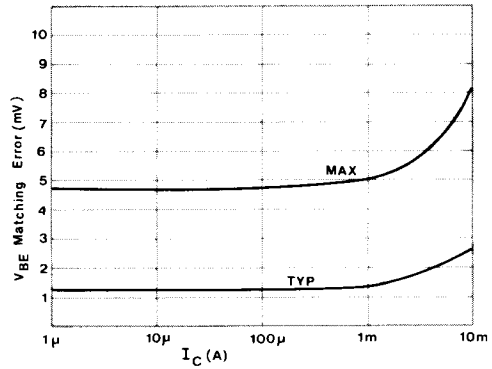
Typical Gain Bandwidth vs Collector Current

500 - 67 - 4

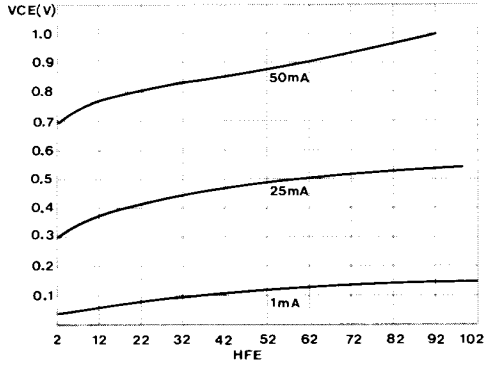
Large PNP Graphs



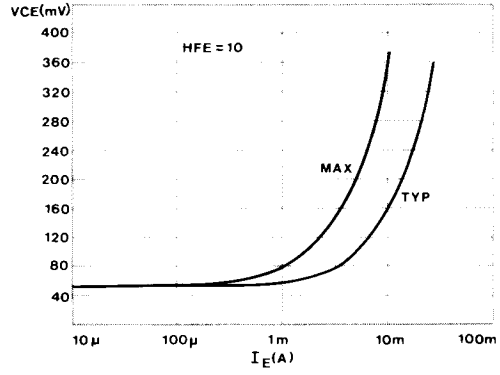
Base Emitter Voltage vs Collector Current



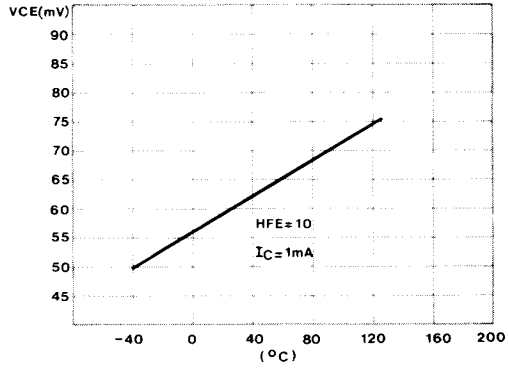
V_{BE} Matching Error



Typical Saturation Voltage vs Forced HFE



Saturation Voltage vs Emitter Current



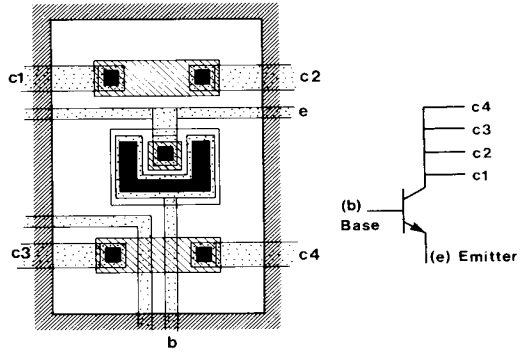
Typical Saturation Voltage vs Ambient Temperature

LOW NOISE NPN
Legend for component drawings

Metallization | Contact | Emitter | Base and Isolation | Base on Isolation in Zener Structure | Deep Collector Diffusion

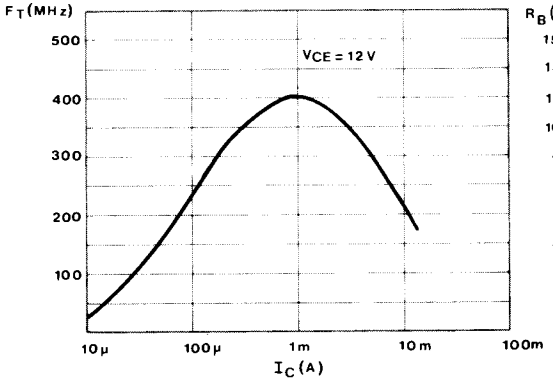
This device features a large base contact area which provides lower noise and better high frequency performance than the standard small npn.

Although intended primarily for the input stages of amplifiers, it may also be used for any standard small npn applications. The two collector pick-ups may be used as cross-unders if required, and in this respect the device is similar to the Schottky npn transistor.

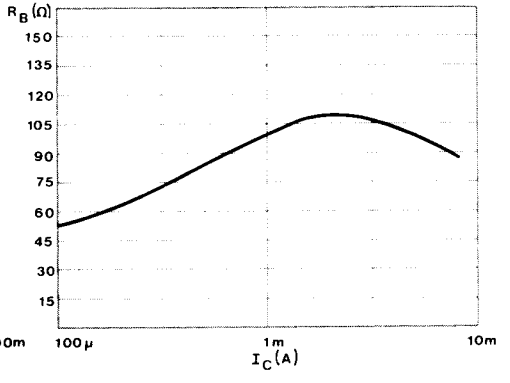


Low Noise NPN Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 1 mA, V_{CE} = 12 V	80		320	
V_{BE}	I_C = 10 μA, V_{CE} = 12 V		600	640	mV
$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA		270	400	mV
	I_C = 1 mA, I_B = 1 mA		100	200	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		12		pA
I_{CBO}	V_{CB} = 12 V		6		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.7		pF
f_T	I_C = 3 mA, V_{CE} = 12 V		350		MHz

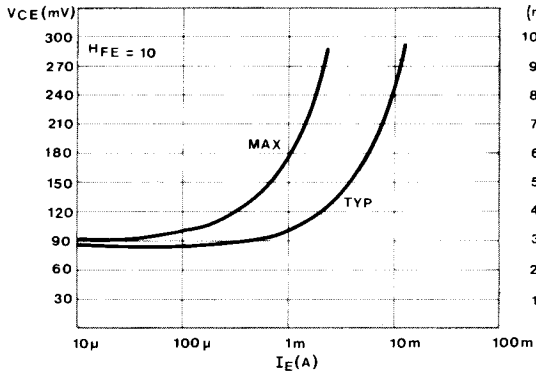


Typical Gain Bandwidth vs Collector Current

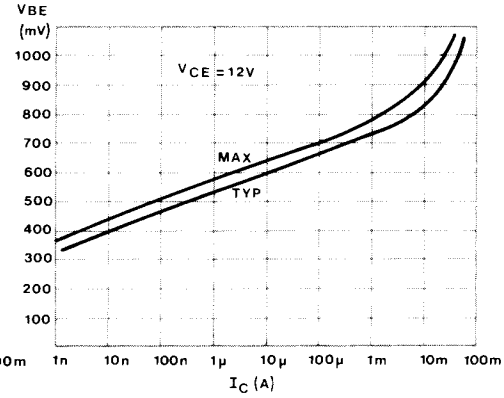


Typical Base Resistance vs Collector Current

Low Noise NPN Graphs (continued)



Saturation Voltage vs Emitter Current



Base Emitter Voltage vs Collector Current

Note: For characteristics not shown see section on Small Emitter NPN

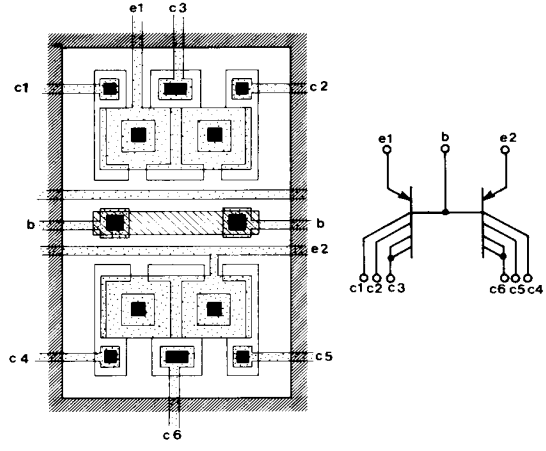
MULTIPLE COLLECTOR PNP

These pnp transistors are of the lateral action construction with the collector split in six segments.

Collectors c1, c2, c4 and c5 have the same effective "emitter area" as standard split collector pnp's. Collectors c3 and c6 are "double area".

The device can be used as a multiple current source or by connecting all collectors together as a pnp with better current handling, i.e. peak H_{FE} approx .- 120 µA.

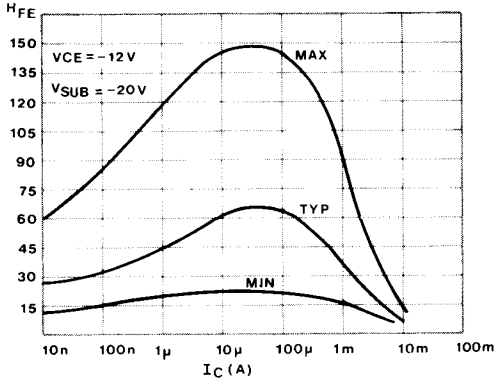
We suggest e1 and e2 be shorted together to prevent possible crosstalk between emitters. If c6 and c3 are considered as two single collectors in parallel, then the current matching performance of the collectors is as described by the collector current matching graph for the twin collector PNP.



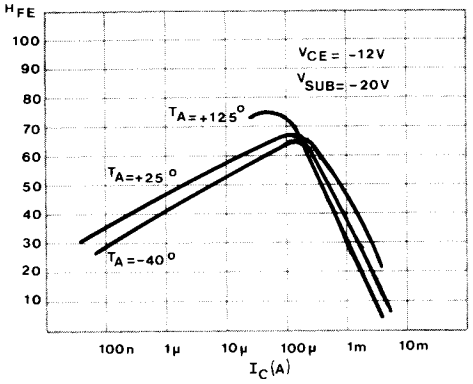
Multiple Collector PNP
(with all collectors connected together and emitters connected together)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 120 µA, V_{CE} = −12 V, V_{SUB} = −20 V	20	65		
V_{BE}	I_C = 40 µA, V_{CE} = −12 V, V_{SUB} = −20V	540	600		mV
$V_{CE(SAT)}$	I_C = 400 µA, I_B = 200 µA, V_{SUB} = −20 V		90	120	mV
BV_{CEO}	I_C = 20 µA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 µA, I_C = 0	20	27		V
I_{CEO}	V_{CE} = −12 V		400		pA
I_{CBO}	V_{CB} = −12 V		20		pA
V_A	I_B = 10 µA, V_{CE} = −5 V and −15 V	30	70		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.8		pF
f_T	I_C = 400 µA, V_{CE} = −12 V, V_{SUB} = −20 V		3.5		MHz

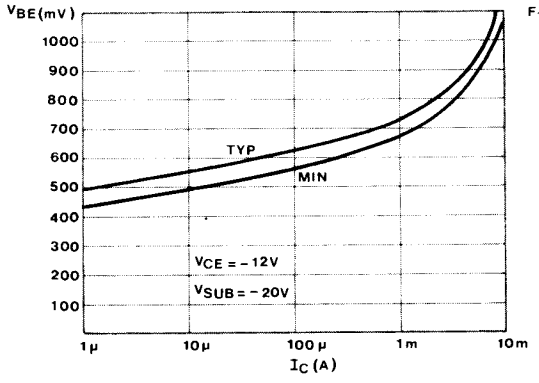
Multiple Collector PNP Graphs (continued)



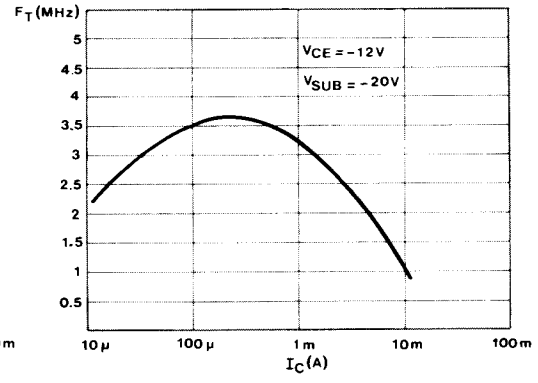
DC Current Gain vs Collector Current



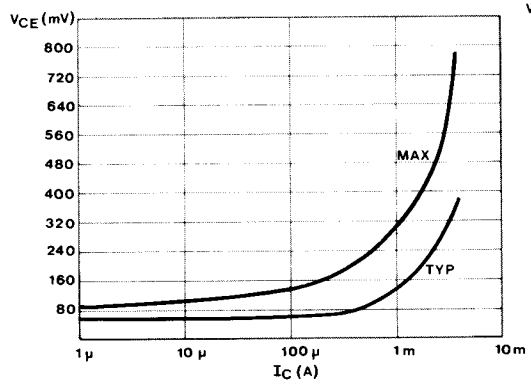
Typical DC Current Gain vs Collector Current over Temperature



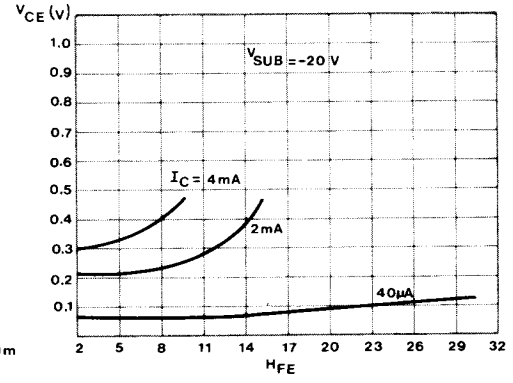
Base Emitter Voltage vs Collector Current



Typical Gain Bandwidth vs Collector Current

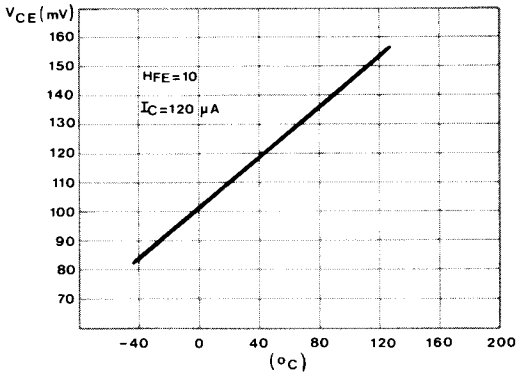


Saturation Voltage vs Collector Current



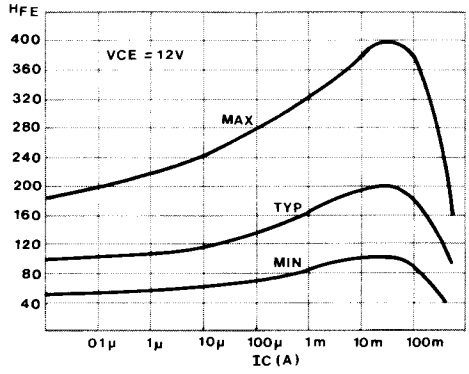
Typical Saturation Voltage vs Forced H_{FE}

Multiple Collector PNP Graphs (continued)



Typical Saturation Voltage vs Ambient Temperature

Power NPN Graph



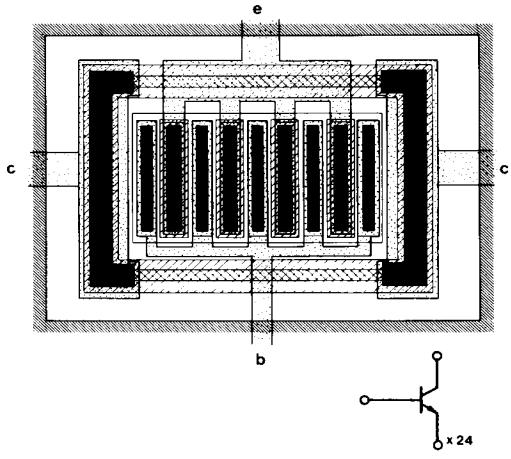
DC Current Gain vs Collector Current

POWER NPN

This transistor has approximately twice (2x) the emitter area of the large npn device on the LA200 series arrays and twenty four times (24x) the emitter area of the small npn; hence' a correspondingly higher current capability (I_C max. = 300 mA). In addition to being physically larger, the device has a number of extra features which offer an enhanced performance over the LA200 series large npn.

These features are:

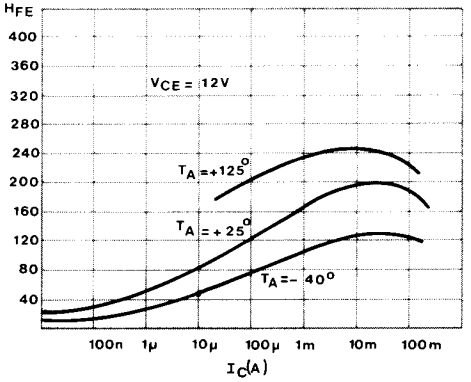
- Four separate emitter structures to provide improved gain at high collector currents.
- Five base contacts to reduce the VBE for high base currents and improve switching speed.
- An all-around deep collector diffusion to ensure a low saturation voltage in switching applications.



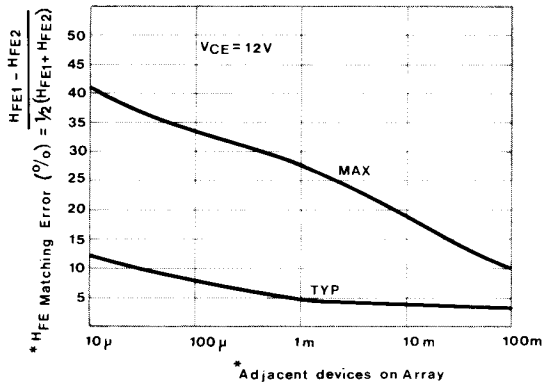
Power NPN Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 20 mA, V_{CE} = 12 V	100		400	
V_{BE}	I_C = 10 mA, V_{CE} = 12 V		660		mV
	I_C = 1 mA, V_{CE} = 12 V		595		mV
$V_{CE(SAT)}$	I_C = 1 mA, I_B = 1 mA		15	26	mV
	I_C = 10 mA, I_B = 1 mA		50	100	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		50		pA
I_{CBO}	V_{CB} = 12 V		25		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		14		pF
f_T	I_C = 36 mA, V_{CE} = 12 V		350		MHz

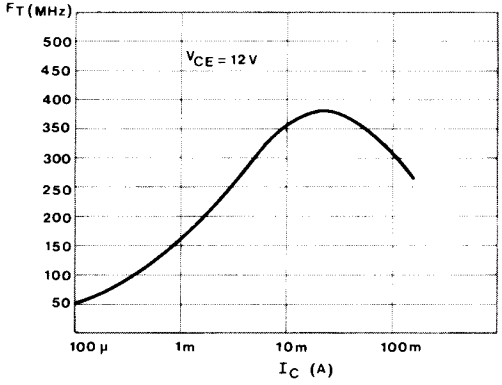
Power NPN Graph (continued)



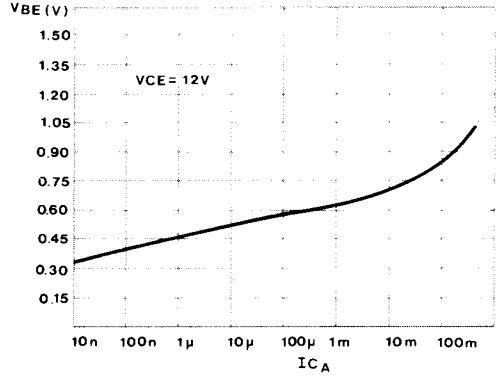
Typical DC Current Gain vs Collector Current over Temperature



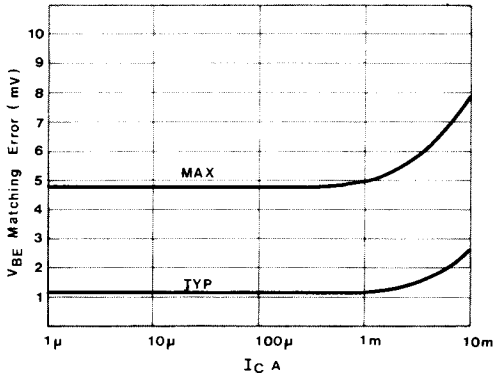
H_{FE} Matching Error



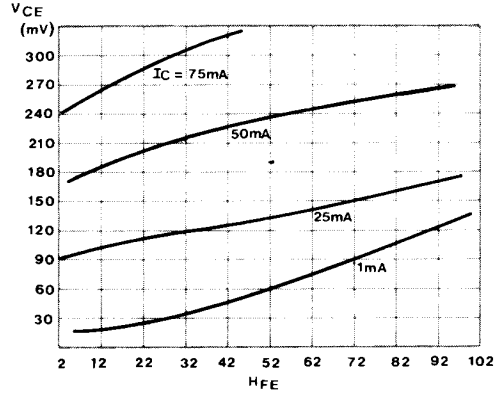
Typical Gain Bandwidth vs Collector Current



Typical Base Emitter Voltage vs Collector Current

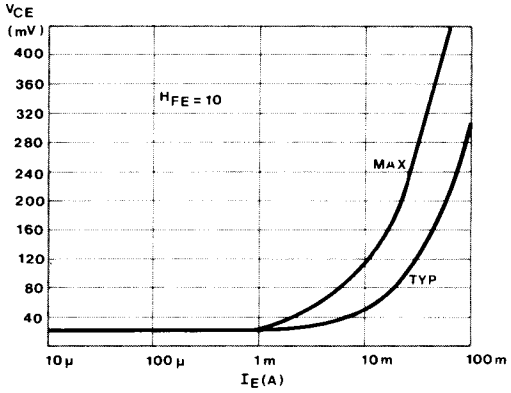


V_{BE} Matching Error



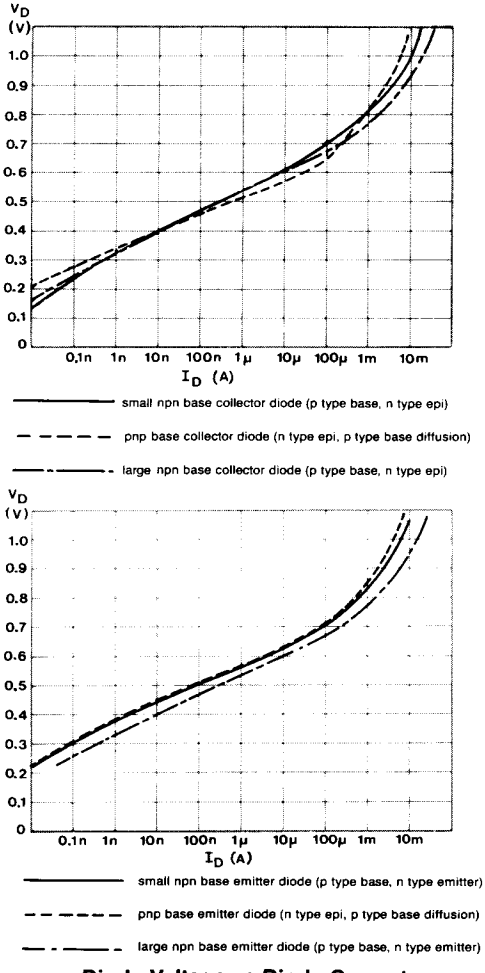
Typical Saturation Voltage vs Forced H_{FE}

Power NPN Graph (continued)



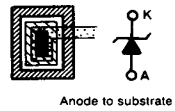
Saturation Voltage vs Emitter Current

Zener Diode Graphs



Diode Voltage vs Diode Current

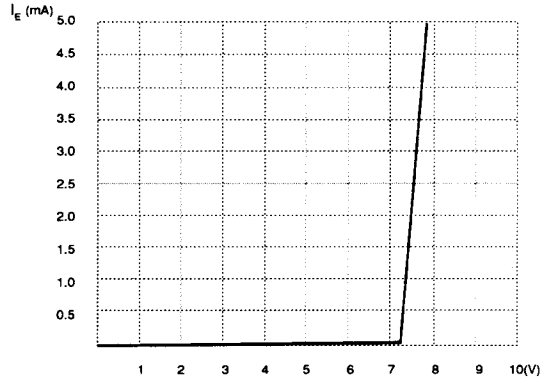
ZENER DIODE



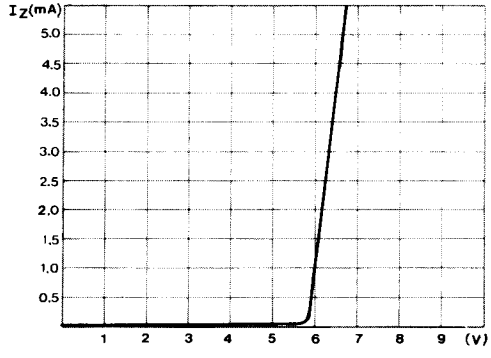
Anode to substrate

This is a generally accepted term for any p-n junction used in thereverse breakdown mode. The voltage at which the reverse biased junction starts to pass significant current is a function of the doping levels of the p-type and the n-type semi-conductor in question. Any number of components on the array may be used in such a way that it will break down a junction and pass current, however, the voltage at which this happens directly affects the temperature coefficient of the resulting reference voltage. The zener diode which is specifically provided as a voltage reference has a breakdown of approximately 5.8 V with respect to substrate. The sandwich capacitors may be used in this mode with a zener diode breakdown of approximately 5.8 V ±0.5 V across the capacitor contacts and without respect to substrate. The temperature coefficient of breakdown voltage is +200 ppm/°C.

Any npn transistor may be used as a zener reference by reverse biasing the base-emitter junction which will break down at approximately 7.5 V with a slope resistance of 100 Ω.



Breakdown Voltage of Reverse Biased Base – Emitter Junction of Small NPN

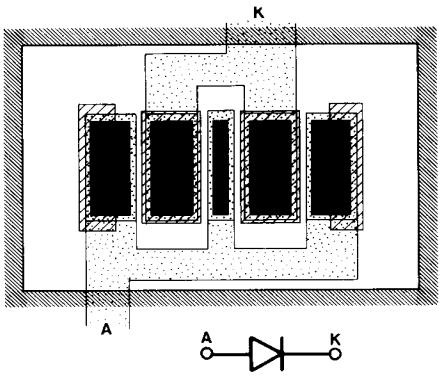


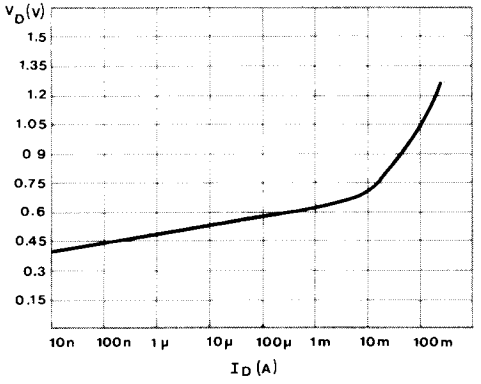
Zener Diode Breakdown Characteristics

DIODES

Large Diode

Two large diodes are provided on the LA251 ans LA252 arrays for applications where high forward current is required. The reverse breakdown characteristic is similar to that of an npn base-emitter junction.





Typical Diode Voltage vs Diode Current

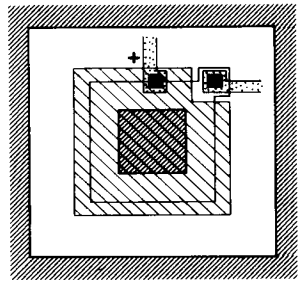
Implementing Diodes using Array Transistors

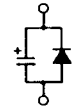
		Diode Voltage at 10 µA	Reverse Breakdown Voltage
Small/Low noise npn	base - emitter	0.6	7.5 V
Small/Low noise npn	base - collector	0.6	>20 V
Small/Multiple pnp	base - emitter	0.6	>20 V
Schottky npn	base - collector	0.4	>20 V
Large/Power npn	base - emitter	0.6	7.5 V
	base - collector	0.6	>20 V

CAPACITORS

The three large area capacitors which are in the corners of the die are junction capacitors with an emitter (diffusion) on base (diffusion) on isolation construction which is often referred to as a *sandwich capacitor*. This type of capacitor has an equivalent circuit as shown: Thus the forward bias voltage is approximately 0.6 V and the reverse bias breakdown voltage is that of the zener diode at 5.8 V (approximately). The nominal value is 75 pF.

In addition, the intrinsic capacitance of any of the structures may be used. In particular, the reverse biased collector to base junction of the npn structures may be used at any voltage up to 20 V.



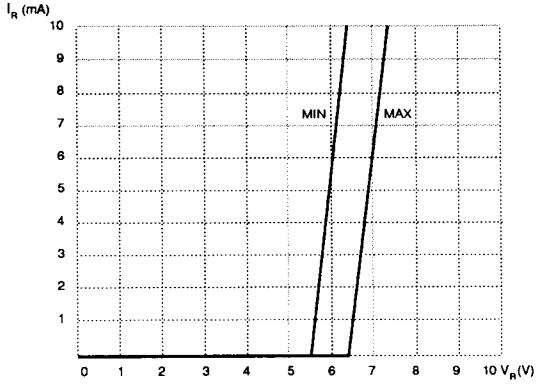


Capacitors

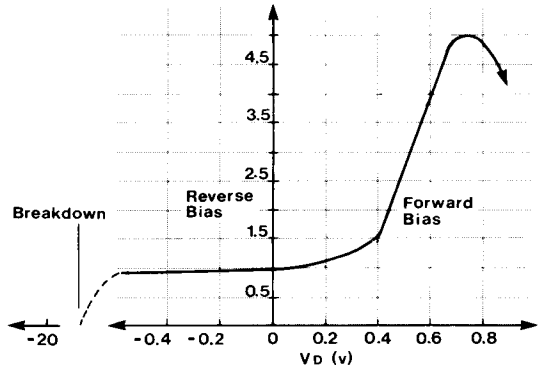
TYPE	NOMINAL VALUE	TOLERANCE OF NOMINAL	ZENER BREAKDOWN VOLTAGE	TEMPERATURE COEFFICIENT OF BREAKDOWN VOLTAGE
Sandwich	*75 pF	± 20%	5.8 V ± 0.5 V	+ 200 ppm/°C
Collector-Base Junction of small npn	0.4pF	± 20%	> 20 V	Do not use in breakdown mode
Collector-Base Junction of large npn	4.7 pF	± 20%	> 20 V	Do not use in breakdown mode
Emitter-Base Junction of small npn	0.7pF	± 20%	7.5 ± 1 V	+ 500 ppm/°C
Emitter-Base Junction of large npn	5.7 pF	± 20%	7.5 ± 1 V	+ 500 ppm/°C

* 56 pF on LA204 array

Capacitors (continued)



Reverse Breakdown Characteristic of Sandwich Capacitor

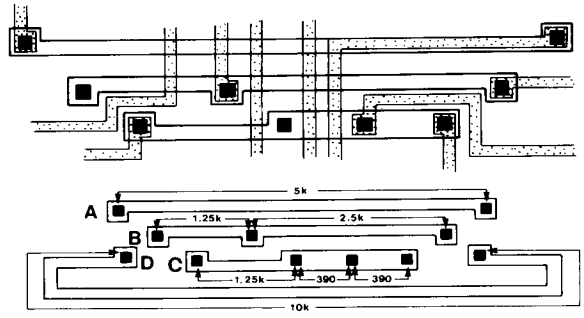


Normalized Capacitance (with respect to C_{JO}) for a PN Junction Capacitor

RESISTORS

All the resistors in the common land are formed during the base diffusion for the npn transistors and are termed "base resistors".

They have nominal values of 10 k (250 series only), 5 k, 2.5 k, 1.25 k and 390 Ω as shown on the diagram of a resistor grouping but their absolute values are dependent on the base diffusion sheet resistivity and so may have a variation of ±25%. However, a ratio of one resistor to another is considerably better and for identical resistors lying side by side on the die the matching tolerance will be ± 4% at the three sigma points.



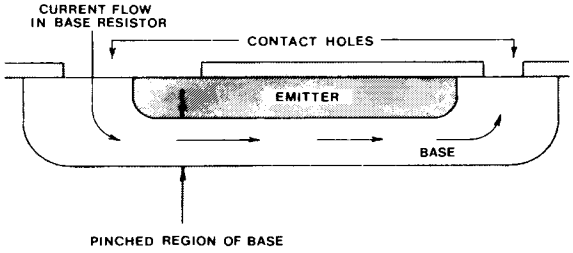
Notes:
1. Resistor values are shown in ohms and are the resistance between adjacent contacts.
2. In the above combination of narrow and wide resistors matching is worse than for like types.

Resistors

TYPE	NOMINAL VALUE	ABSOLUTE TOLERANCE	MATCHING TOLERANCE	TEMPERATURE COEFFICIENT
A	5 k	± 25%	± 4%	+ 2000 ppm/°C
B	2.5 k	± 25%	± 4%	+ 2000 ppm/°C
	1.25 k			
C	1.25 k	± 25%		+ 2000 ppm/°C
	390		± 2%	
	390		± 2%	
D	10 k	± 25%	± 4%	+ 2000 ppm/°C
Pinch	40 k	+ 100% − 50%	± 15%	+ 5000 ppm/°C

PINCH RESISTORS

A pinch resistor is formed by putting emitter diffusion on top of a base resistor so that theeffective thickness of the resistor is greatly reduced. In this way, the resistance may be increased by a factor of ten.

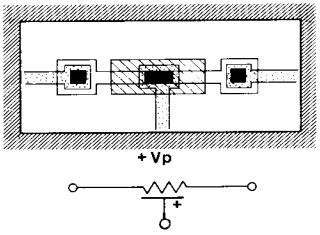


Sectional View of Pinch Resistors

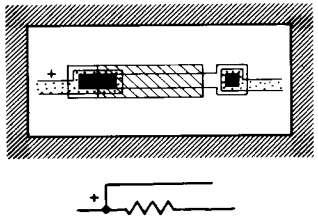
By applying a bias voltage to the emitter region, the associated depletion region further pinches off the base resistor until the reverse breakdown voltage is reached. Since this is the same as a reverse biased base emitter junction of an npn transistor, the pinch resistor will break down at approximately 7.5 volt. A full description of the voltage dependence of the resistor as the bias voltage is applied is shown on the graph Pinch Resistance vs Applied Voltage.

LA250 SERIES PINCH RESISTOR

This is essentially the same device as on the LA200 series, except a separate contact is provided for applying the bias voltage, allowing greater flexibility in layouts. As always, the bias contact should be connected to the most positive end of the resistor.



LA250 Small Series Pinch Resistor

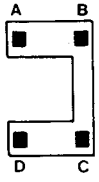


CROSS - UNDERS

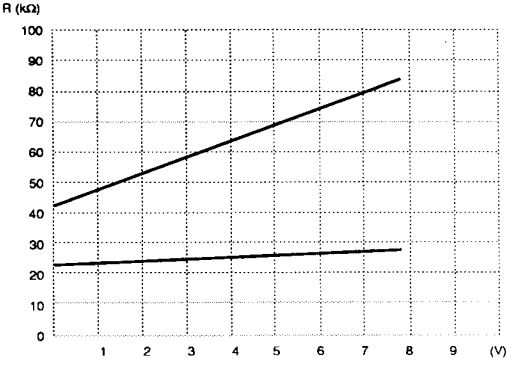
Standard Small NPN

The resistance between the four collector contacts is distributive, hence it is best described by a matrix.
e.g. $R_{AC} = 20\ \Omega$

Ω	B	C	D
A	7	20	23
B	-	16	20
C	16	-	7

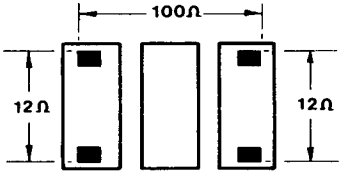


Additional Data for Emitter Diffusion Resistors (cross - unders)		
ABSOLUTE TOLERANCE	MATCHING TOLERANCE	TEMPERATURE COEFFICIENT
± 50%	± 5%	+ 600 ppm/°C

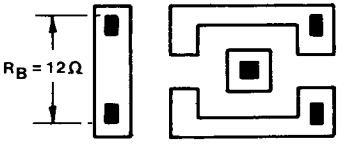


Pinch Resistance vs Applied Voltage

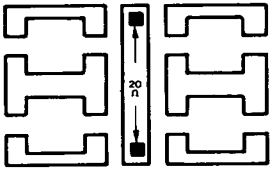
SCHOTTKY/LOW NOISE NPN

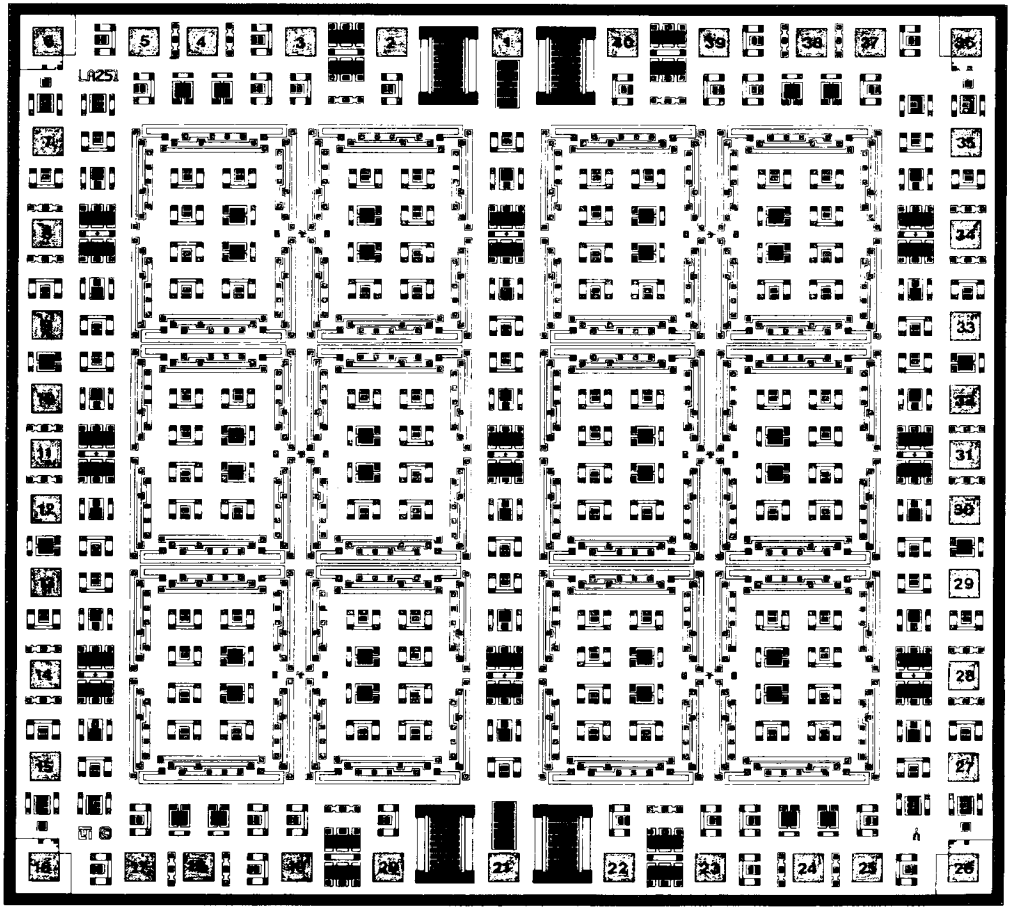


SPLIT COLLECTOR PNP BASE



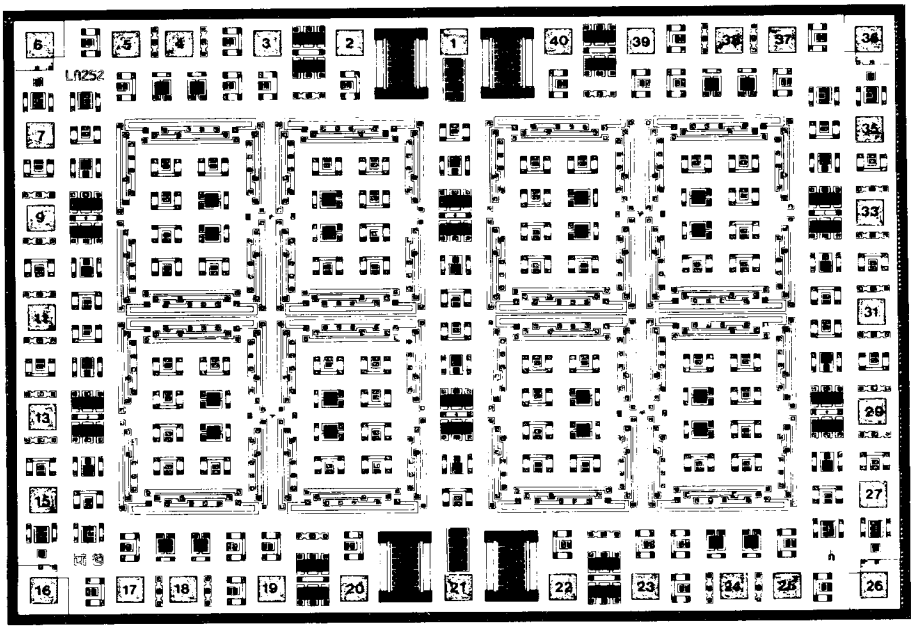
MULTIPLE COLLECTOR PNP BASE





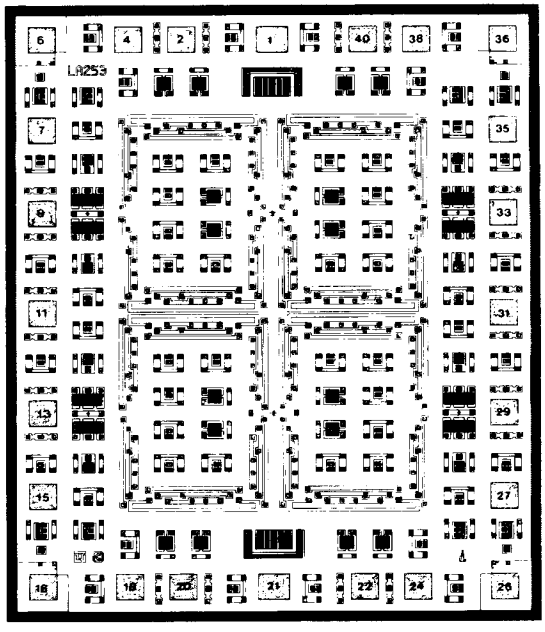
LA251 (SIZE 150 x 144 mils)
Maximum number of bonding pads available - 40

MODULA LA250 SERIES ARRAY LAYOUT



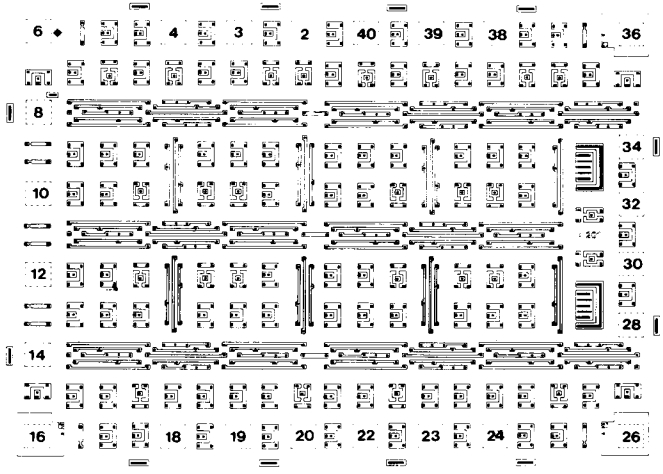
LA252 (SIZE 151 x 111 mils)
Maximum number of bonding pads available - 32

MODULA LA250 SERIES ARRAY LAYOUT



LA253 (SIZE 92 x 111 mils)
Maximum number of bonding pads available - 24

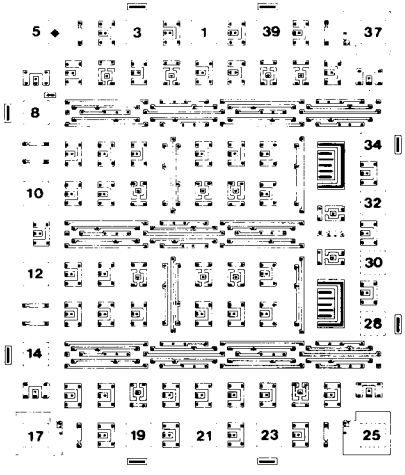
MODULA LA250 SERIES ARRAY LAYOUT



LA201 (SIZE 127 x 94 mils)

Maximum number of bonding pads available - 24

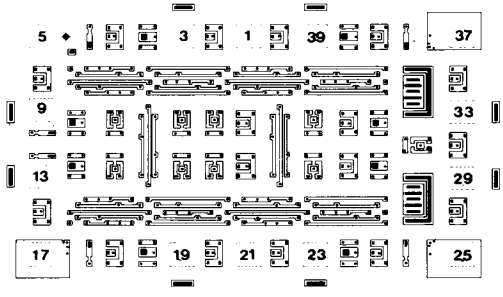
LA200 SERIES ARRAY LAYOUT



LA202 (SIZE 78 x 94 mils)

Maximum number of bonding pads available - 18

LA200 SERIES ARRAY LAYOUT



LA204 (SIZE 56 x 91 mils)

Maximum number of bonding pads available - 18

LA200 SERIES ARRAY LAYOUT