SONY

CXK58257BTM/BYM -70LLX/10LLX

32768-word × 8-bit High Speed CMOS Static RAM

Description

The CXK58257BTM/BYM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits.

A polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

Special feature are operating on a single 5V supply, low power consumption and high speed.

The CXK58257BTM/BYM is a suitable RAM for portable equipment with battery back up.

CXK58257BTM
28 pin TSOP (Plastic)

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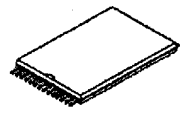
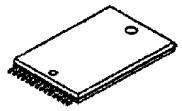
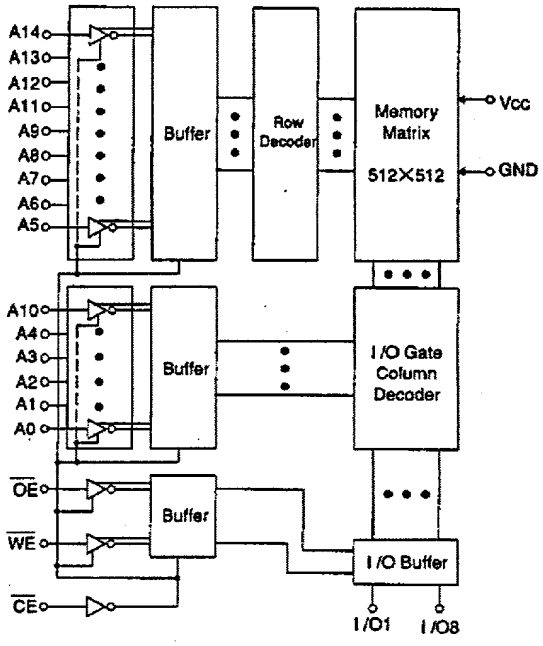




Block Diagram



Features

- Extended operating temperature: −25 to +85°C
- Wide supply voltage operation: 4.5V to 5.5V
- Fast access time:

CXK58257BTM/BYM	(Access time)
−70LLX	70ns (Max.)
−10LLX	100ns (Max.)

- Low power: 10µA (Max.)
- Direct TTL compatible: All inputs and outputs
- Low power data retention current: 6µA (Max.)
- Date retention voltage: 2.0V (Min.)
- Package line-up

  CXK58257BTM/BYM

  8mm × 13.4mm 28 pin TSOP Package

Function

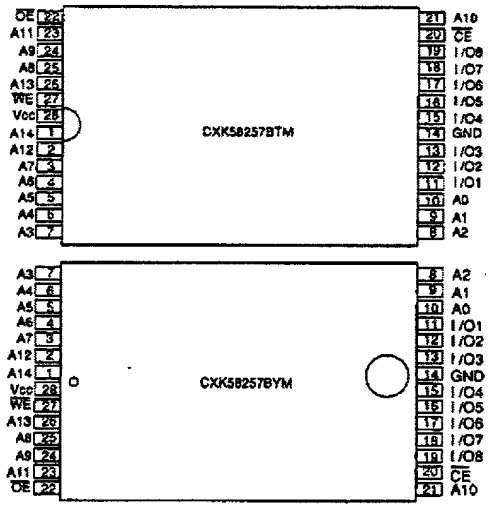
32768-word × 8 bit static RAM

Structure

Silicon gate CMOS IC

E94632-TE

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings (Ta=25°C, GND=0 V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5 to +7.0	V
Input voltage	VIN	−0.5* to Vcc+0.5	
Input and output voltage	VI/O	−0.5* to Vcc+0.5	
Allowable power dissipation	PD	0.7	W
Operating temperature	Topr	−25 to +85	°C
Storage temperature	Tstg	−55 to +150	
Soldering temperature · time	Tsolder	235 · 10	°C · s

*VIN, VI/O=−3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8 pin	Vcc Current
H	×	×	Not selected	High Z	ISB1, ISB2
L	H	H	Output disable	High Z	ICC1, ICC2
L	L	H	Read	Data out	ICC1, ICC2
L	×	L	Write	Data in	ICC1, ICC2

×: "H" or "L"

DC Recommended Operating Conditions (Ta=−25 to +85°C, GND=0 V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	VIH	2.2	—	Vcc+0.3	
Input low voltage	VIL	−0.3*	—	0.8	

*VIL=−3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics (Vcc=5V±10%, GND=0V, Ta=–25 to +85°C)

Item	Symbol	Test Conditions		Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		–0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to Vcc		–0.5	—	0.5	µA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL} V_{IN}=V_{IH} or V_{IL} I_{OUT}=0mA		—	3	10	mA
Average operating current	I_{CC2}	Min. cycle duty=100% I_{OUT}=0mA	70LLX	—	40	60	mA
			10LLX	—	33	60	
Standby current	I_{SB1}	$\overline{CE}$≧Vcc–0.2V	–25 to +85°C	—	—	10	µA
			–25 to +70°C	—	—	5	
			–25 to +40°C	—	—	1	
			+25°C	—	0.2	0.5	
	I_{SB2}	$\overline{CE}$=V_{IH}		—	0.4	2	mA
Output high voltage	V_{OH}	I_{OH}=–1.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V

*1 Vcc=5V, Ta=25°C

I/O capacitance (Ta=25°C, f=1 MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	8	pF

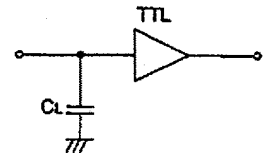
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions (Vcc=5V±10%, Ta=–25 to +85°C)

Item	* Conditions
Input pulse high level	V_{IH}=2.4V
Input pulse low level	V_{IL}=0.6V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	C_L*=100pF, 1TTL

• **Test circuit**



* C_L includes scope and jig capacitances.

• Read cycle ($\overline{WE}$="H")

Item	Symbol	-70LLX		-10LLX		Unit
		Min.	Max.	Miin.	Max.	
Read cycle time	tRC	70	—	100	—	ns
Address access time	tAA	—	70	—	100	
Chip enable access time	tCO	—	70	—	100	
Output enable to output valid	tOE	—	40	—	50	
Output hold from address change	tOH	10	—	10	—	
Chip enable to output in low Z ($\overline{CE}$)	tLZ	10	—	10	—	
Output enable to output in low Z ($\overline{OE}$)	tOLZ	5	—	5	—	
Chip disable to output in high Z ($\overline{CE}$)	tHZ*	—	25	—	30	
Output disable to output in high Z ($\overline{OE}$)	tOHZ*	—	25	—	30	

* tHZ and tOHZ are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

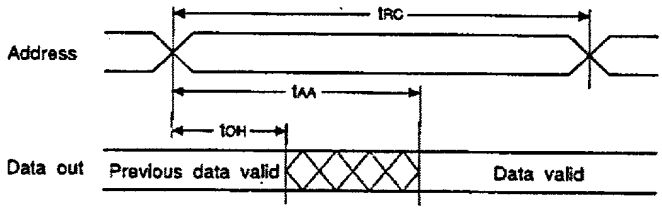
• Write cycle

Item	Symbol	-70LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	tWC	70	—	100	—	ns
Address valid to end of write	tAW	60	—	70	—	
Chip enable to end of write	tCW	60	—	70	—	
Data to write time overlap	tDW	30	—	35	—	
Data hold from write time	tDH	0	—	0	—	
Write pulse width	tWP	50	—	60	—	
Address setup time	tAS	0	—	0	—	
Write recovery time ($\overline{WE}$)	tWR	5	—	5	—	
Write recovery time ($\overline{CE}$)	tWR1	0	—	0	—	
Output active from end of write	tOW	10	—	10	—	
Write to output in high Z	tWHZ*	—	25	—	25	

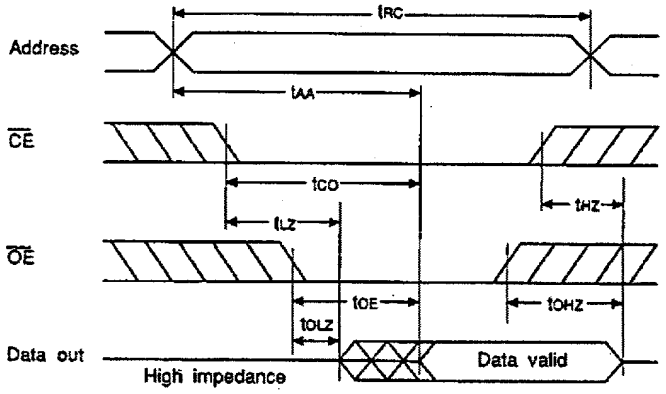
* tWHZ is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

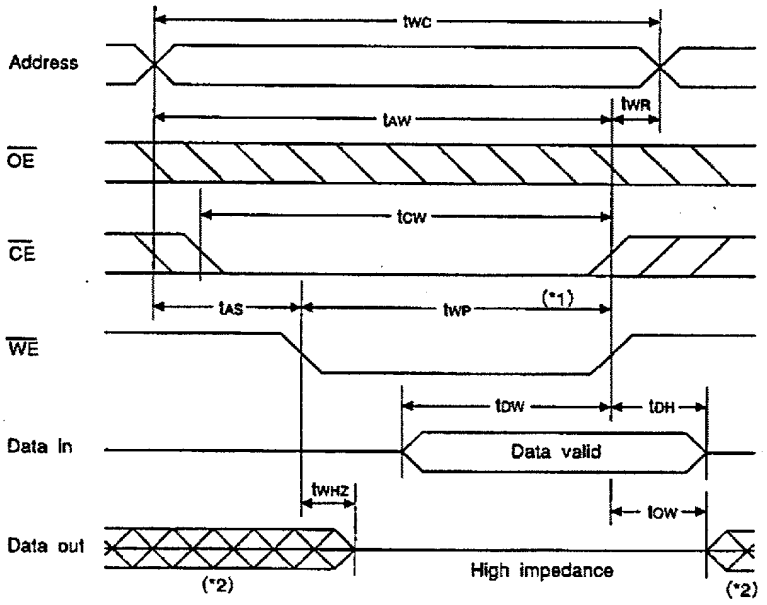
• Read cycle (1): $\overline{CE}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH



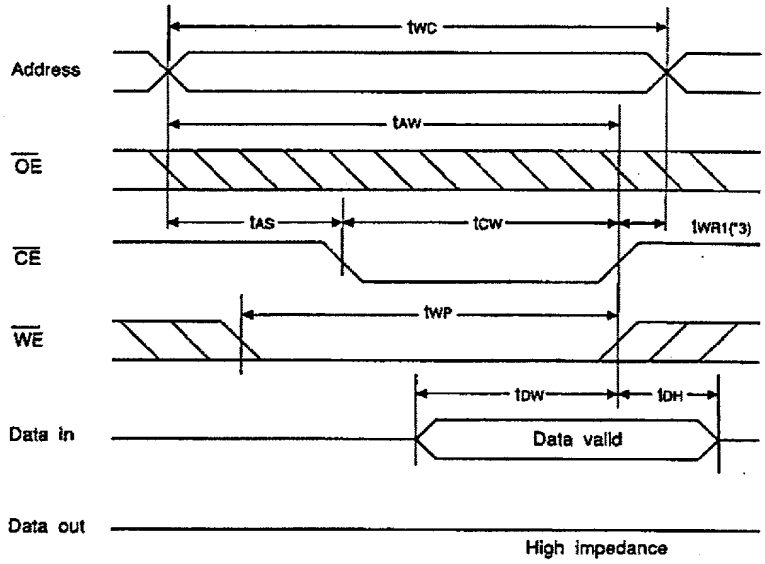
• Read cycle (2): $\overline{WE}$=VIH



• Write cycle (1): $\overline{WE}$ control



• Write cycle (2): $\overline{CE}$ control



Note)

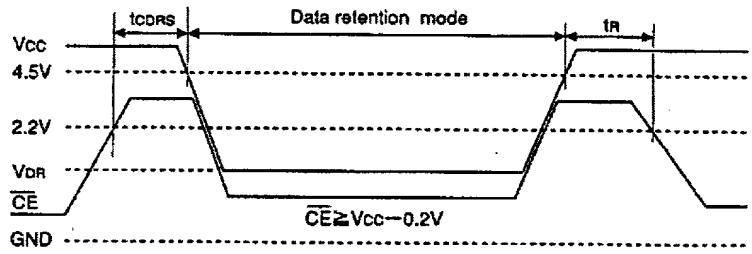
*1 Write is executed when both $\overline{CE}$ and $\overline{WE}$ are at low simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

*3 t_{WR1} is tested from the rising edge of $\overline{CE}$, until the end of the write cycle.

Data retention waveform

• Low supply voltage data retention waveform



Data Retention Characteristics (Ta=−25 to +85°C)

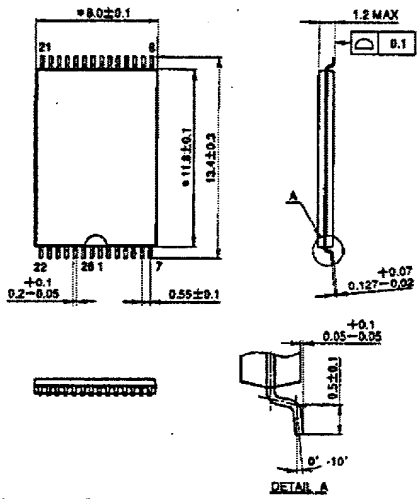
Item	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	CE≧Vcc−0.2		2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0 V CE≧2.8	−25 to +85°C	—	—	6	µA
			−25 to +70°C	—	—	3	
			−25 to +40°C	—	—	0.6	
			+25°C	—	0.1	0.3	
	I_{CCDR2}	Vcc=2.0 to 5.5V CE≧Vcc−0.2V		—	0.2*	10	
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t_R			5	—	—	ms

* Vcc=5V, Ta=25°C

Package Outline Unit : mm

CXK58257BTM

28PIN TSOP (Plastic)



NOTE>Dimension "*" does not include mold protrusion.

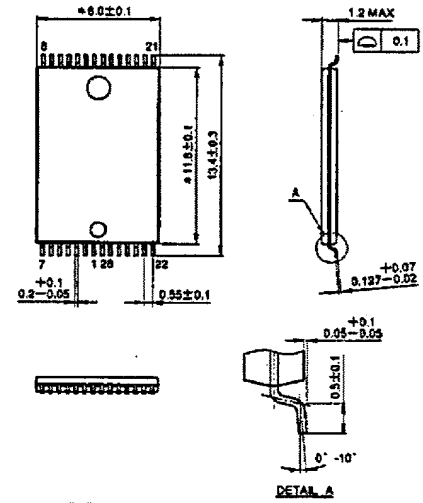
SONY CODE	TSOP-28P-L01
EIAJ CODE	TSOP028-P-0000-A
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

CXK58257BYM

28PIN TSOP (Plastic)



NOTE>Dimension "*" does not include mold protrusion.

SONY CODE	TSOP-28P-L01R
EIAJ CODE	TSOP028-P-0000-B
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g