

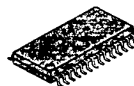
SONY**CXK58267AM**-70L/85L/10L/12L
-70LL/85LL/10LL/12LL**32768-word × 8-bit High Speed CMOS Static RAM****Description**

CXK58267AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. The CXK58267AM's two chip enable inputs are useful for battery back up operation for nonvolatility.

Features

- Fast access time: (Access time)
CXK58267AM-70L,70LL 70ns (Max.)
CXK58267AM-85L,85LL 85ns (Max.)
CXK58267AM-10L,10LL 100ns (Max.)
CXK58267AM-12L,12LL 120ns (Max.)
- Low power operation:
CXK58267AM-70LL,85LL,10LL,12LL;
Standby : 1 μ W (Typ.)
Operation : 15mW (Typ.)
CXK58267AM-70L,85L,10L,12L;
Standby : 2.5 μ W (Typ.)
Operation : 15mW (Typ.)
- Single +5V supply: +5V $\pm$ 10%
- Fully static memory...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 450mil SOP

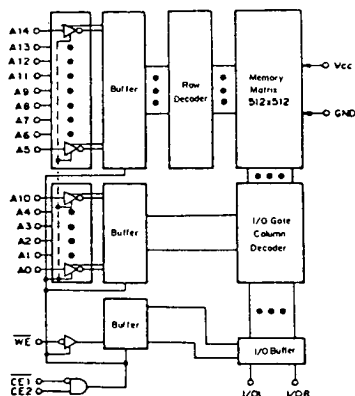
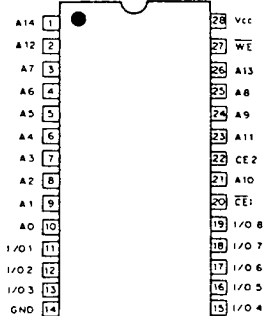
28 pin SOP (Plastic)

**Function**

32768-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

5**Block Diagram****Pin Configuration**
(Top View)**Pin Description**

Symbol	Description
A0 to A14	Address input
I/O 1 to I/O 8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
Vcc	+5V power supply
GND	Ground

E90523A22 - ST

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions		-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		-0.5	—	0.5	-0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE1}=V_{IH}$ or $CE2=V_{IL}$ or $\overline{WE}=V_{IL}$, V _{I/O} =GND to V _{CC}		-0.5	—	0.5	-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	$\overline{CE1}=V_{IL}$, $CE2=V_{IH}$, I _{OUT} =0mA		—	3	10	—	3	10	mA
		$\overline{CE1}=0.2V$, $CE2=V_{CC}-0.2V$ V _{IN} =0.2V or V _{CC} -0.2V		—	1	5	—	1	5	
Average operating current	I _{CC2}	Min. cycle Duty=100%, I _{OUT} =0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I _{SB1}	$CE2 \leq 0.2V$ or $\left(\overline{CE1} \geq V_{CC}-0.2V \right.$ $\left. CE2 \geq V_{CC}-0.2V \right)$	0 to 70 °C	—	—	25	—	—	5	μA
			0 to 40 °C	—	—	5	—	—	1	
			25 °C	—	0.5	2	—	0.2	0.5	
		I _{SB2}	$CE2=V_{IL}$, or $\overline{CE1}=V_{IH}$	—	0.6	3	—	0.6	3	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

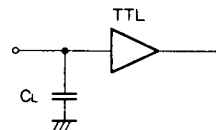
(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics**● AC test conditions**(V_{CC}=5V ± 10%, T_a=0 to +70 °C)

Item		Conditions
Input pulse high level		V _{IH} =2.2V
Input pulse low level		V _{IL} =0.8V
Input rise time		t _r =5ns
Input fall time		t _f =5ns
Input and output reference level		1.5V
Output load conditions	85L/85LL/10L/10LL/12L/12LL	C _L * =100pF, 1TTL
	70L/70LL	C _L * =30pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	– 70L/70LL		– 85L/85LL		– 10L/10LL		– 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time (CE1, CE2)	t _{CO1} , t _{CO2}	—	70	—	85	—	100	—	120	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	0	30	0	30	0	30	0	30	ns

* t_{HZ1} and t_{HZ2} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

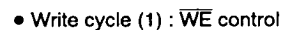
• Write cycle

Item	Symbol	– 70L/70LL		– 85L/85LL		– 10L/10LL		– 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

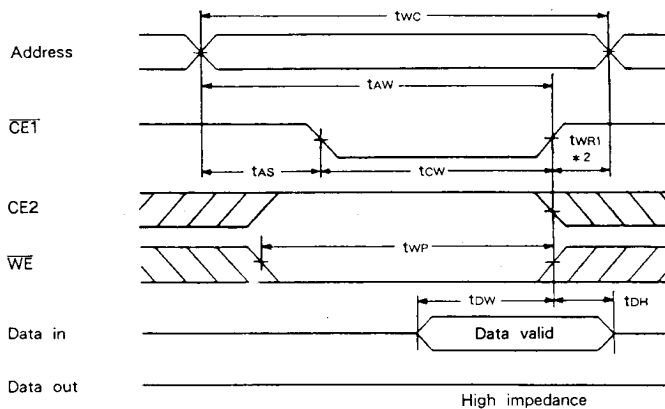
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

- Read cycle (1) : $\overline{CE1}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$

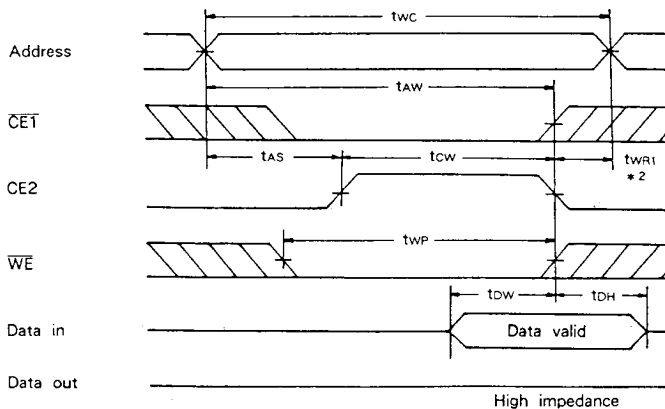
- Read cycle (1) : $\overline{CE1}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



- *1. A write occurs during the period of $\overline{CE1}$ and $\overline{WE}$ being low and CE2 being high.
- *2. t_{WR1} is measured from the earlier of $\overline{CE1}$ or $\overline{WE}$ going high and CE2 going low to the end of write cycle.
- *3. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

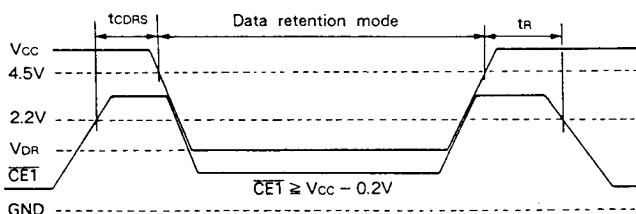
(Ta=0 to 70 °C)

Item	Symbol	Test conditions		- 70L/85L/10L/12L			- 70LL/85LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	* 1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V * 1	0 to 70 °C	—	—	10	—	—	3	μA
			0 to 40 °C	—	—	2	—	—	0.6	
			25 °C	—	0.25	1	—	0.1	0.3	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V * 1		—	0.5	25	—	0.2	5	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} * 2	—	—	t _{RC} * 2	—	—	ns

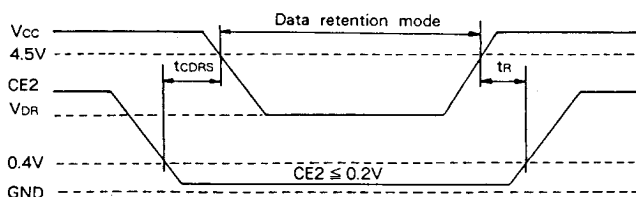
* 1. $\overline{CE1} \geq V_{CC}-0.2V$, $CE2 \geq V_{CC}-0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)* 2. t_{RC}: Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

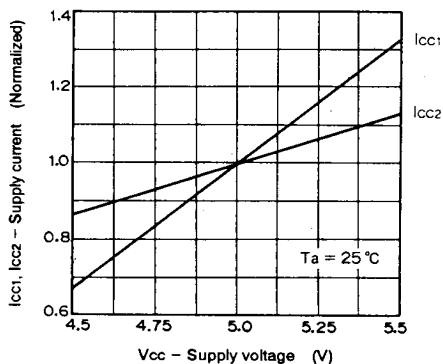


- Low supply voltage data retention waveform (2) ($CE2$ control)

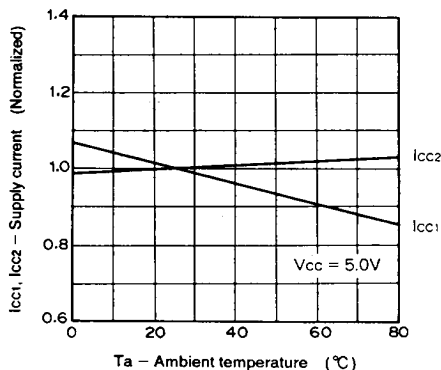


Example of Representative Characteristics

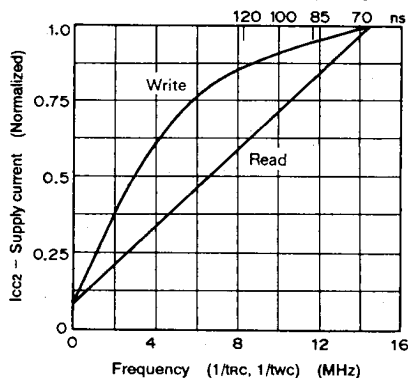
Supply current vs. Supply voltage



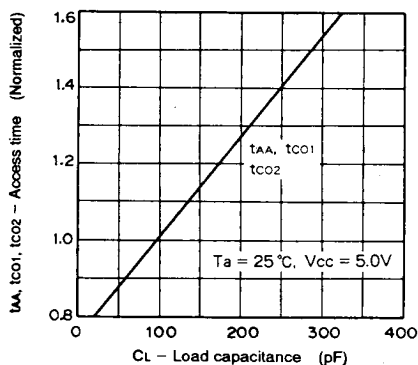
Supply current vs. Ambient temperature



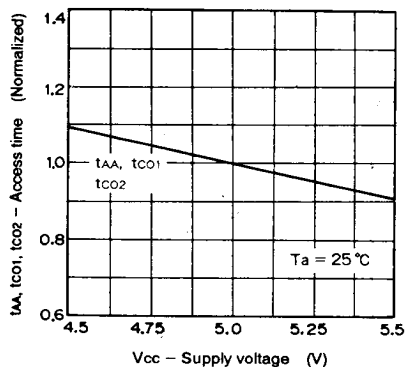
Supply current vs. Frequency



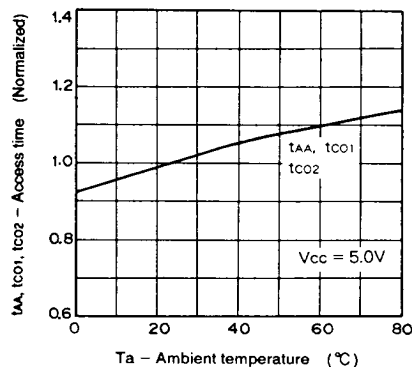
Access time vs. Load capacitance



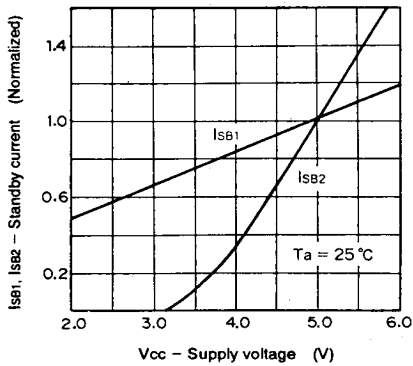
Access time vs. Supply voltage



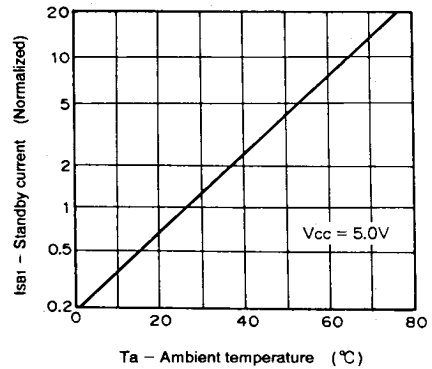
Access time vs. Ambient temperature



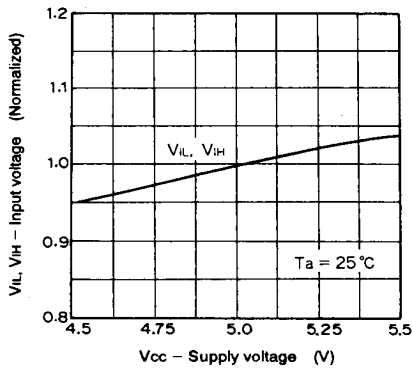
Standby current vs. Supply voltage



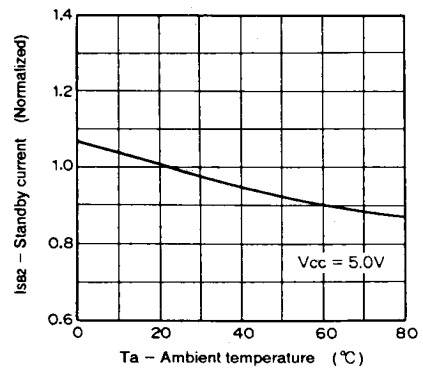
Standby current vs. Ambient temperature



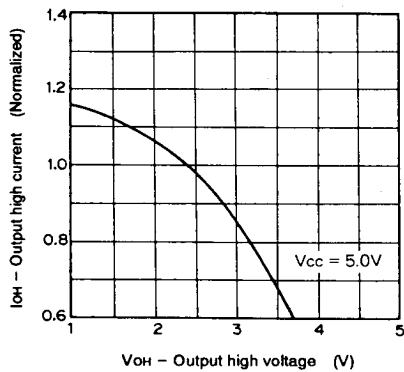
Input voltage level vs. Supply voltage



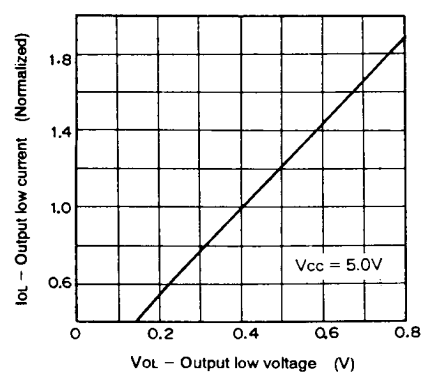
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



Package Outline Unit : mm

