SONY

CXK584000TM/YM/M/P -55L/70L/10L -55LL/70LL/10LL

524288-word × 8-bit High Speed CMOS Static RAM

Description

CXK584000TM/YM/M/P is a 4,194,304 bits high speed CMOS static RAM organized as 524288-word by 8-bits. Polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

This asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

- Fast access time: (Access time)
  - CXK584000TM/YM/M/P-55L/55LL 55ns (Max.)
  - CXK584000TM/YM/M/P-70L/70LL 70ns (Max.)
  - CXK584000TM/YM/M/P-10L/10LL 100ns (Max.)
- Low stand-by current:
  - CXK584000TM/YM/M/P
    - -55L/70L/10L 100µA (Max.)
    - -55LL/70LL/10LL 50µA (Max.)
- Low data retention current: (Ta = 0 to +40°C)
  - CXK584000TM/YM/M/P
    - -55L/70L/10L; 15µA (Max.)
    - -55LL/70LL/10LL; 3µA (Max.)
- Single +5V supply: +5V ± 0.5V
- Low power data retention: 2.0V (Min.)
- Package line-up
  - CXK584000TM/YM 400mil 32 pin TSOP (Type II)
  - CXK584000M 525mil 32 pin SOP
  - CXK584000P 600mil 32 pin DIP

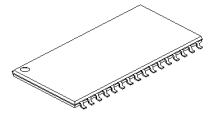
Function

524288-word × 8-bit static RAM

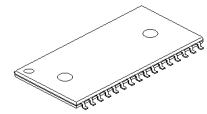
Structure

Silicon gate CMOS IC

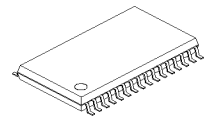
CXK584000TM
32 pin TSOP (Plastic)



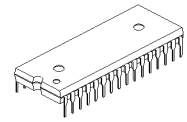
CXK584000YM
32 pin TSOP (Plastic)



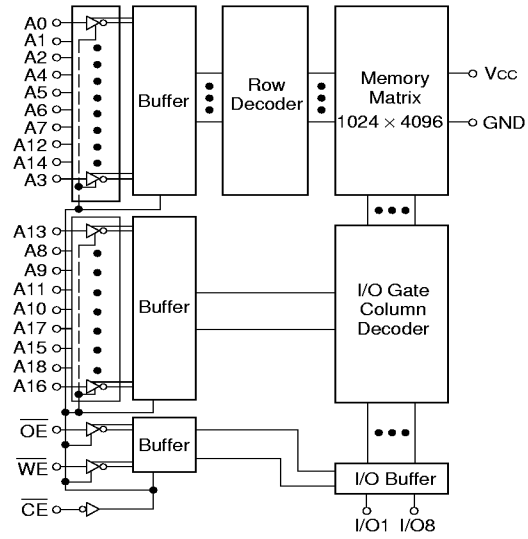
CXK584000M
32 pin SOP (Plastic)



CXK584000P
32 pin DIP (Plastic)



Block Diagram



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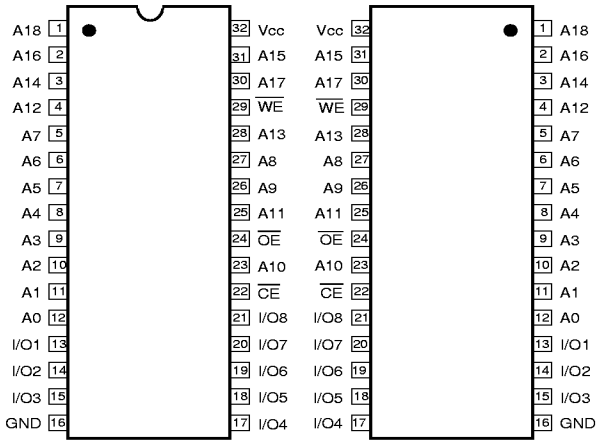
E91785C5Z-PS

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A18	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{CC}	+5V Power supply
GND	Ground

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		–0.5 to +7.0	V
Input voltage	V_{IN}		–0.5*1 to V_{CC} + 0.5	V
output voltage	$V_{I/O}$		–0.5*1 to V_{CC} + 0.5	V
Allowable power dissipation	P_D	CXK584000TM/YM/M	0.7	W
		CXK584000P	1.0	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		–55 to +150	°C
Soldering temperature · time	Tsolder	CXK584000TM/YM	235 · 10	°C · s
		CXK584000M/P	260 · 10	

*1 V_{IN}, $V_{I/O}$ = –3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	V_{CC} current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3*1	—	0.8	V

*1 V_{IL} = –3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• **DC characteristics** (V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions			Min.	Typ.*1	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}			–1	—	1	µA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = GND to V_{CC}			–1	—	1	µA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA			—	6	15	mA
Average operating current	I_{CC2}	Min. Cycle, Duty = 100%, I_{OUT} = 0mA			—	60	100	mA
	I_{CC3}	Cycle time 1µs, Duty = 100%, I_{OUT} = 0mA, $\overline{CE}$ ≤ 0.2V, V_{IL} ≤ 0.2V, V_{IH} ≥ Vcc – 0.2V			—	10	20	mA
Standby current	I_{SB1}	$\overline{CE}$ ≥ Vcc – 0.2V	L*2	0 to +70°C	—	—	100	µA
				0 to +40°C	—	—	35	
				+25°C	—	2	—	
			LL*3	0 to +70°C	—	—	50	
				0 to +40°C	—	—	18	
				+25°C	—	2	—	
	I_{SB2}	$\overline{CE}$ = V_{IH}			—	0.3	3	mA
Output high voltage	V_{OH}	I_{OUT} = –1.0mA			2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA			—	—	0.4	V

*1 V_{CC} = 5V, Ta = 25°C

*2 Guaranteed for L-version (-55L/70L/10L)

*3 Guaranteed for LL-version (-55LL/70LL/10LL)

I/O Capacitance (Ta = 25°C, f = 1MHz)

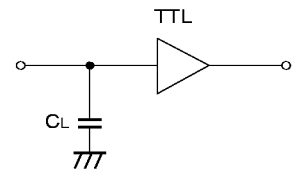
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC test conditions** (Vcc = 5V ± 0.5V, Ta = 0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH} = 2.2V
Input pulse low level		V_{IL} = 0.8V
Input rise time		tr = 5ns
Input fall time		tf = 5ns
Input and output reference level		1.5V
Output load conditions	-70L/70LL -10L/10LL	C_L*1 = 100pF, 1TTL
	-55L/55LL	C_L*1 = 30pF, 1TTL



*1 C_L includes scope and jig capacitances.

• **Read cycle ($\overline{WE}$ = "H")**

Item	Symbol	-55L/55LL		-70L/70LL		-10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	55	—	70	—	100	—	ns
Address access time	t_{AA}	—	55	—	70	—	100	ns
Chip enable access time	t_{CO}	—	55	—	70	—	100	ns
Output enable to output valid	t_{OE}	—	30	—	40	—	50	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*1	0	20	0	25	0	35	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*1	0	20	0	25	0	35	ns

*1 t_{HZ} and t_{OHZ} are defined as the time requied for outputs to turn to high impedance state and are not referred to as output voltage levels.

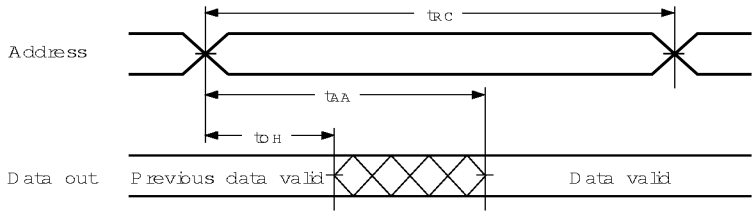
• **Write cycle**

Item	Symbol	-55L/55LL		-70L/70LL		-10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	55	—	70	—	100	—	ns
Address valid to end of write	t_{AW}	50	—	60	—	80	—	ns
Chip enable to end of write	t_{CW}	50	—	60	—	80	—	ns
Data to write time overlap	t_{DW}	25	—	30	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	40	—	50	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*2	0	20	0	25	0	30	ns

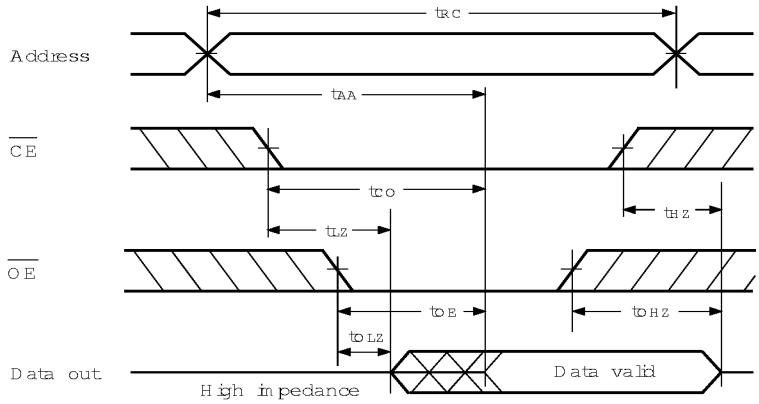
*2 t_{WHZ} is defined as the time requied for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

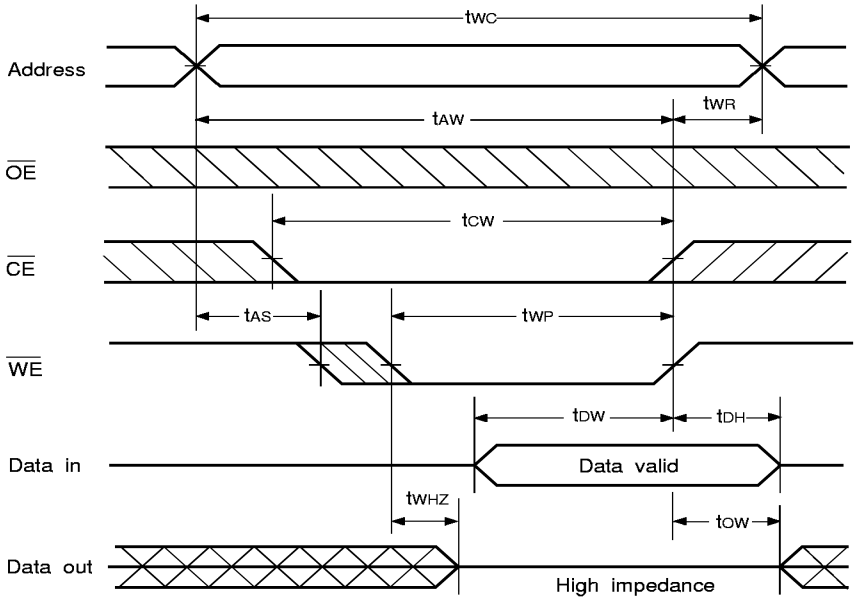
• **Read cycle (1)** : $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}



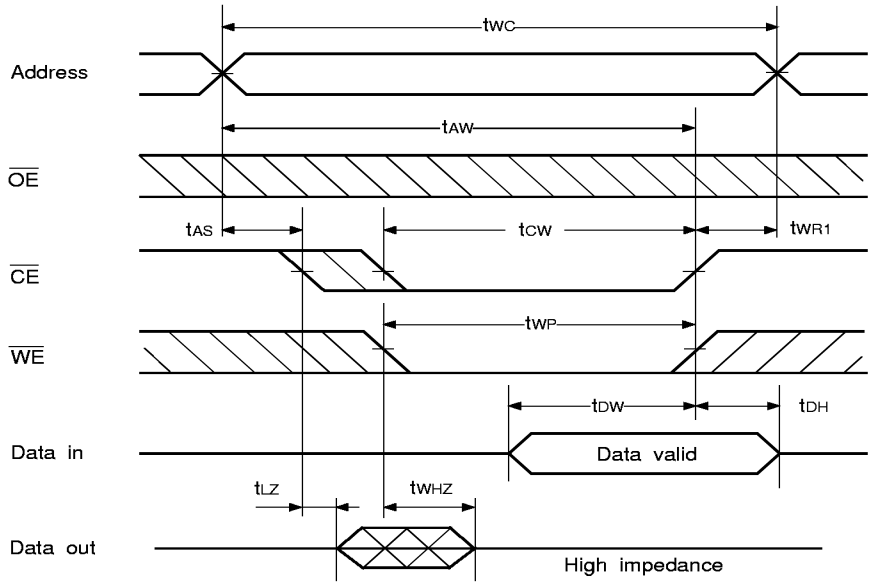
• **Read cycle (2)** : $\overline{WE}$ = V_{IH}



• **Write cycle (1)** : $\overline{WE}$ control



• **Write cycle (2)** : $\overline{CE}$ control

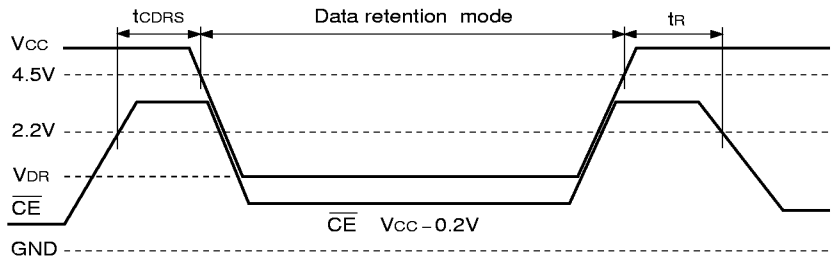


Note) During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics (Ta = 0 to +70°C)

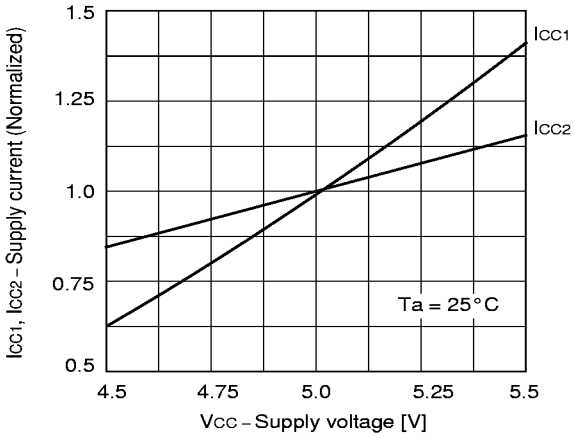
Item	Symbol	Test conditions		-55L/70L/10L			-55LL/70LL/10LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geq Vcc - 0.2V$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc = 3.0V, $\overline{CE} \geq 2.8V$	0 to +70°C	—	—	50	—	—	15	µA
			0 to +40°C	—	—	15	—	—	3	
			+25°C	—	1	—	—	0.5	—	
	I_{CCDR2}	Vcc = 2.0 to 5.5V, $\overline{CE} \geq Vcc - 0.2V$		—	2	100	—	2	50	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			5	—	—	5	—	—	ms

Data retention waveform

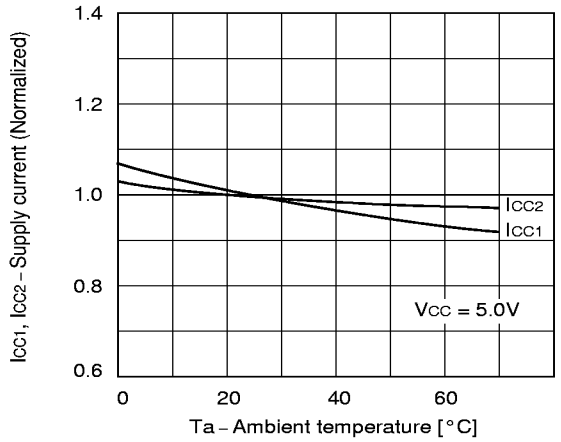


Example of Representative Characteristics

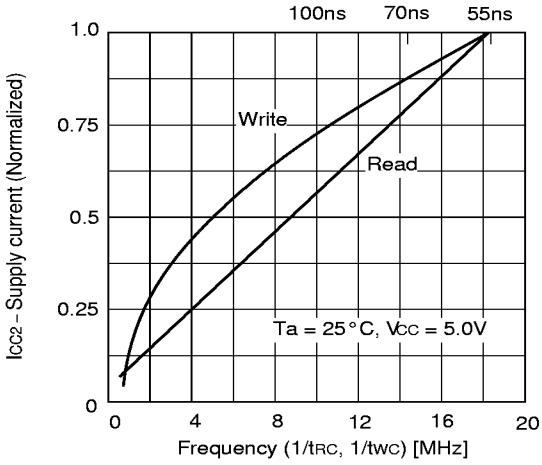
Supply current vs. Supply voltage



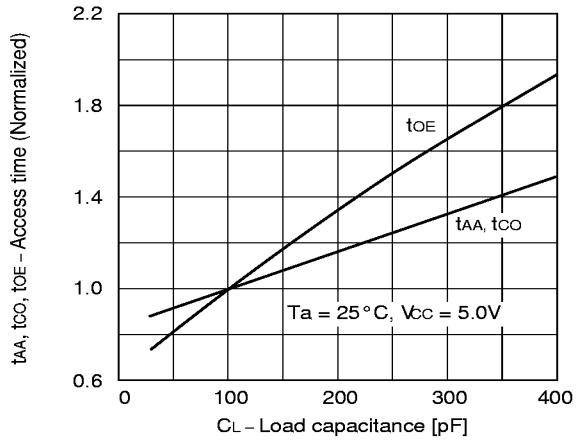
Supply current vs. Ambient temperature



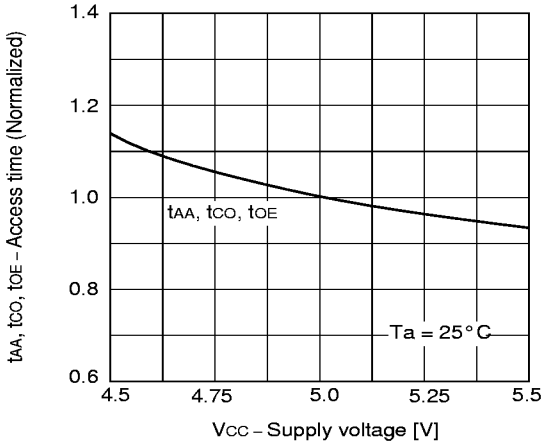
Supply current vs. Frequency



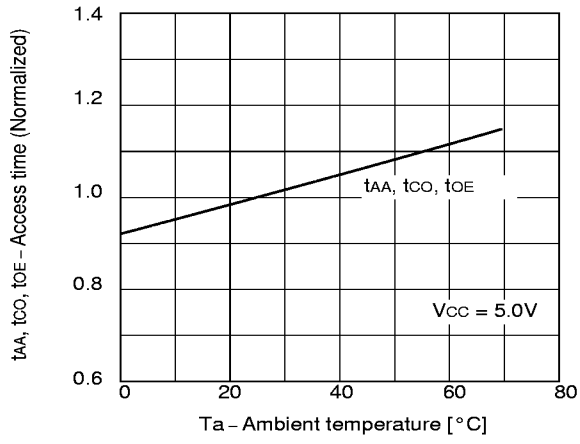
Access time vs. Load capacitance



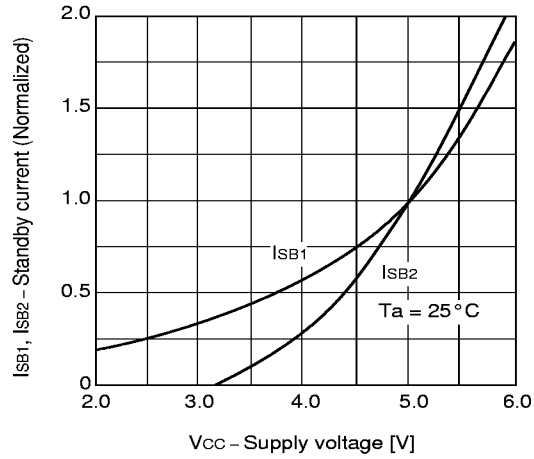
Access time vs. Supply voltage



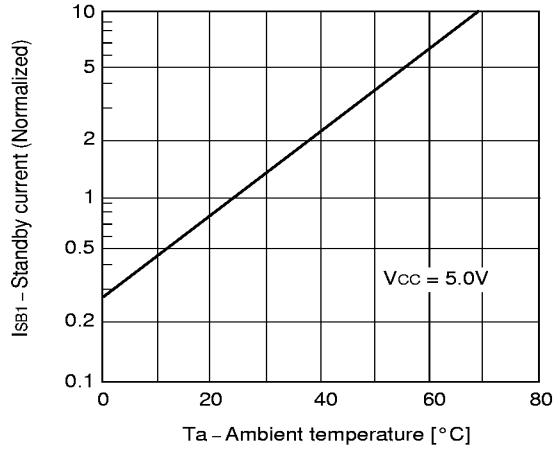
Access time vs. Ambient temperature



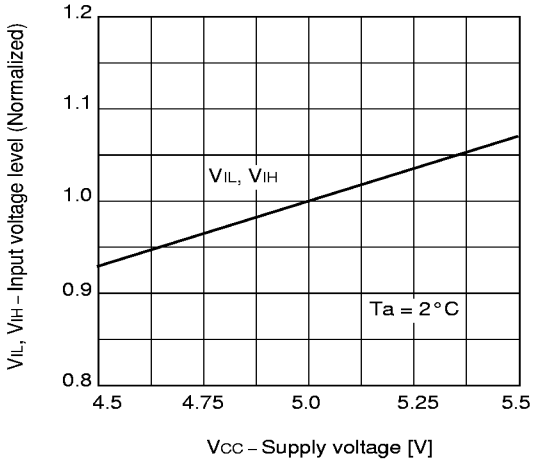
Standby current vs. Supply voltage



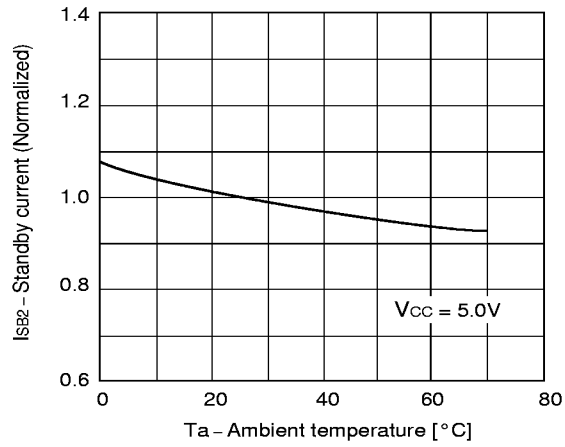
Standby current vs. Ambient temperature



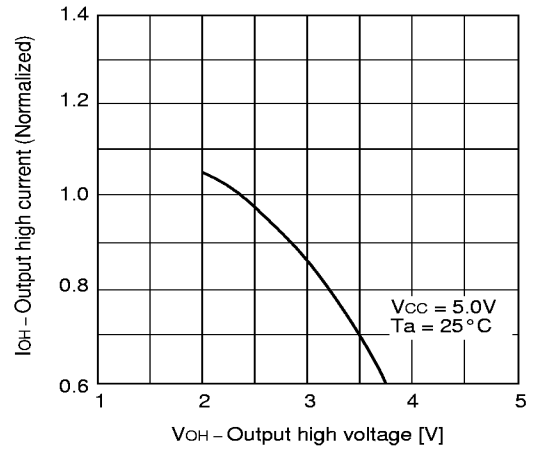
Input voltage level vs. Supply voltage



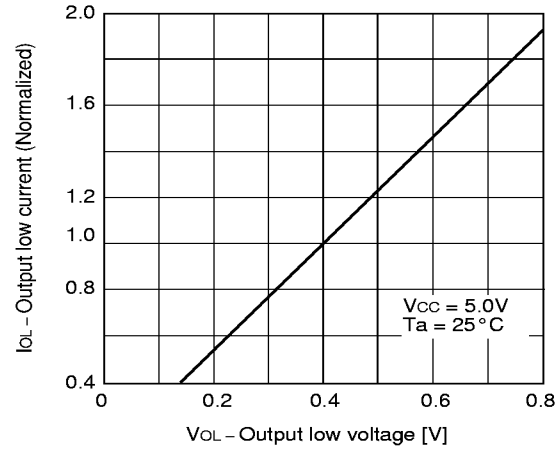
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



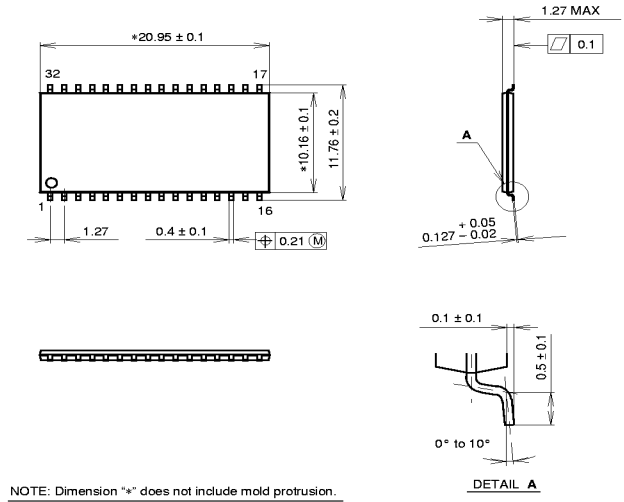
Output low current vs. Output low voltage



Package Outline Unit: mm

CXK584000TM

32PIN TSOP (II) (PLASTIC) 400mil



NOTE: Dimension "*" does not include mold protrusion.

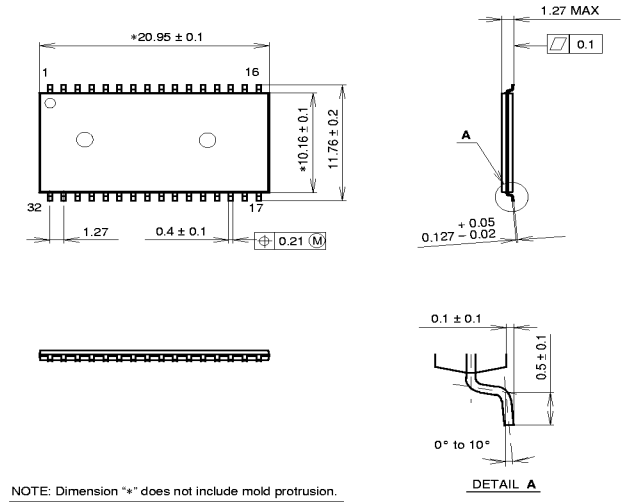
PACKAGE STRUCTURE

SONY CODE	TSOP (II) -32P-L01
EIAJ CODE	TSOP (II) 032-P-0400-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————

CXK584000YM

32PIN TSOP (II) (PLASTIC) 400mil



NOTE: Dimension "*" does not include mold protrusion.

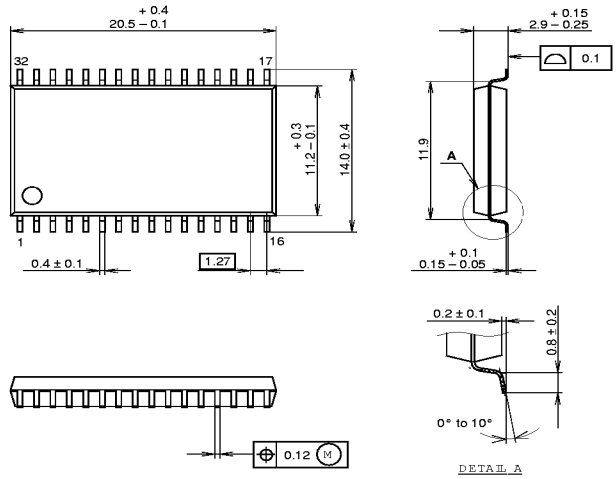
PACKAGE STRUCTURE

SONY CODE	TSOP (II) -32P-L01R
EIAJ CODE	TSOP (II) 032-P-0400-B
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	————

CXK584000M

32PIN SOP (PLASTIC)



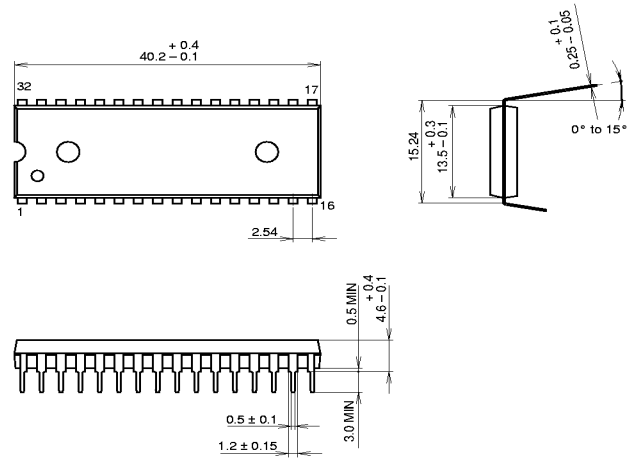
PACKAGE STRUCTURE

SONY CODE	SOP-32P-L02
EIAJ CODE	SOP032-P-0525
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.2g

CXK584000P

32PIN DIP (PLASTIC) 600mil



PACKAGE STRUCTURE

SONY CODE	DIP-32P-01
EIAJ CODE	*DIP32-P-0600-A
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	4.5g