VME 4000

VMEbus
Interrupt Handler

January 1990

Distinctive Features

- **Provides random logic and open collector drive for VMEbus interrupt handling in 300 mil 24 pin DIP or 28 pin LCC**
- **Monitors all seven interrupt levels**
- **Includes IACK-daisy chain driver for slot 1 configurations**
- **Directly drives open collector IACK* signal**
- **Works with PLX VME 1200 Master Controller or any other master controller that meets IEEE 1014**
- **Input hysteresis filters bus noise eliminating need for external buffers**
- **Available in Commercial, Industrial and Military temperature ranges**

Programmable Version Available

If the VME 4000 does not match the requirements of the design, a programmable version is available (the PLX 448 or 464) which allows the user to customize all inputs, outputs and logic. Programming is performed using industry standard tools such as ABEL™ or CUPL™ software and commonly available PLD programming hardware. Contact PLX for a data sheet on the PLX 448, 464 and other information.

Applications

- **Interrupt handler logic for VMEbus interrupts on master modules**

General Description

The VME 4000 is a CMOS seven level interrupt handler for VMEbus interrupts which is packaged in a compact 300 mil wide DIP or 28 pin LCC. The VME 4000 meets the VMEbus IEEE 1014 timing and electrical requirements.

The VME 4000 will generate an interrupt request to the local master (via a local interrupt handler) when any of its seven VMEbus interrupt requests inputs is asserted. Once the master generates an interrupt acknowledge back to the VME 4000, it participates in a VMEbus interrupt acknowledge cycle by driving the appropriate interrupt level code onto the addresss bus as well as asserting IACK* on the bus.

If the VME 4000 is configured to be a slot 1 interrupt handler, it can provide the IACK-daisy chain driver function. The assertion of IACK* on the bus will cause the VME 4000 to drive IACKOUT* during the interrupt acknowledge cycle.

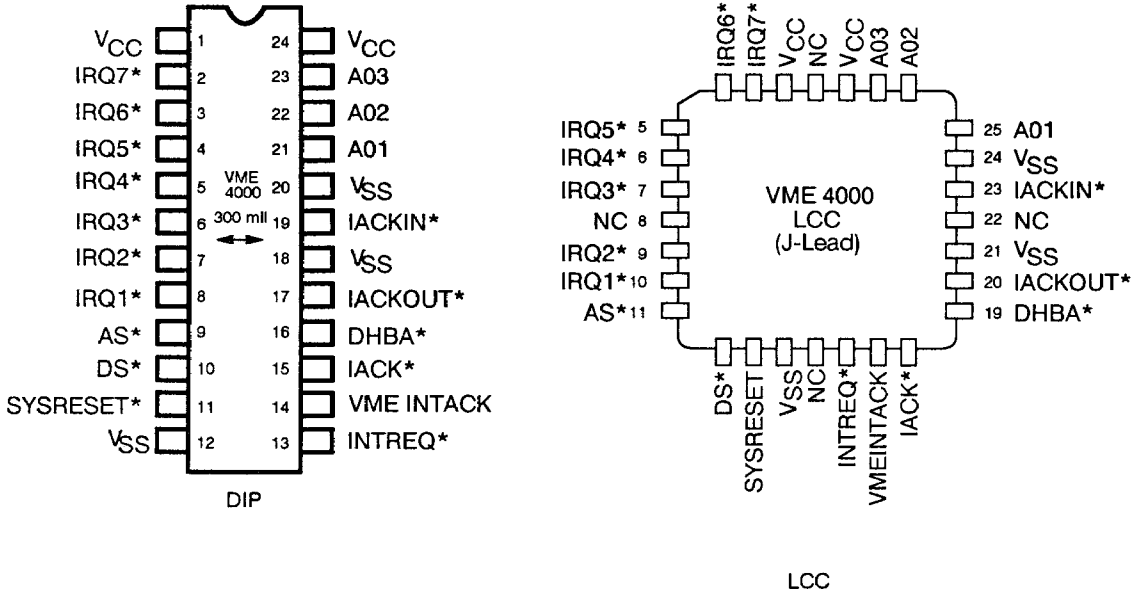

Figure 1. Pinout of VME 4000

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Pin Description

28-Pin LCC	24-Pin DIP	Signal	Type	Function
3	2	IRQ7*	I	Active low; VMEbus Interrupt Request level 7.
4	3	IRQ6*	I	Active low; VMEbus Interrupt Request level 6.
5	4	IRQ5*	I	Active low; VMEbus Interrupt Request level 5.
6	5	IRQ4*	I	Active low; VMEbus Interrupt Request level 4.
7	6	IRQ3*	I	Active low; VMEbus Interrupt Request level 3.
9	7	IRQ2*	I	Active low; VMEbus Interrupt Request level 2.
10	8	IRQ1*	I	Active low; VMEbus Interrupt Request level 1.
11	9	AS*	I	Active low; VMEbus Address Strobe. Used in slot 1 IACK-daisy chain configurations only, otherwise should be tied high.
12	10	DS*	I	Active low; Logical AND of VMEbus Data Strobe DS0* and DS1*. Used in slot 1 IACK-daisy chain configurations only, otherwise should be tied high.
13	11	SYSRESET*	I	Active low; VMEbus system reset.
14, 21,24	12, 18,20	V_{SS}		Chip Ground
16	13	INTREQ*	O	Active low, open collector, VMEbus interrupt request to local master (local interrupt)
17	14	VMEINTACK	I	Active high; VMEbus interrupt acknowledge from local master (IPL decode logic) to VME 4000.
18	15	IACK*	O	Active Low, open collector; Interrupt Acknowledge. Indi cates interrupt acknowledge cycle occurring on VME bus.
19	16	DHBA*	I	Active Low; Device has bus address. Indicates local master has control of the VME address bus.
20	17	IACKOUT*	O	Active low; Interrupt Acknowledge Out. IACK-daisy chain driver output. Used in slot 1 configurations only, otherwise should be left un-connected.
23	19	IACKIN*	I	Active low; Interrupt Acknowledge In. Input to IACK-daisy chain driver. Used in slot 1 configurations only, otherwise should be tied high.
25	21	A01	O	Active high; Local master's address bus bit 1.
26	22	A02	O	Active high; Local master's address bus bit 2.
27	23	A03	O	Active high; Local master's address bus bit 3.
2, 28	1,24	V_{CC}	–	+5 V Chip Power
1, 8, 15,22	–	NC	–	No Connect

Note: TS is Tri-state
OC is Open Collector

Detailed Description

The VME 4000 generates a local interrupt request (INTREQ*) to the local master or local interrupt handler when any of the VMebus interrupt request (IRQ1* – IRQ7*) is asserted. When the local master acknowledges the interrupt, the VME 4000 drives the necessary interrupt priority level and IACK* signals on the bus during the VMEbus interrupt acknowledge cycle. The interrupter that caused the highest priority interrupt will respond with the interrupt vector and terminate the cycle by

asserting DTACK* . In addition to interrupt handling, the VME 4000 provides the IACK-daisy chain driver functionality required in slot 1 configurations. The VME 4000 can interface directly with the VME 1200 Master Controller chipset to provide a complete VME interface. However, this is not required, as the VME 4000 will interface to any master controller that meets the IEEE 1014 specification.

Centralized Interrupt Handling Systems

When configured in a centralized interrupt handling system, a single VME 4000 can handle all seven interrupt levels on the VME bus. When any VME bus interrupt is asserted, the VME 4000 asserts a local interrupt request (INTREQ*) to the local master. Since the VME 4000 leaves handling of the local interrupts to the board designer, the VME 4000's INTREQ* output would typically become an interrupt input to the master's local interrupt handler such as an 8259 or 9519. The local interrupt handler would then generate the appropriate IPL (Interrupt Priority Level) code to the CPU corresponding to the VME 4000's assigned local interrupt level.

When the CPU receives the interrupt (via the IPL code) and determines it should service it, it will initiate a local interrupt acknowledge cycle. The local IPL decoder logic should determine if the CPU is acknowledging the VME 4000's interrupt level or another higher priority local interrupt. If the CPU is acknowledging the VME 4000's interrupt request, the IPL decode logic should assert the VMEINTACK input to the VME 4000. If the CPU is acknowledging a higher priority local interrupt, the IPL decoder logic should select the local interrupt handler to participate in the interrupt acknowledge cycle. In this case, the VME 4000 will continue to asserts its interrupt request (INTREQ*) until the CPU acknowledges it (asserting VMEINTACK). The assertion of VMEINTACK causes the VME 4000 to prepare for an interrupt acknowledge cycle on the bus. At this point the VME 4000 freezes all VME interrupt request inputs (IRQ1* - IRQ7*) and prioritizes them to determine which is the highest priority interrupt. This level will be driven on to the address output pins (A01 - A03). Note that this part of the address bus must be isolated from the CPU's address bus during the interrupt acknowledge cycle since the CPU is driving its local interrupt acknowledge IPL code on the address bus during this time. This can be accomplished by enabling the A1 - A3 address bits out of the VME 4000 onto the VME bus when DHBA* is asserted and VMEINTACK is asserted. Otherwise, the local A1 - A3 address bits can be enabled whenever DHBA* is asserted and VMEINTACK is not asserted.

Once the local VMEbus master controller gains control of the address bus, as indicated by the assertion of the DHBA* input, the VME 4000 will assert the IACK* signal indicating an interrupt acknowledge cycle is occurring on the bus. At this time, the address output pins A01 - A03 should be driven onto the VME bus. Also, at this time, the VME 4000 will de-assert the INTREQ* output. The IACK-daisy chain driver located in slot 1 will see IACK* asserted and assert its IACKOUT* signal. This starts the IACK daisy chain signal. Each interrupter compares its interrupt request level to the interrupt priority level on address bit 1-3. If the levels match, the interrupter is selected to respond to the interrupt acknowledge cycle. If not, the interrupter must pass its IACKIN* input to its IACKOUT* output continuing the daisy chain.

The selected interrupter places its interrupter vector (STATUS/ID vector) on the data bus and asserts DTACK* to terminate the cycle. The vector is returned to the local master's CPU and DHBA* and VMEINTACK are de-asserted. This causes IACK* to be de-asserted and the address pin outputs to be driven to high impedance, ending the interrupt acknowledge cycle. At this point the CPU will use the received vector to call the appropriate interrupt handling routine.

The VME 4000 supports Release On AKnowledge (ROAK) interrupters, which should release their interrupt request at the end of the interrupt acknowledge cycle. Release On Register Access (RORA) interrupters can be supported through modifications. Check with the factory if this functionality is required.

Multiple Interrupts at the Same Time

If multiple interrupt occur between the time the first interrupt request comes in and the time the VMEINTACK input is asserted, the VME 4000 will acknowledge the highest priority interrupt request first. When the interrupt acknowledge cycle for that interrupt request is done, the VME 4000 will immediately assert INTREQ* again in accordance with the next highest priority interrupt request. Additional interrupt requests and acknowledge cycles will occur until all interrupt request have been processed. The VME 4000 does not sample interrupt request during the time IACK* is asserted.

Distributed Interrupt Handling Systems

In multi-master systems where distributed interrupt handling is desired, the VME 4000 can provide support. A VME 4000 should be installed on each master that will handle VME bus interrupts. Those interrupts that each master will not handle should have their corresponding interrupt request inputs to the VME 4000 tied high. For example, suppose the system supports two masters where master 1 responds to interrupt level 1 through 4 and master 2 responds the interrupt levels 5 through 7. Master 1 should connect IRQ1* through IRQ4* inputs on its VME 4000 to the corresponding signals on the VME bus. It should also tie IRQ5* through IRQ7* inputs on its VME 4000 high. Master 2 should connect IRQ5* through IRQ7* inputs on its VME 4000 to the corresponding signals on the VME bus. Finally, it should tie IRQ1* through IRQ4* inputs on its VME 4000 high.

IACK-daisy Chain Driver

The VME 4000 provides the IACK-daisy chain driver functionality required for slot 1 configurations. To configure the device for slot 1 applications, the IACK* output should be connected to the corresponding VME bus signal. DS* is the logical AND of the VMEbus DS0* and DS1* signals. AS* should be connected to the VMEbus AS* signal. When configured this way, the VME 4000 will respond to IACK* being asserted on the bus, by asserting IACKOUT* when both AS* and DS* are asserted. This starts the IACK-daisy chain. IACKOUT* is de-asserted when AS* is de-asserted at the end of the interrupt acknowledge cycle.

If the VME 4000 is not to be configured for slot 1 applications, AS*, DS* and IACKIN* should be tied high and IACKOUT* should be left un-connected.

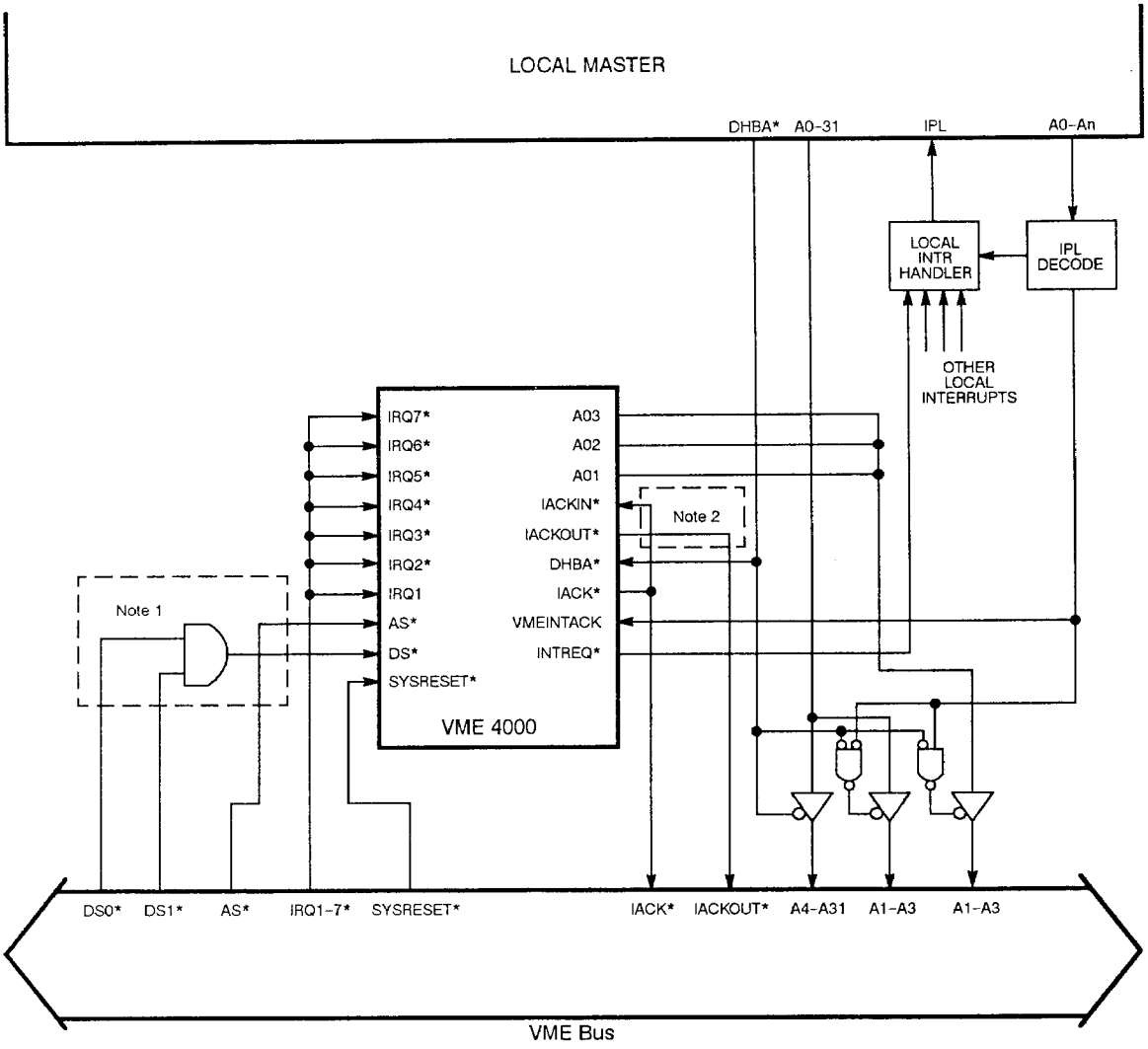


Figure 2. Interrupt Handler Configuration

Note 1. For slot 1 IACK-daisy chain configurations only. Interrupt handler only configurations should tie AS* and DS* high.
2. For slot 1 IACK-daisy chain configurations only. Interrupter handler only configurations should tie IACKIN* high and leave IACKOUT* un-connected.

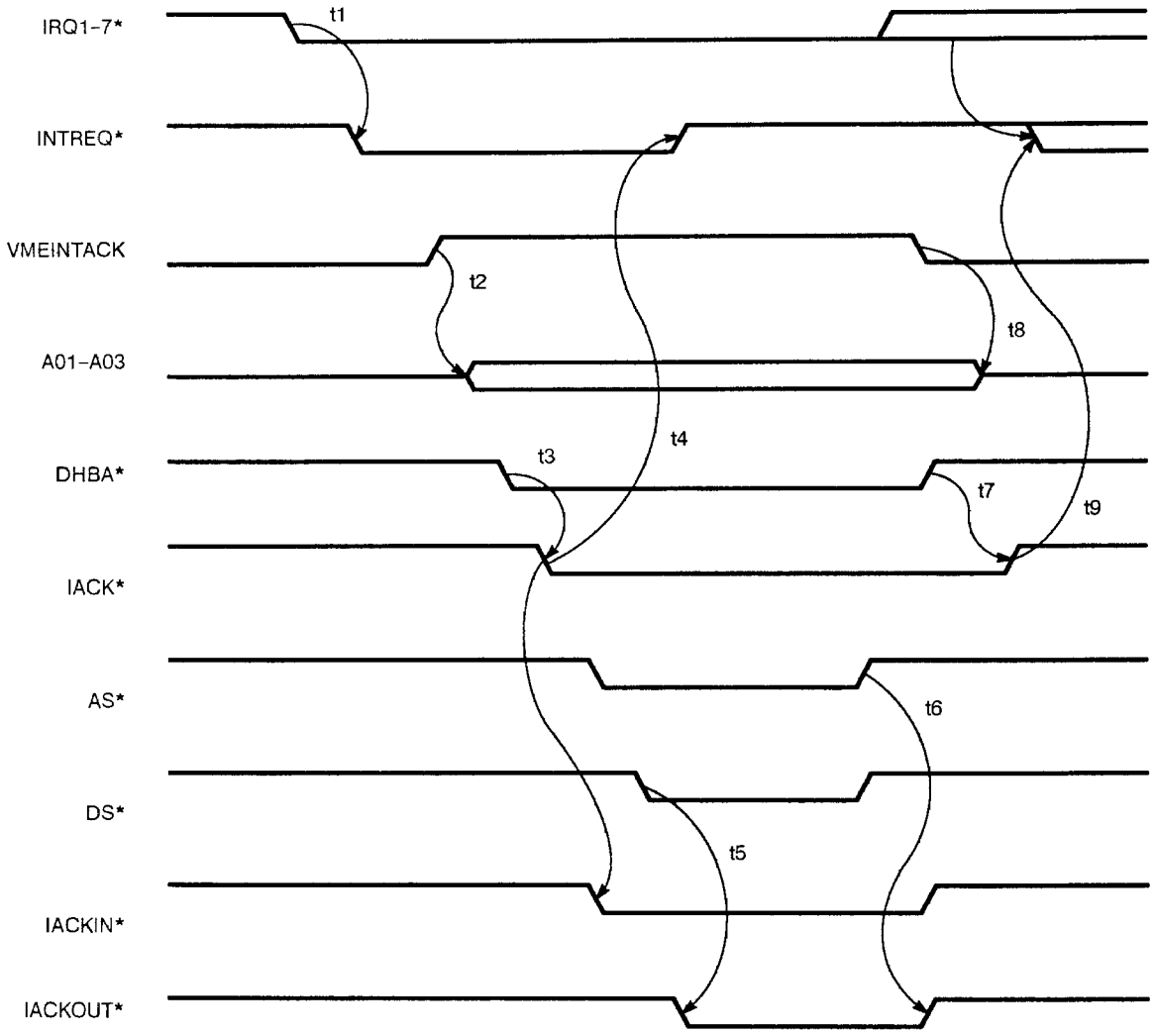


Figure 3. VMEbus Interrupt Handler Timing Diagram

VME 4000 Timing Specifications

Timing Parameter	Signals	Max. Time (ns)		Description
		45	M-65	
t1	IRQ1-7* asserted to INTREQ* asserted	45	65	
t2	VMEINTACK asserted to A01-A03 asserted	45	65	Interrupt requests frozen and prioritized.
t3	DHBA* asserted to IACK* asserted	45	65	
t4	IACK* asserted to INTREQ* de-asserted	45	65	
t5	DS* asserted to IACKOUT* asserted	45	65	
t6	AS* de-asserted to IACKOUT* de-asserted	45	65	Assumes AS* for next cycle. Does not become asserted for this amount of time.
t7	DHBA* de-asserted to IACK* de-asserted	45	65	
t8	VMEINTACK de-asserted to A01-A03 high impedance	45	65	
t9	IACK* de-asserted to INTREQ* asserted	45	65	Assumes another interrupt request is pending.

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -55°C to +125°C
Supply Voltage to Ground ..... -0.5V to +7.0V (pin 24 to pins 12, 18 & 20 DIP)
DC Voltage to Outputs in High Z State ..... -0.5V to +7.0V

Operating Ranges

	Ambient Temperature	Supply Voltage (V_{CC})
Commercial (C)	0°C to +70°C	5V + 5%
Industrial (I)	-40°C to +85°C	5V + 10%
Military (M)	-55°C to +125°C	5V + 10%

Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA (Com'l)		0.5	V
			I_{OL} = 24mA (MIL)		0.6	V
V_{IH}	Input HIGH Level			2.0		V
V_{IL}	Input LOW Level				0.8	V
I_{IX}	Input Leakage Current	V_{SS} <= V_{IN} <= V_{CC}, V_{CC} = Max		-10	10	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{SS} < = V_{OUT} < = V_{CC}		-40	40	mA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.5V		-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max, V_{IN} = GND Outputs Open (Com'l)			80	mA
		V_{CC} = Max, V_{IN} = GND Outputs Open (MIL)			90	mA

Capacitance (sample tested only)

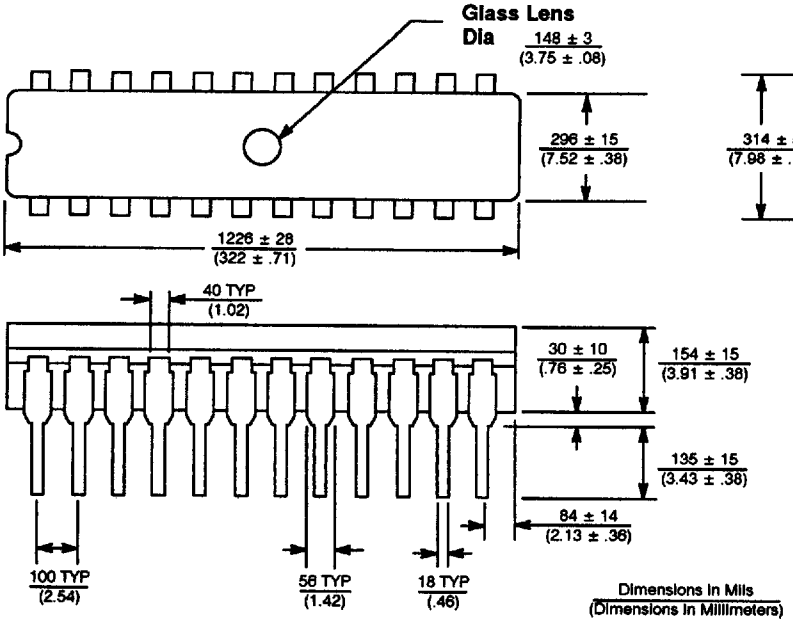
Parameter	Test Conditions	Pins	Typ	Units
C_{IN}	V_{IN} = 2.0V @ f = 1MHz	2-11, 14 (DIP)	5	pF
		13, 15-17, 19, 21-23 (DIP)	10	pF
C_{OUT}	V_{IN} = 2.0V @ f = 1MHz	13, 15-17, 19, 21-23 (DIP)	10	pF

Packaging Information

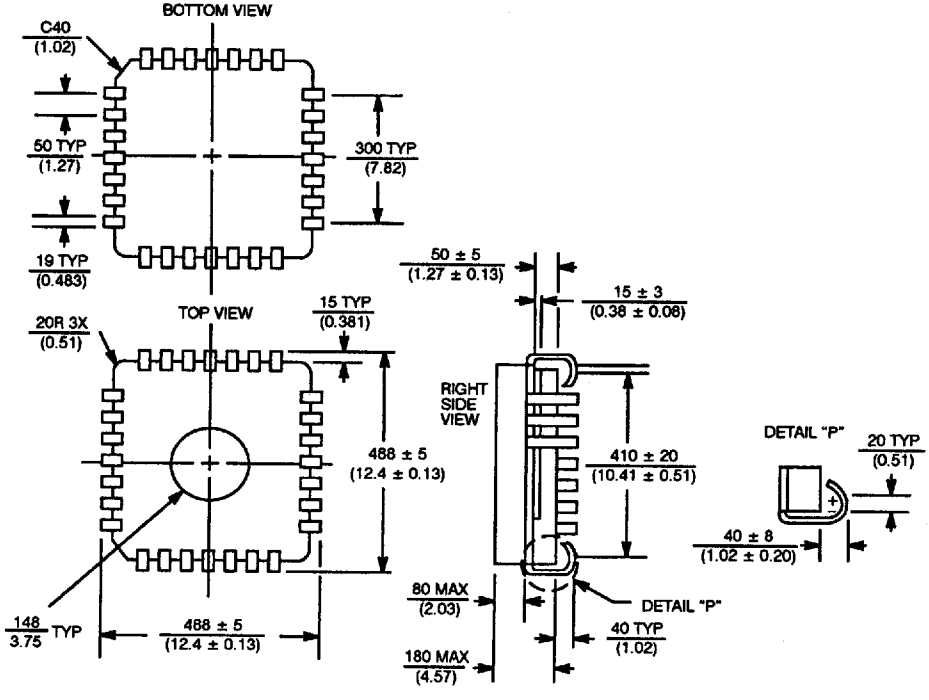
The devices are available in a 24 pin slimline DIP (300 mil wide) or 28 pin LCC.

See PLX 448 or PLX 464 January 1989 or later data sheets for package dimensions. Contact PLX for further packaging information.

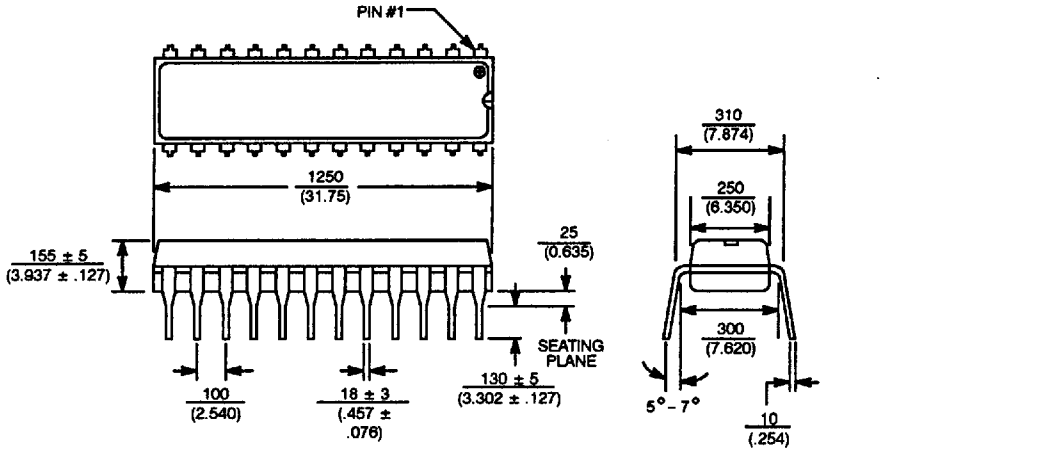
24-Lead Ceramic Dual In-line Package (CERDIP)



28-Pin J Lead Ceramic Chip Carrier



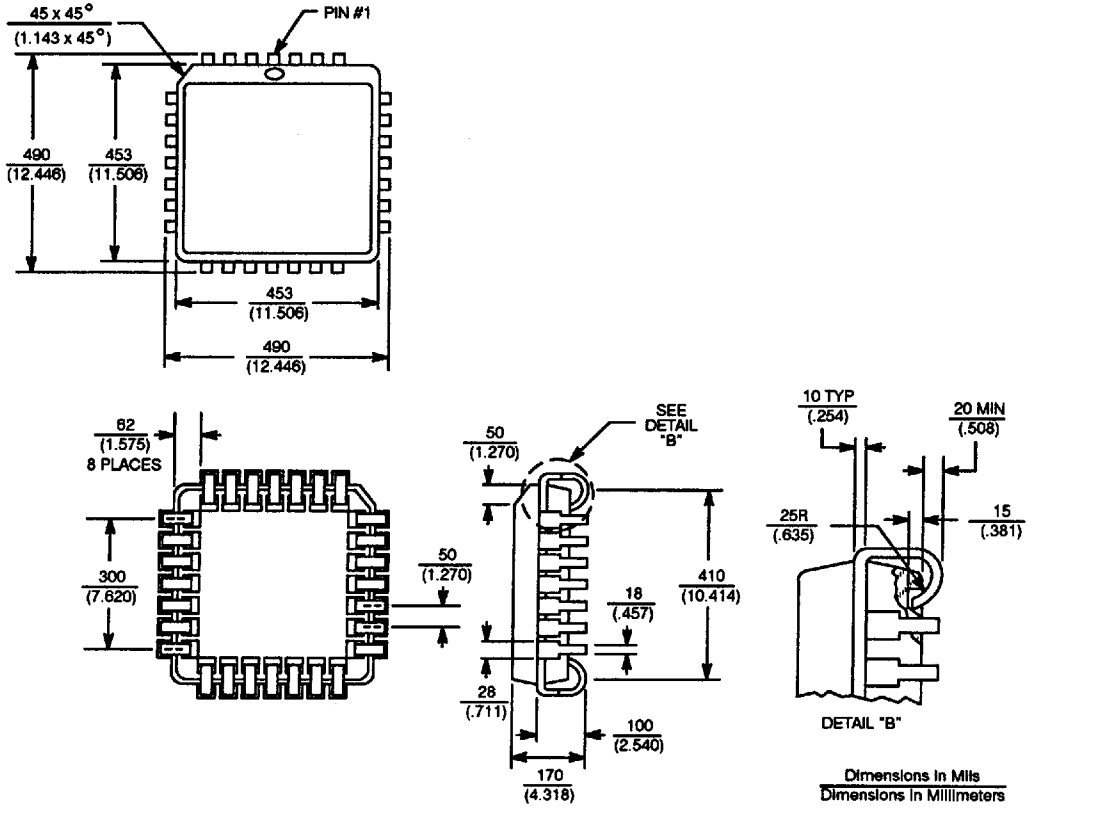
24-Pin DIP Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified

28-Pin LCC Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified