

High-Speed Latched Cache-SRAM

Description

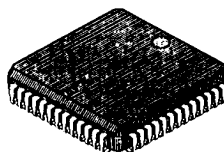
The CXK7701J is a 131,072-bit high speed latched Cache-SRAM suitable for use in high speed cache configurations and low power applications.

Organized as 8192 word $\times$ 16-bit or 4096 word $\times$ 16-bit $\times$ 2 WAY selected by mode control pin, it operates from a single 5V supply.

Features

- Best fit for Cache configurations
Intel 82385 Cache Controller (for 80386-33 MHz, 25MHz, 20MHz)
- Fast access time : (Access time)
CXK7701J-30 30ns (Max.)
CXK7701J-35 35ns (Max.)
CXK7701J-45 45ns (Max.)
- Fast output Enable
CXK7701J-30 10ns (Max.)
CXK7701J-35 13ns (Max.)
CXK7701J-45 16ns (Max.)
- Available in 52 pin PLCC
- Internal 12-bit address latch (A0 – A11)
- Directly TTL compatible : All inputs and outputs

52 pin PLCC (Plastic)

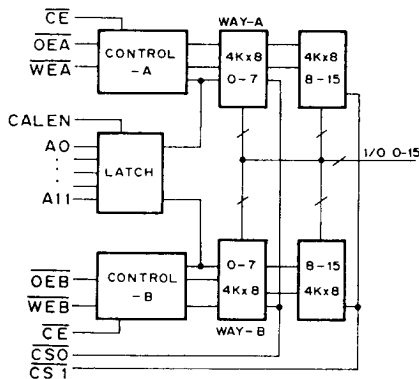


Structure

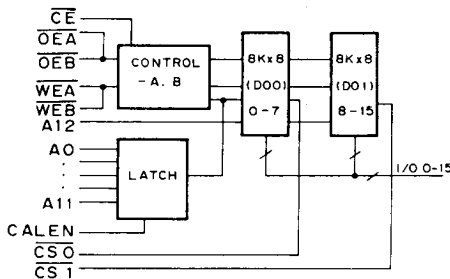
Silicon gate CMOS IC

Block Diagram

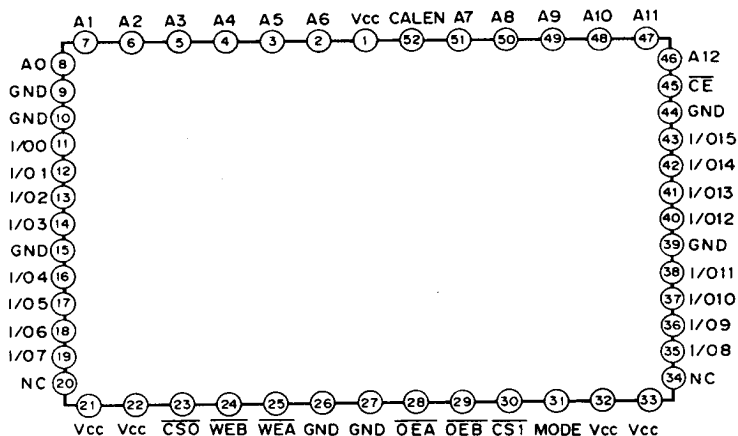
• 2 WAY SET ASSOCIATIVE (MODE = "High")



• DIRECT MAP (MODE = "Low")



Pin Configuration



Pin Description

Symbol	Description
A0 to A12	Address Input
I/O0 to I/O15	Data Input Output
$\overline{CE}$	Global Chip Enable Input
$\overline{CS0}$, $\overline{CS1}$	Chip Enable Input for I/O 0 – 7, I/O 8 – 15
$\overline{OE A}$, $\overline{OE B}$	Output Enable Input for Bank-A, Bank-B
WEA, WEB	Write Enable Input for Bank-A, Bank-B
CALEN	Address Latch Enable Input
MODE	Mode Control
Vcc	+ 5V Power Supply
GND	Ground
NC	No Connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	- 0.5 * to + 7.0	V
Input Voltage	V _{IN}	- 0.5 * to Vcc + 0.5	V
Input & Output Voltage	V _{I/O}	- 0.5 * to Vcc + 0.5	V
Power Dissipation	P _D	2.5	W
Operating Temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering Temperature	T _{solder}	260 • 10	°C • sec

* **Note)** Vcc, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.**DC Recommended Operating Conditions** (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	Vcc + 0.3	V
Input low voltage	V _{IL}	- 0.3 *	—	0.8	V

* **Note)** V_{IL} = - 3.0V Min. for pulse width less than 20ns.**DC and Operating Characteristics**

(Vcc = 5V ± 10%, GND = 0V, Ta = 0 to + 70°C)

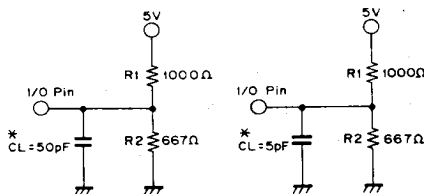
Item	Symbol	Test conditions	Min.	Max.	Unit
Input Leakage Current	I _{LI}	V _{IN} = GND to Vcc	- 2	2	μA
Output Leakage Current	I _{LO}	V _{I/O} = GND to Vcc, $\overline{CE} = V_{IH}$ or $\overline{CS0}$, CS1 = V _{IH} or $\overline{OE A}$, $\overline{OEB} = V_{IH}$ or $\overline{WE A}$, WEB = V _{IL}	- 2	2	μA
Operating Supply Current	I _{cc1}	CS0, CS1 & $\overline{CE} = V_{IL}$ V _{IN} = V _{IL} or V _{IH} I _{OUT} = 0mA	—	180	mA
Average Operating Current	I _{cc2}	100 % Duty Cycle V _{IN} = GND to Vcc I _{OUT} = 0mA	—	240	mA
	I _{cc3}	50 % Duty Cycle V _{IN} = GND to Vcc I _{OUT} = 0mA	—	220	mA
Output High Voltage	V _{OH}	I _{OH} = - 1.0mA	2.4	—	V
Output Low Voltage	V _{OL}	I _{OL} = 4.0mA	—	0.4	V

A. C. Test Condition (Applies to Read & Write Cycle Timing)(V_{CC} = 5V ± 10%, T_a = 0 to +70 °C)

Item	Conditions	Unit
Input Pulse High Level	V _{IH} = 3.0	V
Input Pulse Low Level	V _{IL} = 0.0	V
Input Rise Time	tr = 3	ns
Input Fall Time	tf = 3	ns
Input and Output Reference Level	1.5	V
Output Load (See Test Circuit Fig-1)	R1 1000	Ω
	R2 667	Ω
	CL 50	pF

Fig-1

Output Load (1) Output Load (2) **



* Including scope and jig capacitance

** For tLZ, tHZ, tOHZ, tOLZ, tWLZ, tWHZ

Truth Tables**Two-Way Mode (Mode = High)**

CE	CS0	CST	OEA	OEB	WEA	WEB	Operation	
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled	
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled	
X	X	X	H	H	X	X	Outputs High-Z	
X	X	X	L	L	X	X	Outputs High-Z	
L	L	H	L	H	H	H	Read I/O 0 - 7	Way A
L	L	H	H	L	H	H	Read I/O 0 - 7	Way B
L	H	L	L	H	H	H	Read I/O 8 - 15	Way A
L	H	L	H	L	H	H	Read I/O 8 - 15	Way B
L	L	L	L	H	H	H	Read I/O 0 - 15	Way A
L	L	L	H	L	H	H	Read I/O 0 - 15	Way B
L	L	H	X	X	L	H	Write I/O 0 - 7	Way A
L	L	H	X	X	H	L	Write I/O 0 - 7	Way B
L	H	L	X	X	L	H	Write I/O 8 - 15	Way A
L	H	L	X	X	H	L	Write I/O 8 - 15	Way B
L	L	L	X	X	L	H	Write I/O 0 - 15	Way A
L	L	L	X	X	H	L	Write I/O 0 - 15	Way B
L	L	H	X	X	L	L	Write I/O 0 - 7	Way A & B
L	H	L	X	X	L	L	Write I/O 8 - 15	Way A & B
L	L	L	X	X	L	L	Write I/O 0 - 15	Way A & B

Note) X : "H" or "L"

Truth Tables**Direct Mode** (Mode = Low)

CE	CS0	CS1	OEA	OEB	WEA	WEB	Operation
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled
X	X	X	H	H	X	X	Outputs High-Z
L	L	H	L	L	H	H	Read I/O 0 – 7
L	H	L	L	L	H	H	Read I/O 8 – 15
L	L	L	L	L	H	H	Read I/O 0 – 15
L	L	H	X	X	L	L	Write I/O 0 – 7
L	H	L	X	X	L	L	Write I/O 8 – 15
L	L	L	X	X	L	L	Write I/O 0 – 15

Note) X : "H" or "L"

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Input/Output capacitance	C _{I/O}	V _{I/O} = 0V	—	9	pF

Note) This parameter is sampled and is not 100% tested.

• Write Cycle Timing

(V_{CC} = 5V ± 10 %)

Item	Symbol	- 30		- 35		- 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t _{WC}	30	—	35	—	45	—	ns
Address Valid to End of Write	t _{AW}	20	—	25	—	35	—	ns
A12 Valid to End of Write	t _{A12W}	18	—	22	—	30	—	ns
Chip Select to End of Write	t _{CW}	18	—	22	—	30	—	ns
Data Valid to End of Write	t _{DW}	10	—	12	—	15	—	ns
Data Hold from End of Write	t _{DH}	0	—	0	—	0	—	ns
Write Enable Active to High-Z	t _{WHZ} *	—	15	—	15	—	20	ns
WRITE Enable Inactive to Low-Z	t _{WLZ} *	3	—	3	—	3	—	ns
Write Pulse Width	t _{WP}	18	—	22	—	30	—	ns
CE Pulse Width During Chip Enable Controlled Write	t _{CP}	18	—	22	—	30	—	ns
Address Setup Time	t _{AS}	0	—	0	—	0	—	ns
Write Recovery Time	t _{WR}	0	—	0	—	2	—	ns
Address Latch Enable Pulse Width	t _{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t _{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t _{AHL}	5	—	5	—	5	—	ns

* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1 (2).
This parameter is sampled and is not 100% tested.

• Read Cycle Timing

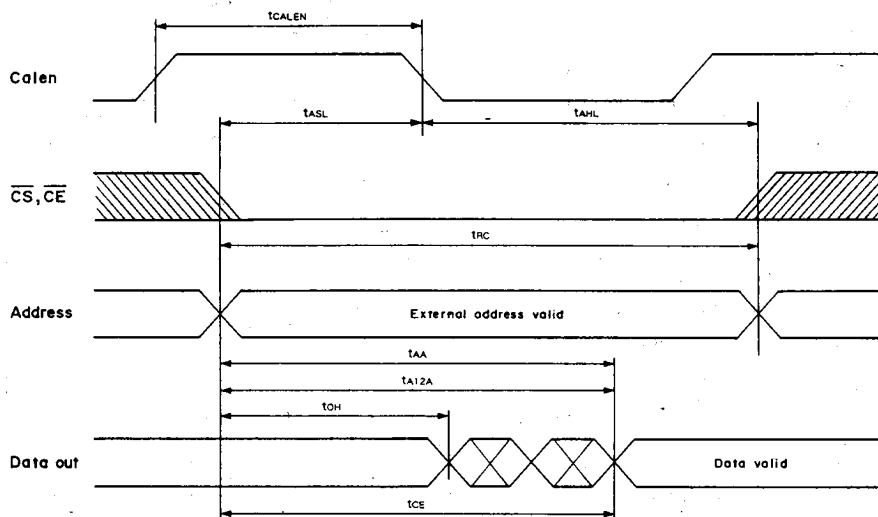
(V_{CC} = 5V ± 10 %)

Item	Symbol	- 30		- 35		- 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t _{RC}	30	—	35	—	45	—	ns
Address Access Time	t _{AA}	—	30	—	35	—	45	ns
A12 Address Access Time	t _{A12A}	—	17	—	25	—	30	ns
Chip Select Access Time	t _{CS} t _{CSE}	—	20	—	25	—	35	ns
Output Enable to Output Valid	t _{OE}	—	10	—	13	—	16	ns
Output Hold from Address Change	t _{OH}	3	—	3	—	3	—	ns
Chip Select to Output Low-Z	t _{LTZ} *	3	—	3	—	3	—	ns
Output Enable to Output Low-Z	t _{OLZ} *	2	—	2	—	2	—	ns
Chip Deselect to Output High-Z	t _{HZ} *	—	15	—	25	—	30	ns
Output Disable to Output High-Z	t _{OHZ} *	—	10	—	14	—	14	ns
Address Latch Enable Pulse Width	t _{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t _{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t _{AHL}	5	—	5	—	5	—	ns

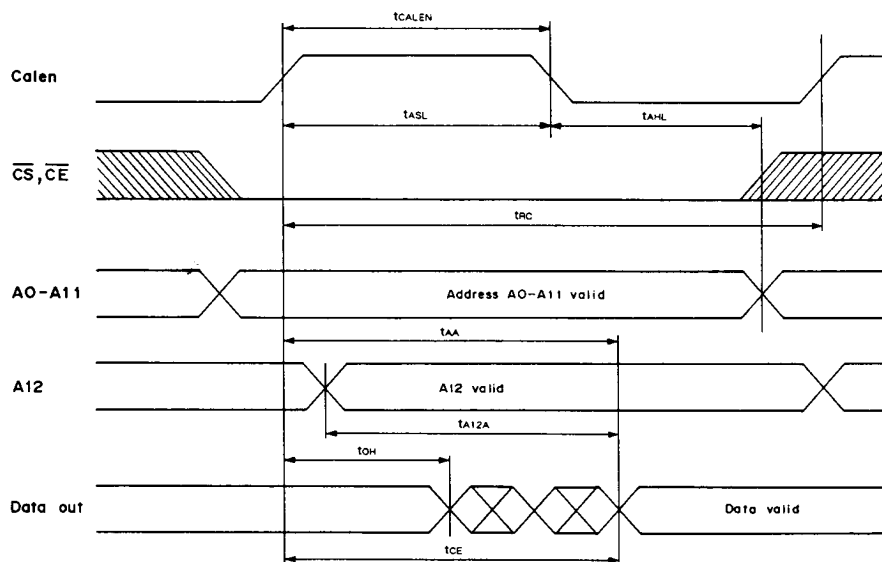
* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1 (2).
This parameter is sampled and is not 100% tested.

Timing Waveform

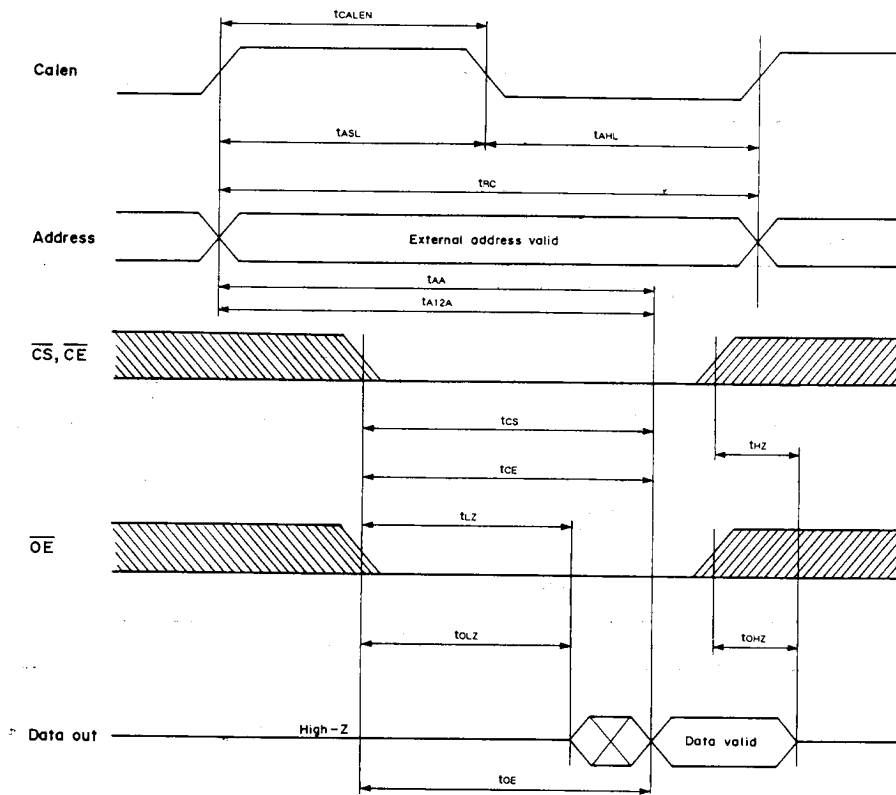
- Read cycle (1) : $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$, $\overline{CS} = V_{IL}$



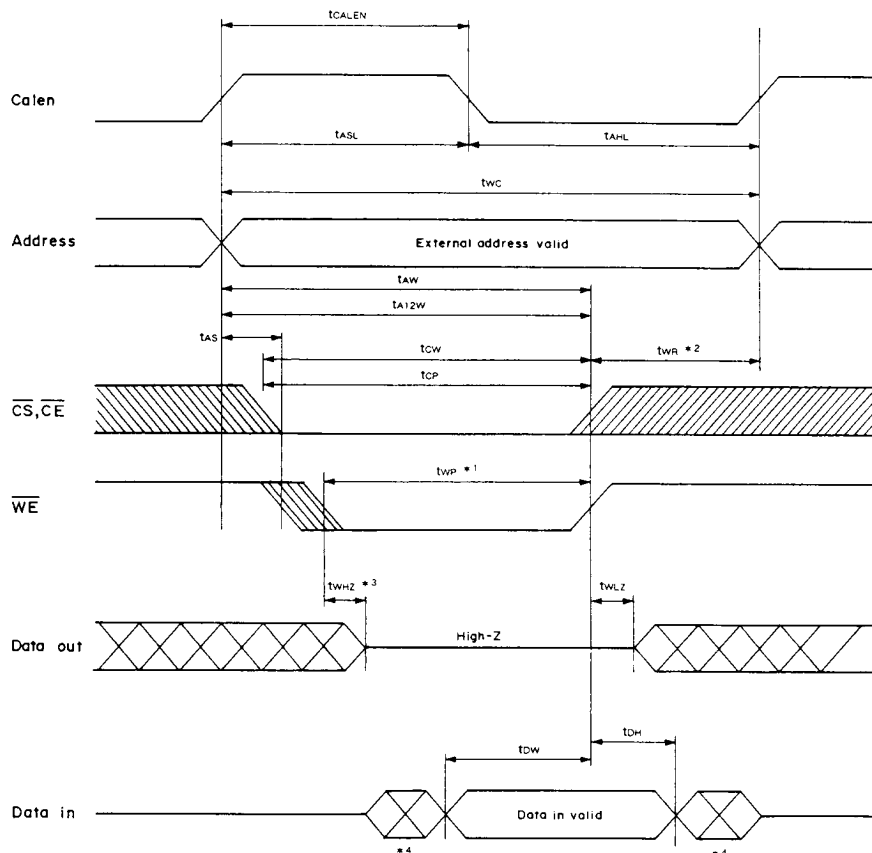
- Read cycle (2) : $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$, $\overline{CS} = V_{IL}$



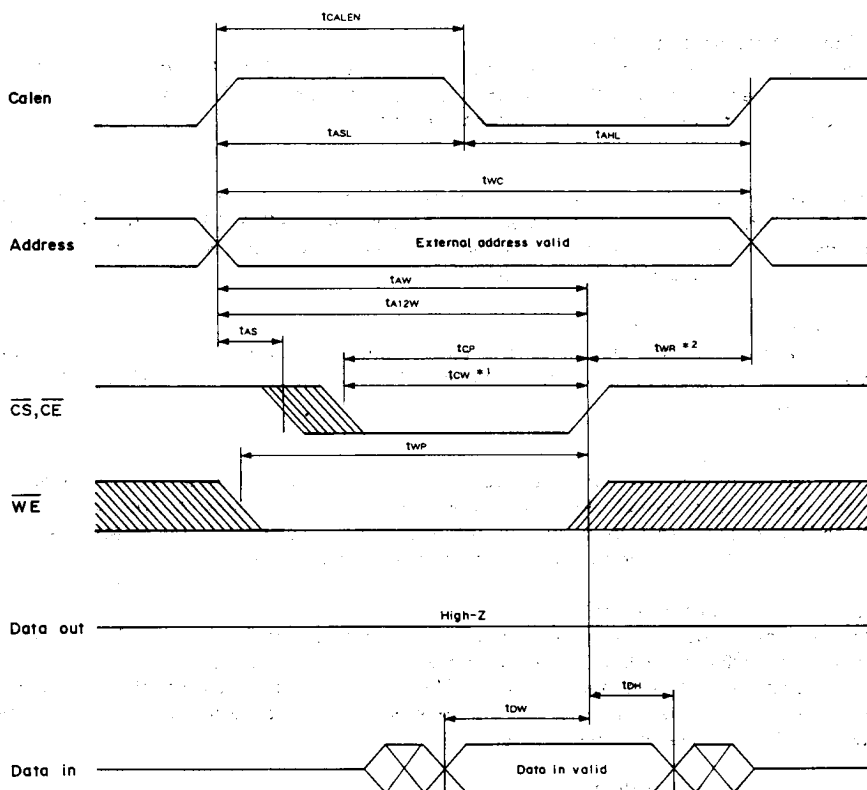
- Read cycle (3) : $\overline{WE} = V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



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- *1. A write occurs during the low overlap of $\overline{CS}$, $\overline{CE}$ and $\overline{WE}$.
- *2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
- *3. If $\overline{CE}$ and $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
- *4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Control Pin Description

CALEN (Cache Address Latch Enable)

This signal controls the internal address latch that resides between the address inputs and the memory array. When CALEN is high the latch is transparent. The falling edge of CALEN latches the current address inputs.

MODE

This signal controls whether the memory device is to be used in a direct mapped (8k × 16) configuration or a two-way set associative (2-4k × 16) configuration. When the mode signal is high, the device is placed in two-way mode. When the mode pin is low, the device is placed in direct mode.

$\overline{CS0}$, $\overline{CS1}$ (Cache Chip Selects)

These active low signals tie to the cache ram chip selects and individually enable the two bytes of the memory. $\overline{CS0}$ enables bits I/O0 – I/O7 and, $\overline{CS1}$ enables bits I/O8 – I/O15.

$\overline{CE}$ (Cache Chip Enable)

This active low signal, when active, enable writes to the data ram or reads from the data ram. It is a global signal, and controls both cache bank A and cache bank B. It's function is the same in both the set associative mode and the direct mapped mode. This input also functions as a chip enable controlled write.

$\overline{OEA}$, $\overline{OEB}$ (Cache Output Enables)

In two-way mode, these active low signals enable cache bank A or B to drive the data bus. Either $\overline{OEA}$ or $\overline{OEB}$ is active during a read hit, depending on which bank is selected. Activation of $\overline{OEA}$ simultaneous with $\overline{OEB}$ will cause both banks to become deselected. In direct mode, these inputs will be externally wired together and A12 will determine which 4K × 16 memory bank is enabled.

$\overline{WEA}$, $\overline{WEB}$ (Cache Write Enables)

In two-way mode, these active low signals enable cache bank A or B to receive data from the data bus. Either $\overline{WEA}$ or $\overline{WEB}$ is enabled in a read miss update or write hit. In direct mode, these inputs will be externally wired together and A12 will determine which 4K × 16 memory bank will be enabled for writing.

A0 – A11 (Addresses)

The address input provide the address into the SRAM array. These signals are latched on the trailing edge of CALEN.

A12 (Address)

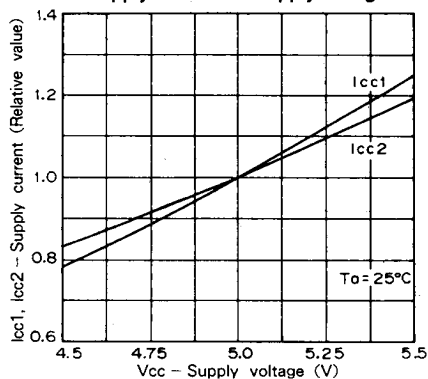
In two-way mode, the upper address input A12 will be a "don't care" and will be externally wired to ground.

In direct mode, A12 will determine which 4K × 16 memory bank is enabled by $\overline{WEA}$ and $\overline{WEB}$, and $\overline{OEA}$ and $\overline{OEB}$.

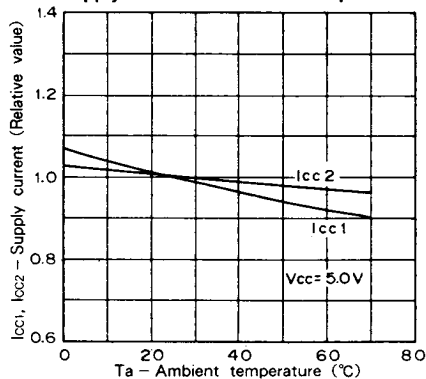
Unlike the other address lines, A12 is not latched.

Example of Representative Characteristics

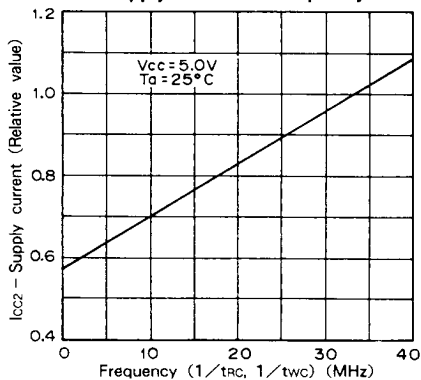
Supply current vs. Supply voltage



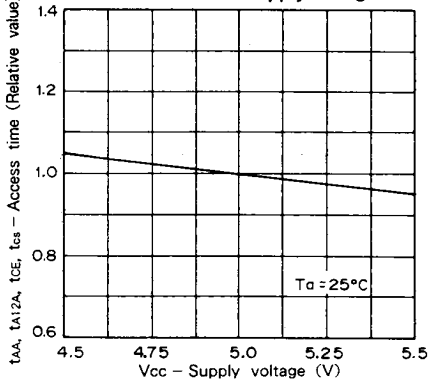
Supply current vs. Ambient temperature



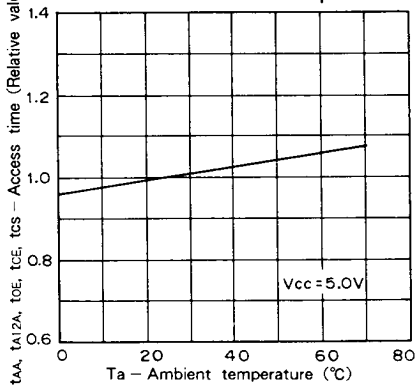
Supply current vs. Frequency



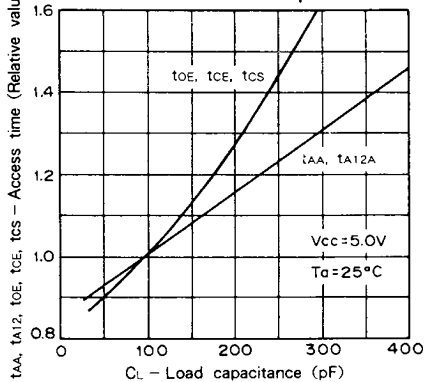
Access time vs. Supply voltage

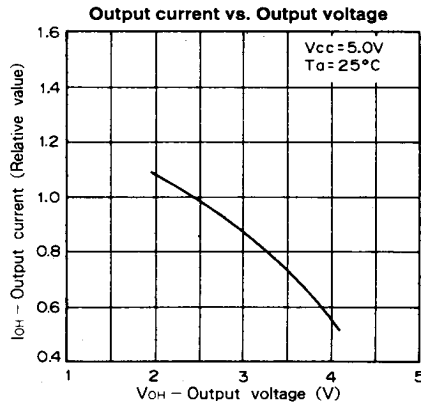
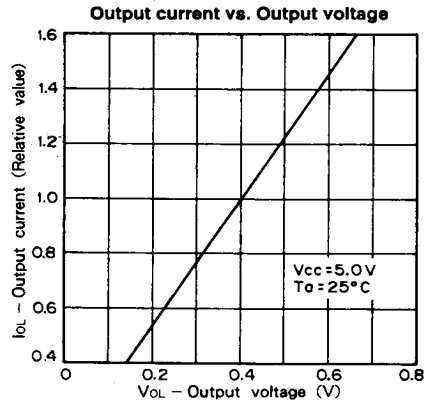
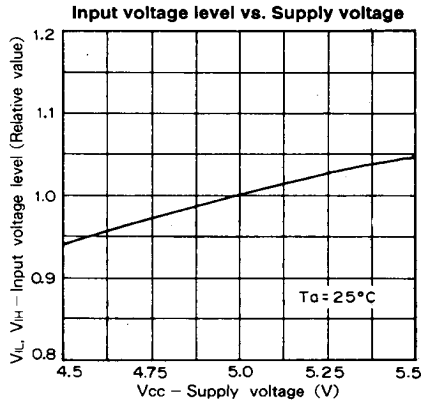


Access time vs. Ambient temperature



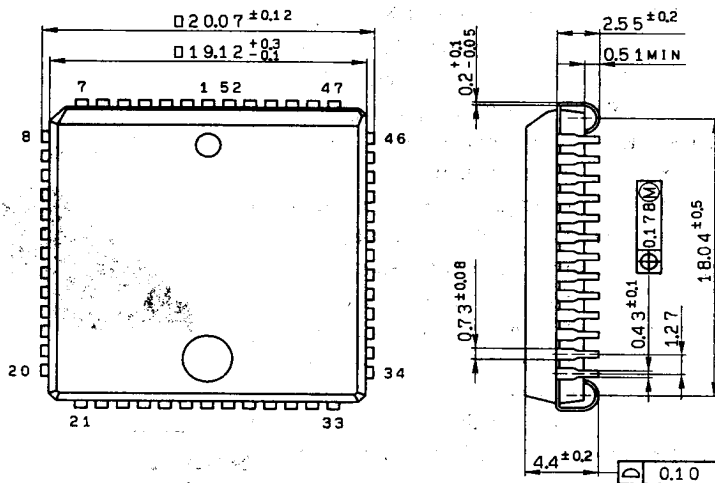
Access time vs. Load capacitance





Package Outline Unit : mm

52 pin PLCC (Plastic)



SONY NAME	PLCC-52P-01
EIAJ NAME	*QFJ052-P-S750-A
JEDEC CODE	MO-047-A-D