SONY

CXP80116

CMOS 8-bit Single Chip Microcomputer

Description

CXP80116 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, VTR vertical sync separation circuit and the measuring circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

80 pin QFP (Plastic)

Also CXP80116 provides power on reset function, sleep/stop function which enables to lower power consumption, modes which extends an external memory and microprocessor mode.

Features

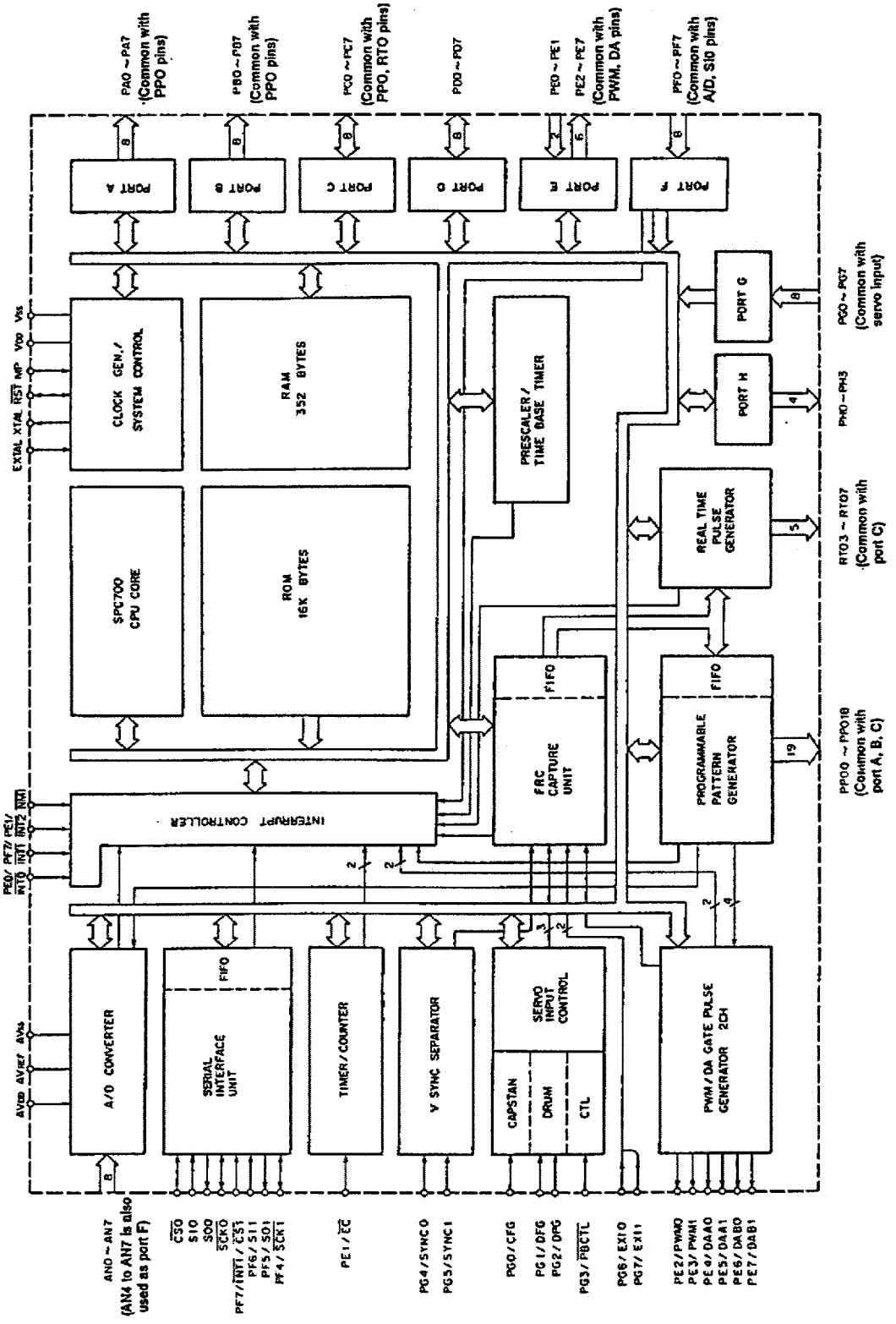
- A wide instruction set (213 instructions) which cover various types of data.
  - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle — During operation 500ns/8MHz
- Incorporated ROM capacity — 16Kbytes
- Incorporated RAM capacity — 352bytes
- Enables to extend a memory (ROM, RAM) up to 64Kbytes
- Peripheral function
  - A/D converter — 8-bit, 8-channel, successive approximation system (Conversion time : 20 µs)
  - Serial I/O — Incorporated 8-bit and 8-stage FIFO for data (1 to 8 bytes auto transfer)
  - Timer — 8-bit timer, 8-bit timer/counter, 19-bit time base timer
  - High precision timing pattern generator — PPG (19 pins) /RTG (5 pins)
  - PWM/DA gate output — 12 bit, 2-channel
  - Servo input control — Capstan FG, Drum FG/PG, CTL input
  - VSYNC separator
  - FRC capture unit — Incorporated 22-bit and 6-stage FIFO
- Interruption — 15 factors, 15 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- 3-type operation modes — Single chip mode/Memory extension mode/Microprocessor mode
- Package — 80-pin plastic QFP

Structure

Silicon gate CMOS IC

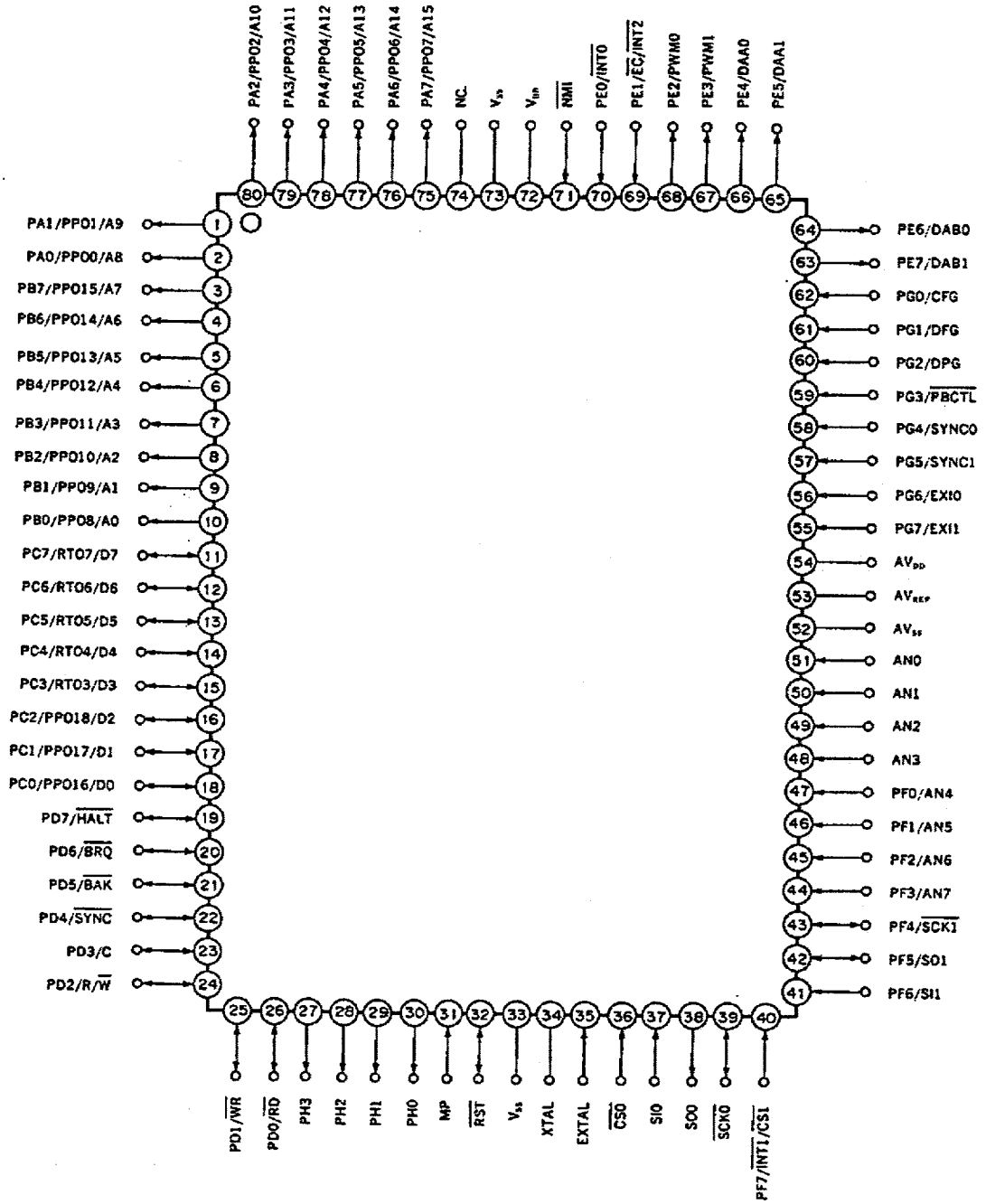
E89543A2X – ST

Block Diagram



Pin Configuration Diagram (Top View)

Note) 1) NC (pin 74) is always connected to V_{DD}.
2) V_{SS} (pins 33 and 73) are both connected to GND.

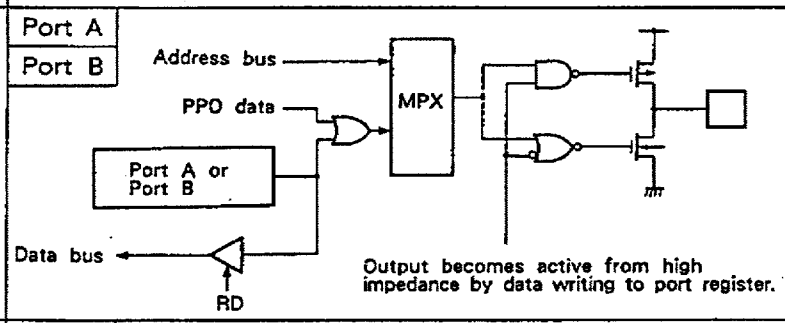
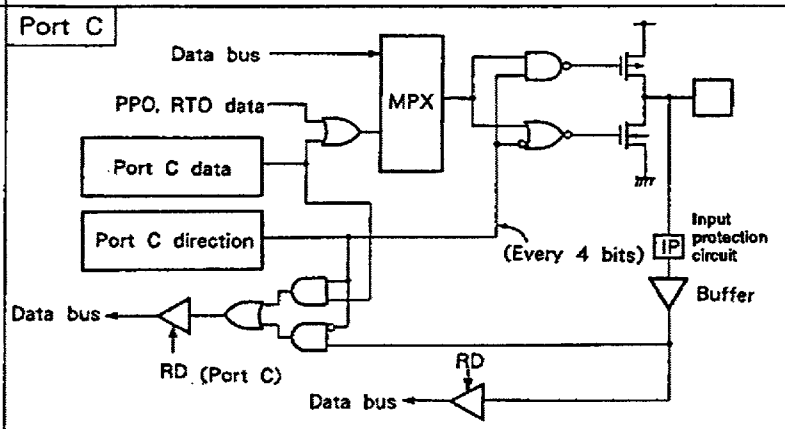
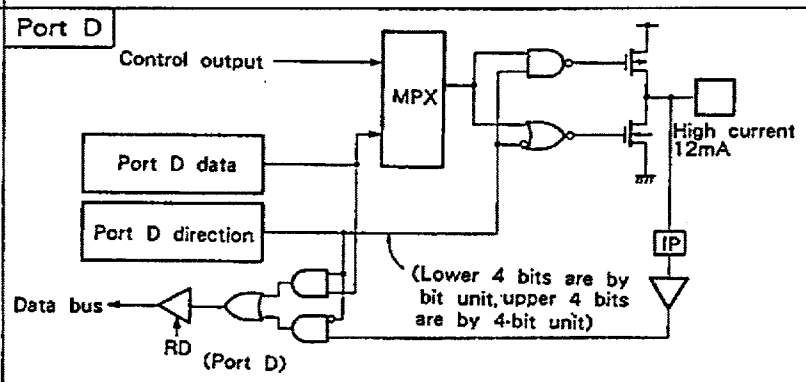
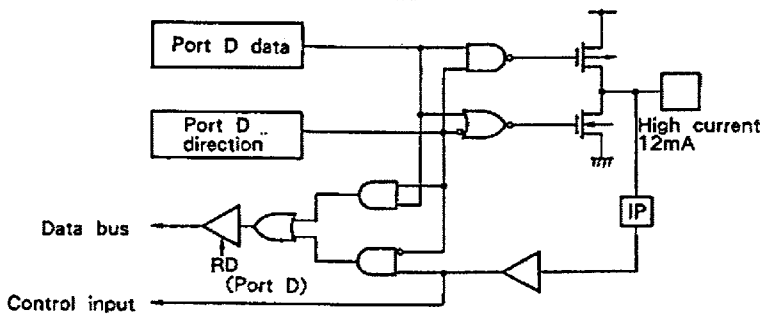


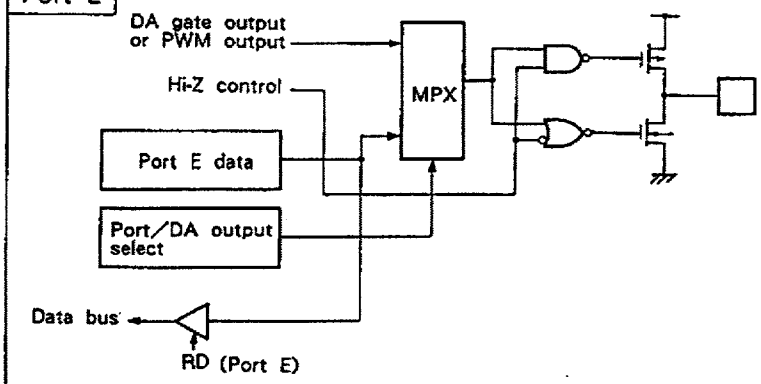
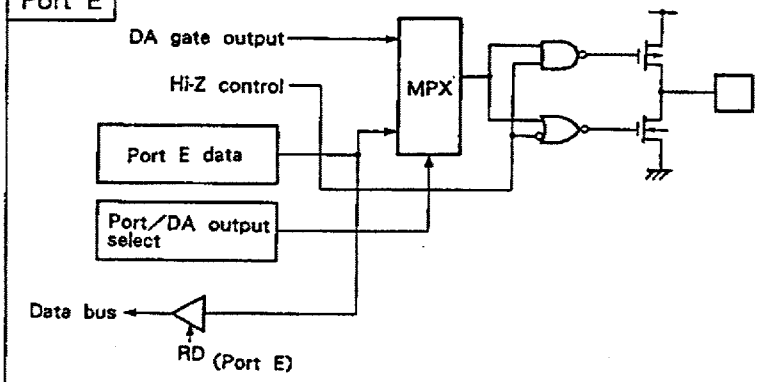
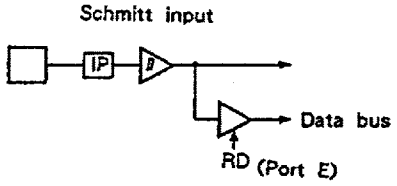
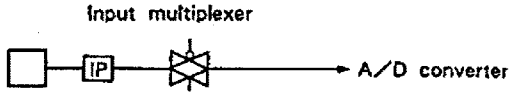
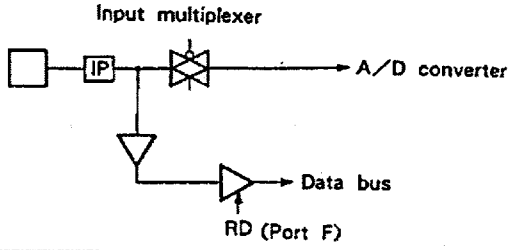
Pin Description

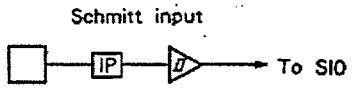
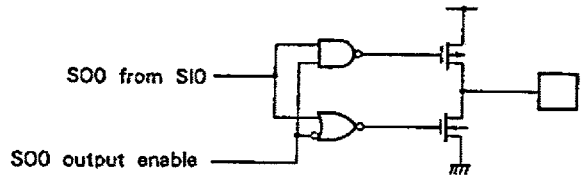
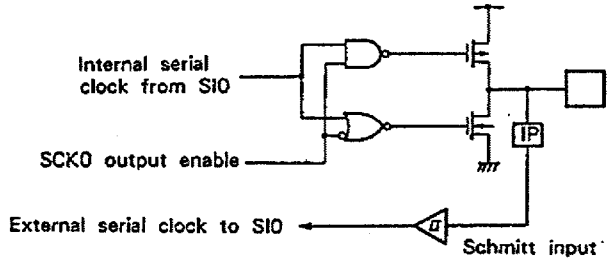
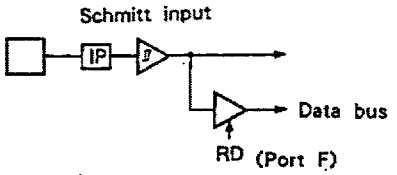
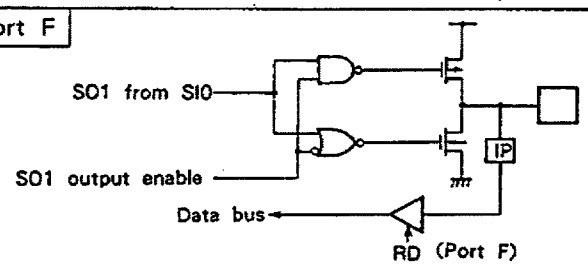
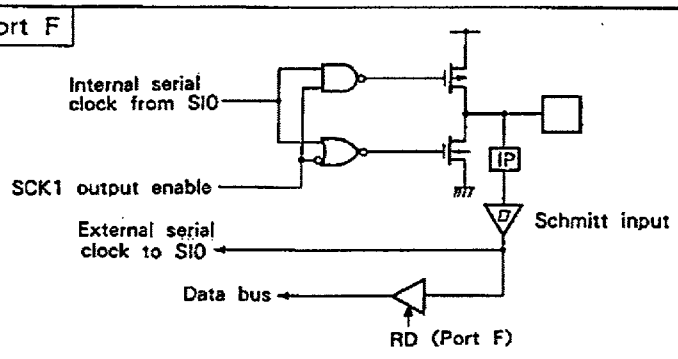
<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td>PA0/PPO0/A8 to PA7/PPO7/A15</td><td>Output/ Real time Output/ Output</td><td>(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)</td><td rowspan="2">Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins)</td><td rowspan="2">Functions as address bus for external memory in the memory extension mode or microprocessor mode. (16 pins)</td></tr>
<tr><td>PB0/PPO8/A0 to PB7/PPO15/A7</td><td>Output/ Real time Output/ Output</td><td>(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)</td></tr>
<tr><td>PC0/PPO16/D0 to PC2/PPO18/D2</td><td>I/O/ Real time Output/ I/O</td><td rowspan="2">(Port C) 8-bit input/output port, enables to specify input/output by 4-bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)</td><td rowspan="2">Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)</td><td rowspan="2">Functions as data bus for external memory in the memory extension mode or microprocessor mode. (8 pins)</td></tr>
<tr><td>PC3/RTO3/D3 to PC7/RTO7/D7</td><td>I/O/ Real time Output/ I/O</td></tr>
<tr><td>PD0/$\overline{RD}$</td><td>I/O/Output</td><td rowspan="8">(Port D) 8-bit input/output port. Lower 4 bits can be specified as input/output by bit unit and upper 4 bits can be specified as input/output by 4-bit unit. Enables to drive 12mA sync current. (8 pins)</td><td colspan="2">Strobe signal for external memory reading operation. Enabled when "L".</td></tr>
<tr><td>PD1/$\overline{WR}$</td><td>I/O/Output</td><td colspan="2">Strobe signal for external memory writing operation. Enabled when "L".</td></tr>
<tr><td>PD2/R/$\overline{W}$</td><td>I/O/Output</td><td colspan="2">"H" when CPU's machine cycle is in read cycle, "L" when in write cycle.</td></tr>
<tr><td>PD3/C</td><td>I/O/Output</td><td colspan="2">Timing signal output pin.</td></tr>
<tr><td>PD4/$\overline{SYNC}$</td><td>I/O/Output</td><td colspan="2">"L" when CPU is in opcode fetch cycle.</td></tr>
<tr><td>PD5/$\overline{BAK}$</td><td>I/O/Output</td><td colspan="2">"L" when CPU receives bus request ($\overline{BRQ}$), at the same time address output, data input/output, $\overline{RD}$, $\overline{WR}$ and R/$\overline{W}$ pins become high impedance state.</td></tr>
<tr><td>PD6/$\overline{BRQ}$</td><td>I/O/Output</td><td colspan="2">Input pin to bus-request for CPU.</td></tr>
<tr><td>PD7/$\overline{HALT}$</td><td>I/O/Output</td><td colspan="2">Input pin to stop CPU operation.</td></tr>
<tr><td>PE0/$\overline{INT0}$</td><td>Input</td><td rowspan="8">(Port E) 8-bit port. Lower 2 bits are input pins, upper 6 bits are output pins. (8 pins)</td><td colspan="2">Input pin to request external interruption. Active when falling edge.</td></tr>
<tr><td>PE1/$\overline{EC}$/$\overline{INT2}$</td><td>Input</td><td>External event input pin for timer/counter.</td><td>Input pin to request external interruption. Active when falling edge.</td></tr>
<tr><td>PE2/PWM0</td><td>Output</td><td colspan="2" rowspan="2">PWM output pins. (2 pins)</td></tr>
<tr><td>PE3/PWM1</td><td>Output</td></tr>
<tr><td>PE4/DAA0</td><td>Output</td><td colspan="2" rowspan="4">DA gate pulse output pins. (4 pins)</td></tr>
<tr><td>PE5/DAA1</td><td>Output</td></tr>
<tr><td>PE6/DAB0</td><td>Output</td></tr>
<tr><td>PE7/DAB1</td><td>Output</td></tr>
</table>

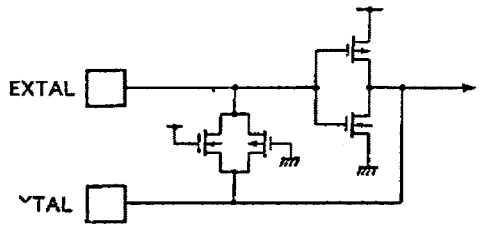
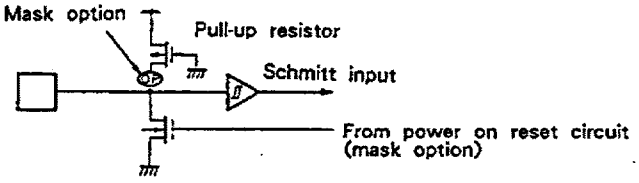
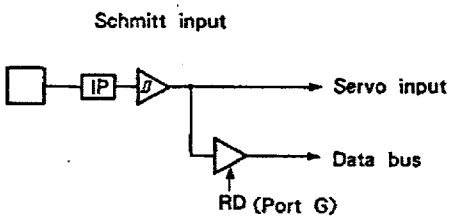
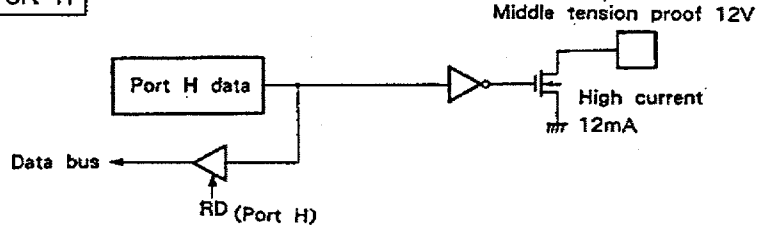
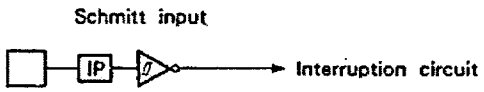
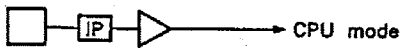
Symbol	I/O	Description
AN0 to AN3	Input	Analog input pins to A/D converter. (8 pins)
PF0/AN4 to PF3/AN7	Input	(Port F) 8-bit input port. Lower 4 bits also serve as standby release input pin. (8 pins)
PF4/$\overline{SCK1}$	Input/ I/O	Serial clock input/output pin.
PF5/SO1	Input/ Output	Serial data output pin.
PF6/SI1	Input	Serial data input pin.
PF7/$\overline{INT1}$ /$\overline{CS1}$	Input	External interrupt request input pin. Active when falling edge. / Chip select input pin to serial interface.
$\overline{SCK0}$	I/O	Serial clock input/output pin.
SO0	Output	Serial data output pin.
SI0	Input	Serial data input pin.
$\overline{CS0}$	Input	Chip select input pin to serial interface.
PG0/CFG	Input	(Port G) 8-bit input port. (8 pins) / Capstan FG input pin.
PG1/DFG	Input	Drum FG input pin.
PG2/DPG	Input	Drum PG input pin.
PG3/$\overline{PBCTL}$	Input	Playback CTL pulse input pin.
PG4/SYNC0	Input	Composite sync signal input pin.
PG5/SYNC1	Input	
PG6/EXI0	Input	External input pin to FRC capture unit.
PG7/EXI1	Input	
PH0 to PH3	Output	(Port H) 4-bit output port; Middle tension proof (12V) and high current (12mA), N-ch open drain output. (4 pins)
$\overline{NMI}$	Input	Non-maskable interrupt request pin. Active during falling edge.
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and set XTAL pin to open.
XTAL	Output	
$\overline{RST}$	I/O	System reset pin of active "L" level. $\overline{RST}$ pin is input/output pin, which output "L" level by incorporated power on reset function when power on. (Mask option)
MP	Input	Microprocessor mode input pin. When it is set to "H" level, it becomes microprocessor mode. When it is "L" level, single chip mode or memory extension mode is selected.
AV_{DD}		Positive power supply pin of A/D converter.
AV_{REF}	Input	Reference voltage input pin of A/D converter.
AV_{SS}		GND pin of A/D converter.
V_{DD}		Positive power supply pin.
V_{SS}		GND pin. Connect both V_{SS} pins to GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/PPO0/A8 to PA7/PPO7/A15 PB0/PPO8/A0 to PB7/PPO15/A7 16 pins		Hi-Z
PC0/PPO16/D0 to PC2/PPO18/D2 PC3/RTO3/D3 to PC7/RTO7/D7 8 pins		Hi-Z
PD0/$\overline{RD}$ PD1/$\overline{WR}$ PD2/R/$\overline{W}$ PD3/C PD4/$\overline{SYNC}$ PD5/$\overline{BAK}$ 6 pins		Hi-Z
PD6/$\overline{BRQ}$ PD7/$\overline{HALT}$ 2 pins		Hi-Z

Pin	Circuit format	When reset
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E 	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E 	H level
PE0/$\overline{\text{INT0}}$ PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$ 2 pins	Port E 	Hi-Z
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z

Pin	Circuit format	When reset
$\overline{CS0}$ SI0 2 pins		Hi-Z
SO0 1 pin		Hi-Z
$\overline{SCK0}$ 1 pin		Hi-Z
PF7/$\overline{CS1}$/$\overline{INT1}$ PF6/SI1 2 pins	Port F 	Hi-Z
PF5/SO1 1 pin	Port F 	Hi-Z
PF4/$\overline{SCK1}$ 1 pin	Port F 	Hi-Z

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
$\overline{RST}$ 1 pin		L level
PG0/CFG PG1/DFG PG2/DPG PG3/$\overline{PBCTL}$ PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1 8 pins	Port G  (Note) For PG4/SYNC0, PG5/SYNC1, TTL schmitt input can be selected with the mask option.	Hi-Z
PH0 to PH3 4 pins	Port H 	Open
NMI 1 pin		Hi-Z
MP 1 pin		Hi-Z

Absolute Maximum Ratings V_{SS} = 0V

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD}	−0.3 to +7.0	V	
	AV_{DD}	AV_{SS} to +7.0*1	V	
	AV_{SS}	−0.3 to +0.3	V	
Input voltage	V_{IN}	−0.3 to +7.0*2	V	
Output voltage	V_{OUT}	−0.3 to +7.0*2	V	
Middle tension proof output voltage	V_{OUTP}	−0.3 to +15.0	V	PH pin
High level output current	I_{OH}	−5	mA	
High level total output current	ΣI_{OH}	−50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than high current output pins : per pin
	I_{OLC}	20	mA	High current port pin*3 : per pin
Low level total output current	ΣI_{OL}	130	mA	Total of output pins
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operation conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

*1) AV_{DD} and V_{DD} should be set to a same voltage.

*2) V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*3) The high current operation transistors are the N-CH transistors of the PD and PH ports.

Recommended Operating Condition V_{SS} = 0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range during operation
		2.5	5.5	V	Guaranteed data hold operation range during STOP
Anaolg power supply	AV_{DD}	4.5	5.5	V	*1
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	C-MOS schmitt input*3
	V_{IHTS}	2.2	V_{DD}	V	TTL schmitt input*4
	V_{IHEX}	V_{DD}−0.4	V_{DD}+0.3	V	EXTAL pin*5
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2
	V_{ILS}	0	0.2V_{DD}	V	C-MOS schmitt input*3
	V_{ILTS}	0	0.8	V	TTL schmitt input*4
	V_{ILEX}	−0.3	0.4	V	EXTAL pin*5
Operating temperature	Topr	−20	+75	°C	

*1) AV_{DD} and V_{DD} should be set to a same voltage.
*2) Normal input port (each pin of PC, PD, PF0 to PF3 and PF5), MP pin
*3) Each pin of $\overline{NMI}$, $\overline{CS0}$, SI0, $\overline{SCK0}$, $\overline{RST}$, PE0/$\overline{INT0}$, PE1/$\overline{EC}$/$\overline{INT2}$, PF4/$\overline{SCK1}$, PF6/SI1, PF7/$\overline{INT1}$/$\overline{CS1}$ and PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option)
*4) Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)
*5) It specifies only when the external clock is input.

Electrical Characteristics

DC characteristics $T_a = -20°C$ to $+75°C$, $V_{SS} = 0V$

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4, PF5, SO0, $\overline{SCK0}$, PH (V_{OL} only), $\overline{RST}$ *1 (V_{OL} only)	$V_{DD} = 4.5V$, $I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V$, $I_{OH} = -1.2mA$	3.5			V
Low level output voltage	V_{OL}		$V_{DD} = 4.5V$, $I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V$, $I_{OL} = 3.6mA$			0.6	V
		PD, PH	$V_{DD} = 4.5V$, $I_{OL} = 12.0mA$			1.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V$, $V_{IH} = 5.5V$	0.5		40	μA
	I_{ILE}		$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	−0.5		−40	μA
	I_{ILR}	$\overline{RST}$ *2	$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	−1.5		−400	μA
I/O leakage current	I_{IZ}	PA to PG, AN0 to AN3, $\overline{CS0}$, SI0, SO0, $\overline{SCK0}$, $\overline{NMI}$, $\overline{RST}$ *2, MP	$V_{DD} = 5.5V$ $V_I = 0, 5.5V$			±3	μA
Open drain output leakage current (N-CH Tr OFF in state)	I_{LOH}	PH	$V_{DD} = 5.5V$ $V_{OH} = 12V$			50	μA
Supply current	I_{DD}	V_{DD}	Operating mode (1/2 dividing clock) Crystal oscillation (C1 = C2 = 15pF) of 8MHz Entire output pins open		20	40	mA
	I_{DDSL}		SLEEP mode		5	15	mA
	I_{DDST}		STOP mode			3	μA
Input capacity	C_{IN}	Other than V_{DD}, V_{SS}, AV_{DD}, AV_{SS} pins	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) $\overline{RST}$ pin specifies only when the power on reset circuirt has been selected with mask option.
*2) $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when non-resistance is selected.

AC Characteristics

(1) Clock timing

Ta = −20°C to +75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1	8	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	50		ns
System clock input rising and falling times	t_{CR} t_{CF}				200	ns
Event count clock input pulse width	t_{EL} t_{EH}	$\overline{EC}$	Fig. 3	tsys*1 +50		ns
Event count clock input rising and falling times	t_{ER} t_{EF}	$\overline{EC}$	Fig. 3		20	ms

*1) tsys indicates three values according to the contents of the clock control register (address; $00FF_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

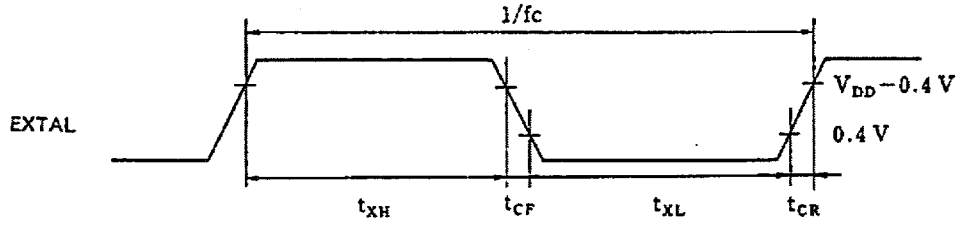


Fig. 1 Clock timing

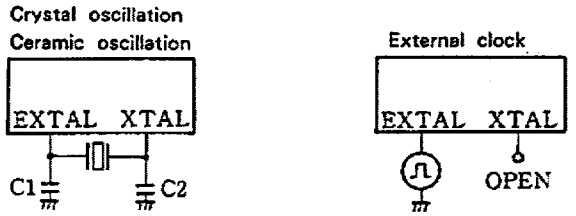


Fig. 2 Clock applying condition

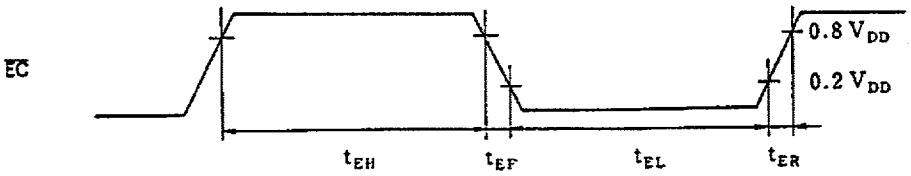


Fig. 3 Event count clock timing

(2) Serial transfer

Ta = −20°C to +75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS}$ ↓→$\overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS}$ ↑→$\overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$ $\overline{SCK1}$			tsys + 200	ns
$\overline{CS}$ ↓→SO delay time	t_{DCSO}	SO0 SO1	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ ↓→SO floating delay time	t_{DCSOF}	SO0 SO1			tsys + 200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$ $\overline{CS1}$		tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	tsys + 100		ns
			Output mode	8000/fc−50		ns
SI input setup time (against $\overline{SCK}$ ↑)	t_{SIK}	SI0 SI1	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}$ ↑)	t_{KSI}	SI0 SI1	$\overline{SCK}$ input mode	tsys + 200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓→SO delay time	t_{KSO}	SO0 SO1	$\overline{SCK}$ input mode		tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address ; 00FF$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

2) The marks $\overline{CS}$, $\overline{SCK}$, SI and SO respectively mean pins of $\overline{CS}$→$\overline{CS0}$, $\overline{CS1}$, $\overline{SCK}$→$\overline{SCK0}$, $\overline{SCK1}$, SI→SI0, SI1, and SO→SO0, SO1.

3) The Load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

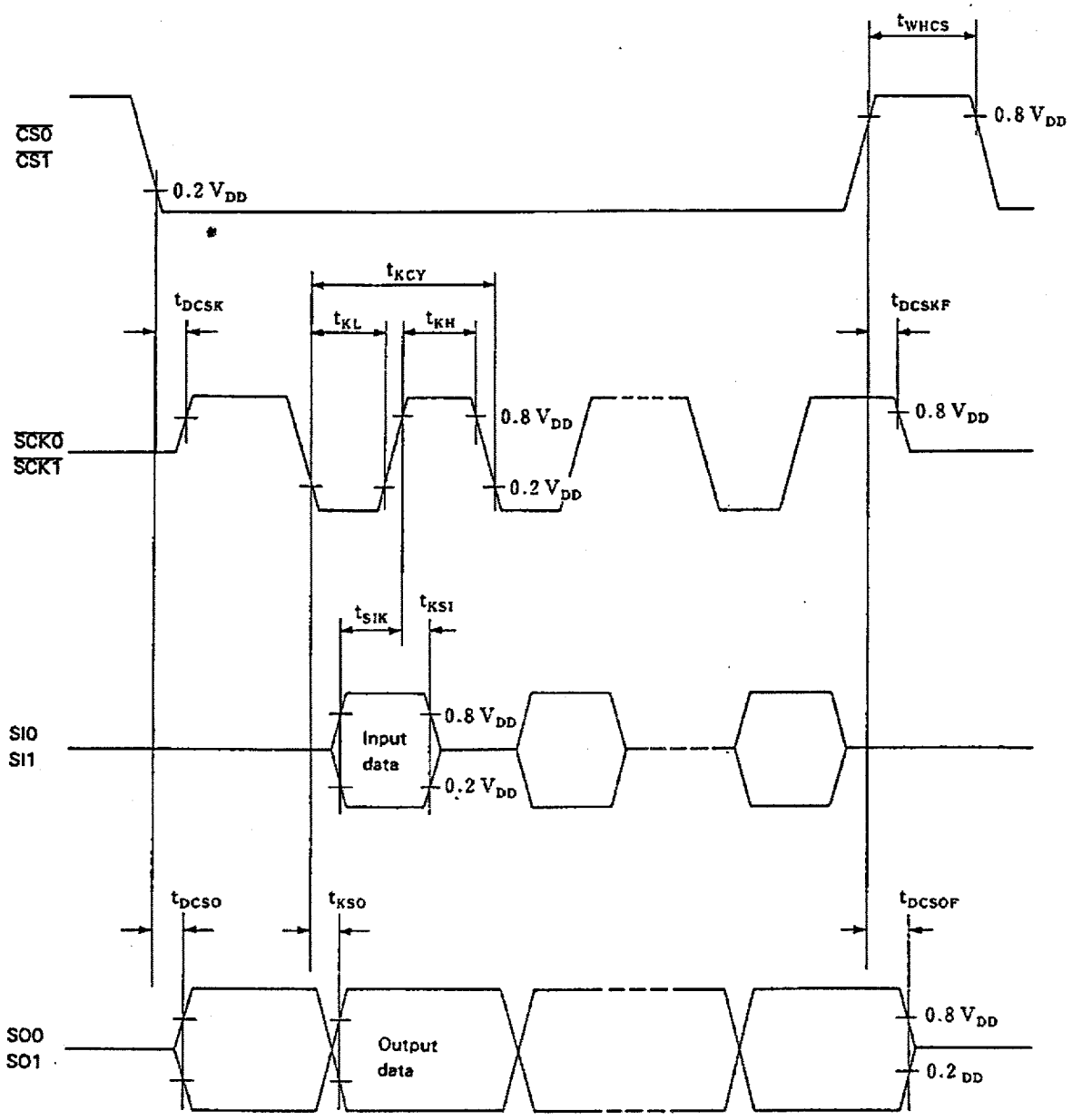


Fig. 4 Serial transfer timing

(3) A/D converter characteristics

Ta = −20°C to +75°C, V_{DD} = AV_{DD} = 4.5V to 5.5V, AV_{REF} = 4.0V to AV_{DD}, V_{SS} = AV_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{DD} = 5.0V V_{SS} = AV_{SS} = 0V			±1	LSB
Zero transition voltage	V_{ZT} *1			−10	30	70	mV
Full scale transition voltage	V_{FT} *2			4930	4970	5010	mV
Conversion time	t_{CONV}			160/fc			µs
Sampling time	t_{SAMP}			12/fc			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD} − 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode			10	µA

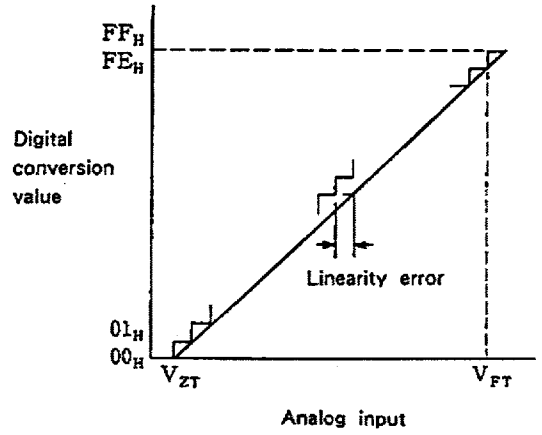


Fig. 5. Definitions of A/D converter terms

* 1) V_{ZT} : Indicates the value that digital conversion value changes from 00$_H$ to 01$_H$ and vice versa.
* 2) V_{FT} : Indicates the value that digital conversion value changes from FE$_H$ to FF$_H$ and vice versa.

(4) Interruption, reset input Ta = −20°C to +75°C, V_{DD} = 4.5V to 5.5V, Vss = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH}, t_{IL}	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{NMI}$		1		μs
Reset input low level width	t_{RSL}	$\overline{RST}$		8/fc		μs

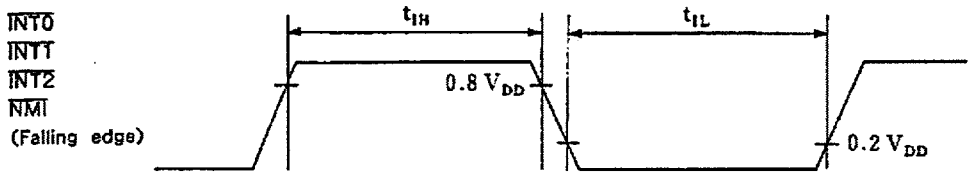


Fig. 6 Interruption input timing

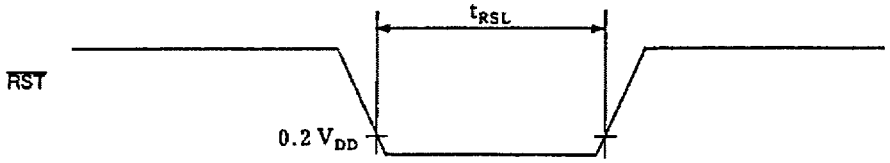


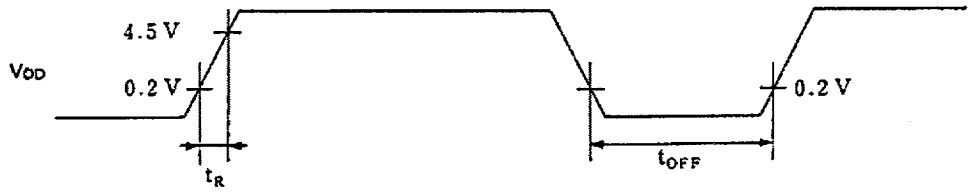
Fig. 7 Reset input timing

(5) Power on reset

Power on reset * Ta = −20°C to +75°C, V_{DD} = 4.5V to 5.5V, Vss = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

* Specifies only when power on reset function is selected.



The power supply should rise smoothly.

Fig. 8 Power on reset

(6) Others

Ta = −20°C to +75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
GFG input high and low level widths	t_{CFH}, t_{CFL}	CFG		tsys + 200		ns
DFG input high and low level widths	t_{DFH}, t_{DFL}	DFG		1000/fc + 200		ns
DPG minimum pulse width	t_{DPW}	DPG		50		ns
DPG minimum removal time	trem	DPG		50		ns
$\overline{\text{PBCTL}}$ input high and low level widths	t_{CTH}, t_{CTL}	$\overline{\text{PBCTL}}$	tsys = 2000/fc	tsys + 200		ns
EXI input high and low level widths	t_{EIH}, t_{EIL}	EXI0 EXI1	tsys = 2000/fc	tsys + 200		ns

Note) tsys indicates three values according to the contents of the clock control register (address ; 00FF$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

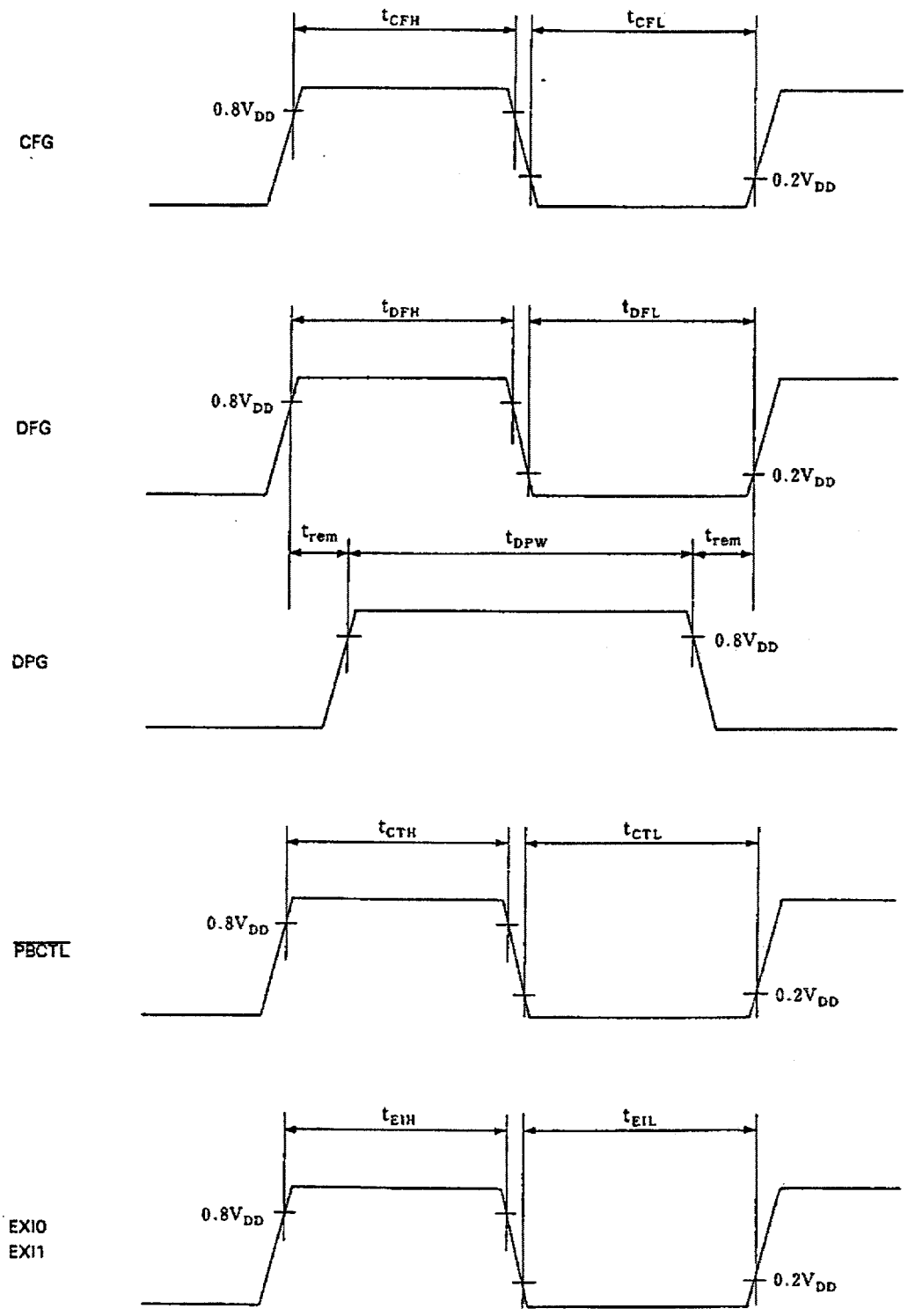


Fig. 9 Others timing

(7) Memory extension mode and microprocessor mode input/output timing

Ta = − 20 °C to + 75 °C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, fc = 8MHz (t_{CYC} = 250ns)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Control clock output (C) high and low level widths	t_{CWL}, t_{CWH}	C	Fig. 10	90		ns
High address (A15 to A8) output delay time	t_{CAHD}	A15 to A8			80	ns
Low address (A7 to A0) output delay time	t_{CALD}	A7 to A0			80	ns
Data (D7 to D0) output delay time	t_{CWD}	D7 to D0			200	ns
Data (D7 to D0) output hold time	t_{WDHD}				15	ns
Data (D7 to D0) input setup time	t_{RDS}			80		ns
Data (D7 to D0) input hold time	t_{RDHD}			15		ns
Read pulse ($\overline{RD}$) output delay time	t_{RDD}	$\overline{RD}$			90	ns
Write pulse ($\overline{WD}$) output delay time	t_{WRD}	$\overline{WR}$			130	ns
Read/write pulse (R/$\overline{W}$) output delay time	t_{RWD}	R/$\overline{W}$			50	ns
Sync pulse ($\overline{SYNC}$) output delay time	t_{SYD}	$\overline{SYNC}$			50	ns

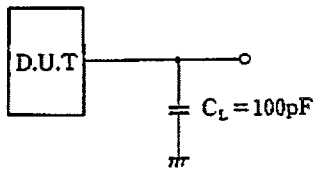


Fig. 10 Load condition

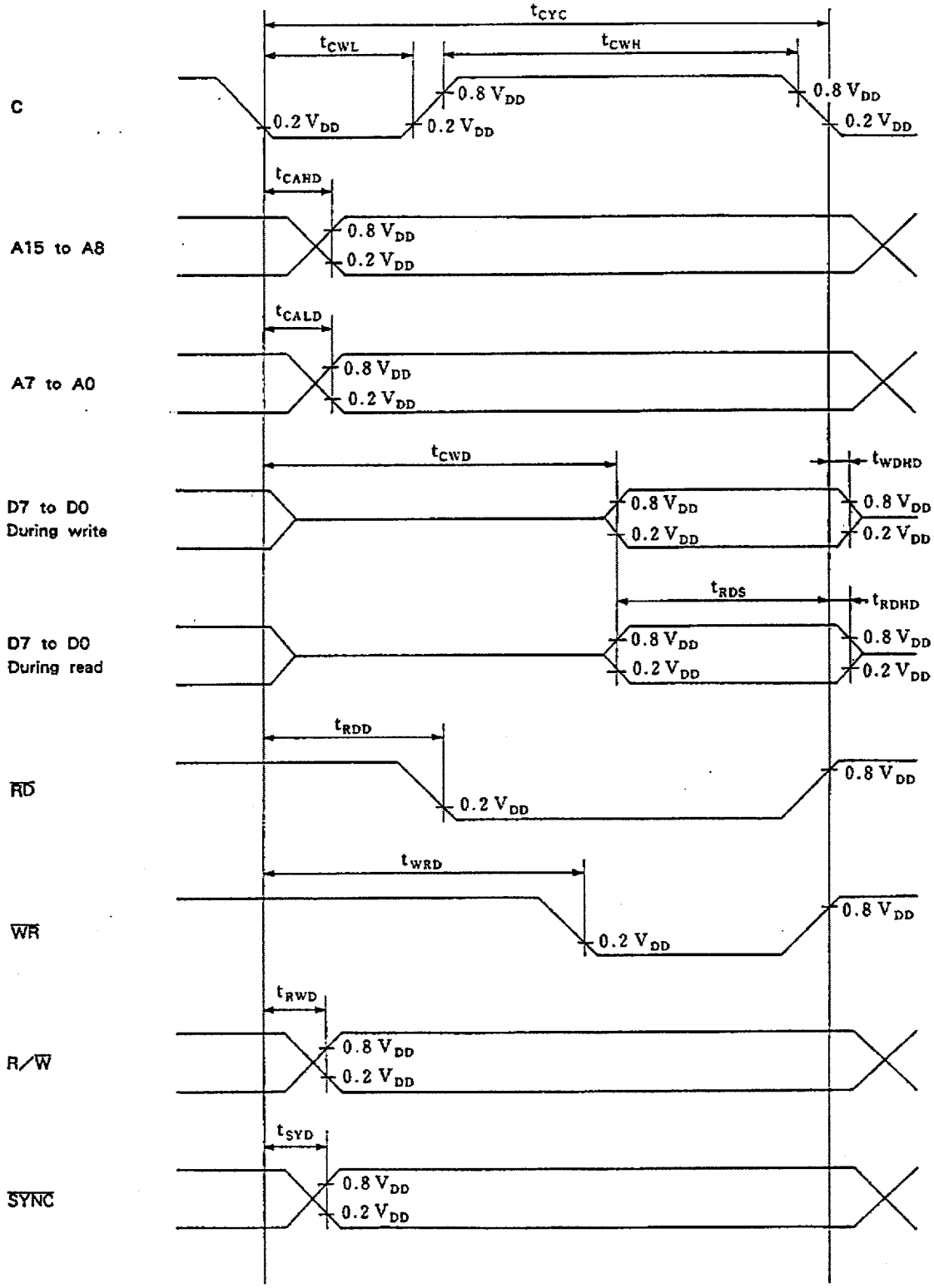


Fig. 11 Memory extension mode, microprocessor mode I/O timing

(8) Bus hold timing Ta = −20°C to +75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, fc = 8MHz

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Bus request ($\overline{BRQ}$) setup time	t_{BRDS}	$\overline{BRQ}$	Fig. 12	100		ns
Bus acknowledge ($\overline{BAK}$) delay time	t_{SYBA}	$\overline{BAK}$			50	ns
Bus acknowledge ($\overline{BAK}$) releasing delay time	t_{BRBA}				220	ns
Bus line, control signal releasing delay time	t_{BRAD}	A15 to A0 D7 to D0 $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$			210	ns

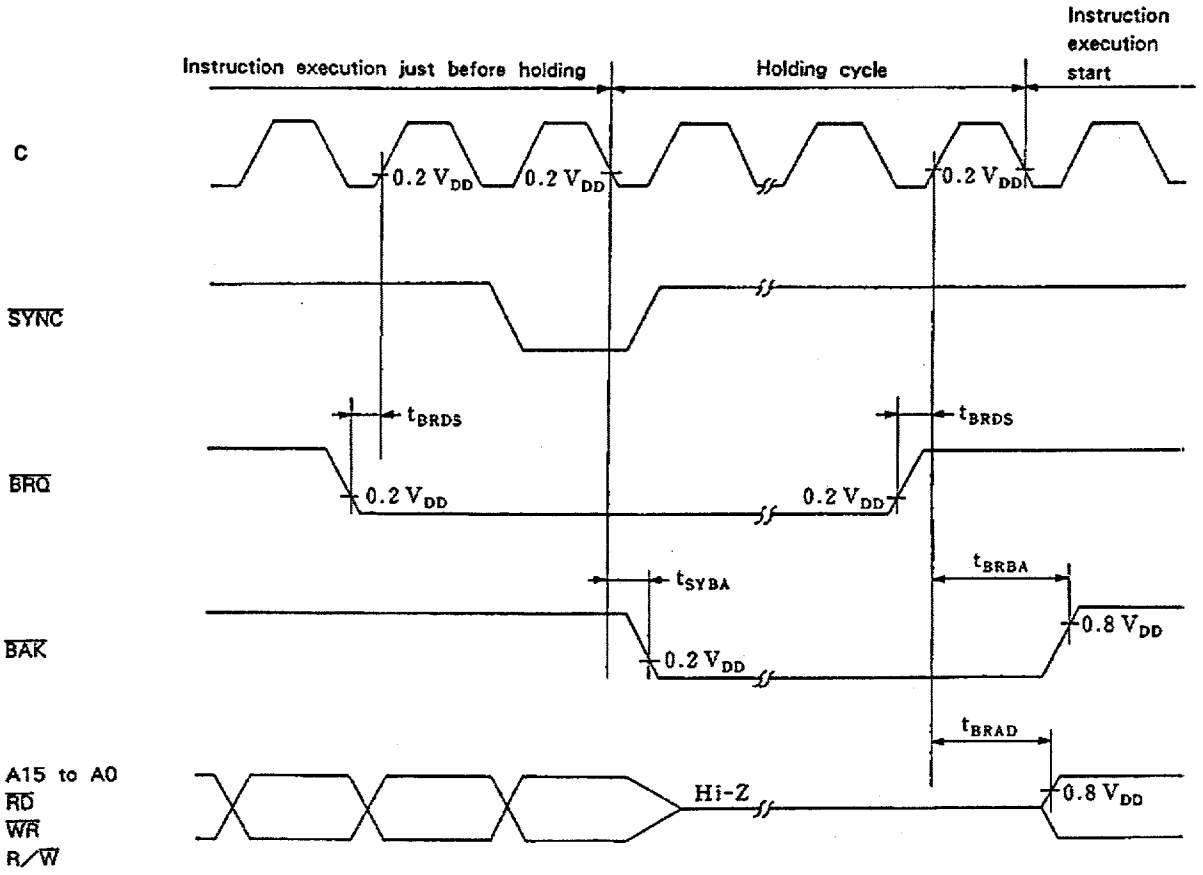
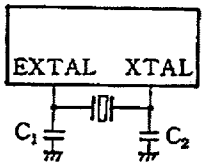


Fig. 12 Bus hold timing

Fig. 13 shows recommended circuits and oscillators.

Use the trimmer capacitor to C1, in the case of accurate adjustment of the oscillation frequency.

1.



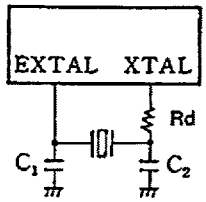
Ceramic resonator

Manufacturer	Model	Frequency range (MHz)	C1 (pF)	C2 (pF)
MURATA MFG CO., LTD.	CSA6.00MG010	6.00	100	100
	CSA8.00MT	8.00	30	30

Crystal oscillator

Manufacturer	Model	Frequency range (MHz)	C1 (pF)	C2 (pF)
FUJI SANGYO CO., LTD.	HC-49/U-03	6.00	12	12
		8.00	12	12
KINSEKI LTD.	HC-49/U-S	6.00	15	15
		8.00	15	15

2.



Manufacturer	Model	Frequency range (MHz)	C1 (pF)	C2 (pF)	Rd (kΩ)
CITIZEN WATCH CO., LTD.	CSA-309	6.144	5	5	1
		8.00	5	5	1

About the details of oscillators, please inquire the makers or the agencies.

Fig. 13 Recommended oscillation circuit

Mask option table

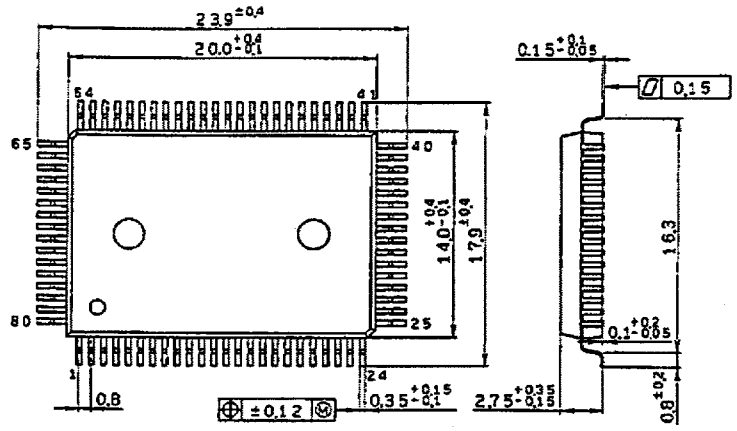
Item		
Reset pin pull-up resistor	Non-existent	Exsistent
Power on reset circuit	Non-existent	Exsistent
Input circuit format (Fig.1)	C-MOS schmitt	TTL schmitt

Note) In PG4/SYNC0 pin and PG5/SYNC1 pin, the input circuit format can be selected to every pin.

Package Outline

Unit : mm

80pin QFP (Plastic) 1.6g



SONY NAME	QFP-80P-L01
EIAJ NAME	*QFP080-P-1420-A
JEDEC CODE	———