Clock Pulse Generator/Driver

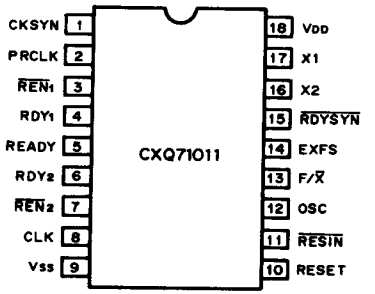
Description

The CXQ71011 is a clock pulse generator/driver for microprocessors and their peripherals with high speed CMOS technology.

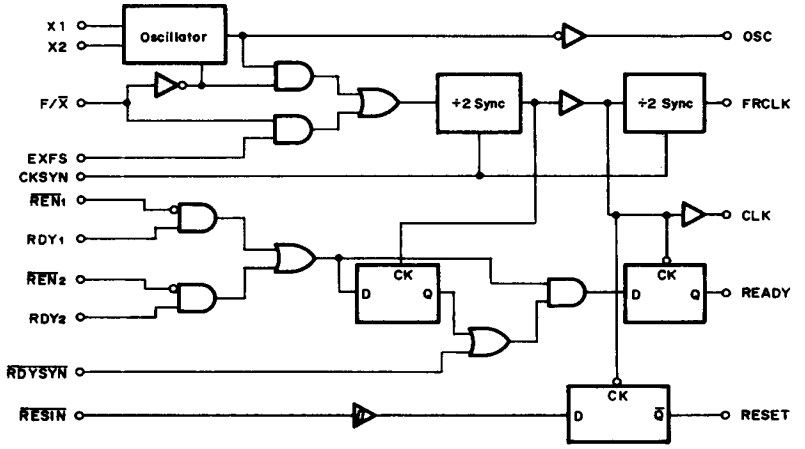
Features

- Clock pulse generator/driver for CXQ70108/70116 CPUs and their peripherals
- Frequency source can be a crystal or an external clock
- Internal frequency source power-down mode available when external clock is used ($F/\overline{X}$='H')
- Reset signal with Schmitt-trigger circuit for CPU or peripherals
- Bus ready signal with two-bus system synchronization
- Clock synchronization with other CXQ71011s
- CMOS technology
- +5V single power supply
- 18-pin plastic DIP (300 mil)
- NEC μPD71011 compatible

Pin Configuration (Top View)



Block Diagram



Pin Identification

No.	Symbol	Direction	Function
1	CKSYN	In	Clock synchronization input
2	PRCLK	Out	Peripheral clock output
3	$\overline{REN_1}$	In	Bus ready enable input 1
4	RDY_1	In	Bus ready input 1
5	READY	Out	Ready output
6	RDY_2	In	Bus ready input 2
7	$\overline{REN_2}$	In	Bus ready enable input 2
8	CLK	Out	Processor clock output
9	V_{SS}		Ground
10	RESET	Out	Reset output
11	$\overline{RESIN}$	In	Reset input
12	OSC	Out	Oscillator output
13	F/$\overline{X}$	In	External frequency source/crystal select
14	EXFS	In	External frequency source input
15	$\overline{RDYSYN}$	In	Ready synchronization select
16	X2	In	Crystal input
17	X1	In	Crystal input
18	V_{DD}		Power supply

Pin Functions

X1, X2 [Crystal Inputs]

A crystal is connected to these inputs to generate clocks for a CPU and its peripherals. The crystal frequency should be two times the frequency of CLK.

EXFS [External Frequency Source Input]

EXFS is external frequency input in the external frequency source mode (F/$\overline{X}$='H'). A square TTL-level clock signal of two times the frequency of CLK output should be used for the source.

F/$\overline{X}$ [Frequency/Crystal Select]

F/$\overline{X}$ selects either the external frequency source or the crystal as the source of the CLK output. When F/$\overline{X}$ is low, CLK is generated from the crystal connected to X1 and X2. When F/$\overline{X}$ is high, CLK is generated from an external TTL-level frequency input on the EXFS pin and at the same time, the internal oscillation circuit will go into the power-down mode.

CLK [Processor Clock]

CLK supplies a 50% duty cycle clock to drive the CPU and its peripherals on the local bus. CLK has a half frequency of crystal or EXFS input. The CLK output is +0.4V higher than the other outputs.

PRCLK [Peripheral Clock]

PRCLK supplies a 50% duty cycle clock at one-half the frequency of CLK to drive peripheral devices.

OSC [Oscillator]
OSC outputs a TTL-level signal at the same frequency as the crystal input.

CKSYN [Clock Synchronization]
CKSYN synchronizes one CXQ71011 to other CXQ71011s. A high level at CKSYN resets the internal counter, and a low level enables it to count. CKSYN needs to be externally synchronized to EXFS. When using the crystal oscillator, CKSYN needs to be stopped to ground.

$\overline{\text{RESIN}}$ [Reset Input]
This Schmitt trigger input generates the RESET output. An RC connection can be used to provide power-on-reset.

RESET [Reset]
This output is a reset signal for the CPU.

RDY_1, RDY_2 [Bus Ready]
A peripheral device sends RDY_1 or RDY_2 to signal that the data on the system bus has been received or is ready to be sent. $\overline{REN}_1$ and $\overline{REN}_2$ control the RDY_1 and RDY_2 signals.

$\overline{REN}_1$, $\overline{REN}_2$ [Bus Ready Enable]
$\overline{REN}_1$ and $\overline{REN}_2$ qualify their respective RDY inputs.

$\overline{\text{RDYSYN}}$ [Ready Synchronization Select]
$\overline{\text{RDYSYN}}$ selects the mode of READY signal synchronization. A low-level signal makes the synchronization a two-step process. This is used when RDY_1 and RDY_2 inputs are not synchronized to CLK. A high-level signal makes synchronization a one-step process. This is used when RDY_1 and RDY_2 are synchronized to CLK. See Block Diagram.

READY [Ready]
The READY signal to the processor is synchronized by the RDY inputs to the processor CLK. READY is cleared after the guaranteed hold time of the processor.

Absolute Maximum Ratings

($Ta=25°C$, $V_{SS}=0V$)

Parameter	Symbol	Rating Value	Unit
Power supply voltage	V_{DD}	−0.5 to +7.0	V
Input voltage	V_I	−1.0 to V_{DD}+1.0	V
Output voltage	V_O	−0.5 to V_{DD}+0.5	V
Power dissipation	P_{DMAX}	500	mW
Operating temperature	Topr	−40 to +85	°C
Storage temperature	Tstg	−65 to +150	°C

Comment: Exposing the device to stresses above those listed in the absolute maximum ratings could cause permanent damage. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Characteristics

(Ta=−40 to +85°C, V_{DD}=5V±10%)

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Input voltage high	V_{IH}	2.2		V	
Input voltage high	V_{IH}	2.6		V	$\overline{RESIN}$ only
Input voltage low	V_{IL}		0.8	V	
Output voltage high	V_{OH}	V_{DD}−0.8		V	I_{OH}=−4 mA
Output voltage high	V_{OH}	V_{DD}−0.4		V	CLK, I_{OH}=−4 mA
Output voltage low	V_{OL}		0.45	V	I_{OL}=4 mA
Input current leakage	I_{IL}	−1.0	1.0	μA	
$\overline{RDYSYN}$ input current	I_I	−400	1.0	μA	
$\overline{RESIN}$ input hysteresis	V_H	0.25		V	
Power supply current (dynamic)	I_{DDdyn}		30	mA	f_{IN}=20 MHz
Power supply current (static)	I_{DD}		200	μA	

Capacitance

(Ta=25°C, V_{DD}=+5V)

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Input capacitance	C_{IN}		12	pF	f_C=1 MHz

AC Characteristics

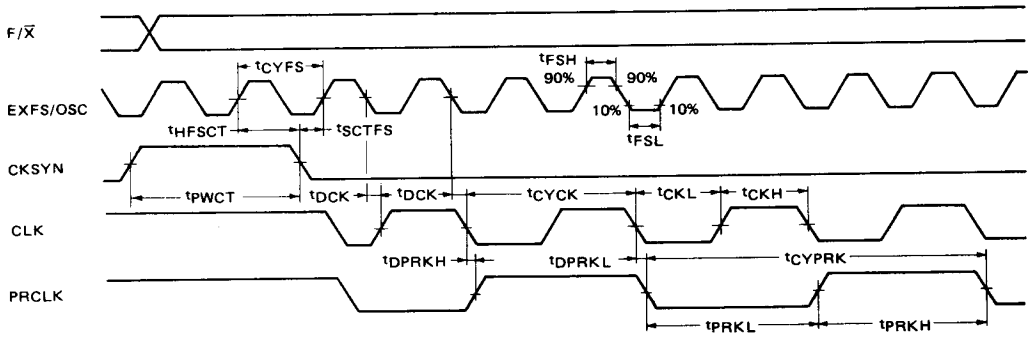
(fosc=10 MHz: Ta=−40 to +85°C, V_{DD}=5V±10%
fosc=16 MHz: Ta=−10 to +70°C, V_{DD}=5V±5%)

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
EXFS cycle time	t_{CYFS}	50		ns	
EXFS high	t_{FSH}	20		ns	90%—90% V_{IN}
EXFS low	t_{FSL}	20		ns	10%—10% V_{IN}
OSC frequency	fosc	8	20	MHz	
CKSYN width	t_{PWCT}	2t_{CYFS}		ns	
CKSYN hold for EXFS (active)	t_{HFSCT}	20		ns	
CKSYN setup (inactive)	t_{SCTFS}	20		ns	
CLK cycle time	t_{CYCK}	125		ns	
CLK high	t_{CKH}	50		ns	Test point 3.0V, fosc=16 MHz
		80		ns	Test point 3.0V, fosc=10 MHz

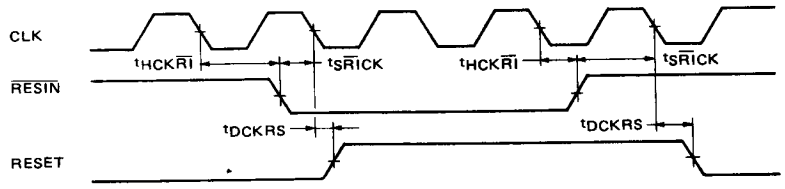
Parameter	Symbol	Min.	Max.	Unit	Test Conditions
CLK low	t_{CKL}	60		ns	Test point 1.5V, fosc=16 MHz
		90		ns	Test point 1.5V, fosc=10 MHz
CLK rise time	t_{RCK}		8	ns	Test point 1.5V to 3.0V, fosc=16 MHz
			10	ns	Test point 1.5V to 3.0V, fosc=10 MHz
CLK fall time	t_{FCK}		7	ns	Test point 3.0V to 1.5V, fosc=16 MHz
			10	ns	Test point 3.0V to 1.5V, fosc=10 MHz
OSC to CLK ↑ delay	t_{DCK}	2	30	ns	
OSC to CLK ↓ delay	t_{DCK}	−6	28	ns	
PRCLK cycle time	t_{CYPRK}	250		ns	
PRCLK high	t_{PRKH}	$t_{CYCK}-20$		ns	
PRCLK low	t_{PRKL}	$t_{CYCK}-20$		ns	
CLK ↓ to PRCLK ↑ delay	t_{DPRKH}		22	ns	
CLK ↓ to PRCLK ↓ delay	t_{DPRKL}		22	ns	
$\overline{RESIN}$ to CLK ↓ setup	$t_{S\overline{RI}CK}$	65		ns	
CLK ↓ to $\overline{RESIN}$ hold	$t_{HCK\overline{RI}}$	20		ns	
CLK ↓ to RESET delay	t_{DCKRS}		40	ns	
$\overline{REN}_{1,2}$ to $RDY_{1,2}$ setup	$t_{S\overline{RE}RY}$	15		ns	
CLK ↓ to $\overline{REN}_{1,2}$ hold	$t_{HCK\overline{RE}}$	0		ns	
$RDY_{1,2}$ to CLK ↓ setup	t_{SRYCK}	35		ns	$\overline{RDYSYN}$ high
$RDY_{1,2}$ to CLK ↑ setup	t_{SRYCK}	35		ns	$\overline{RDYSYN}$ low
CLK ↓ to $RDY_{1,2}$ hold	t_{HCKRY}	0		ns	
$\overline{RDYSYN}$ ↑ to CLK ↓ setup	$t_{S\overline{RYS}CK}$	50		ns	
CLK ↓ to $\overline{RDYSYN}$ ↓ hold	$t_{HCK\overline{RYS}}$	0		ns	
CLK ↓ to READY ↑ output delay	t_{DCKRDY}		8	ns	
CLK ↓ to READY ↓ output delay	t_{DCKRDY}		8	ns	
Input rise time	t_{RI}		20	ns	0.8V to 2.0V
Input fall time	t_{FI}		12	ns	2.0V to 0.8V
Output rise time	t_{RO}		20	ns	0.8V to 2.0V
Output fall time	t_{FO}		12	ns	2.0V to 0.8V

Timing Waveforms

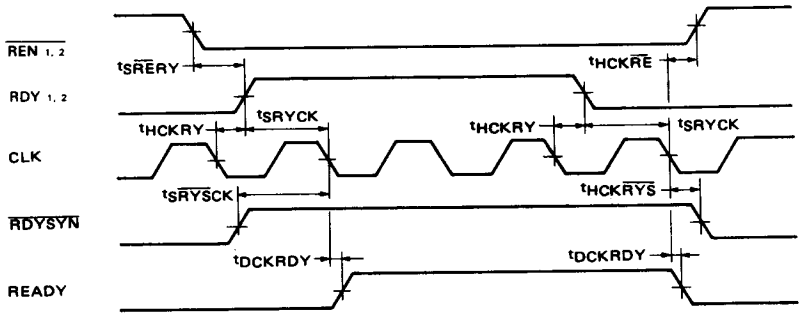
Clock Output



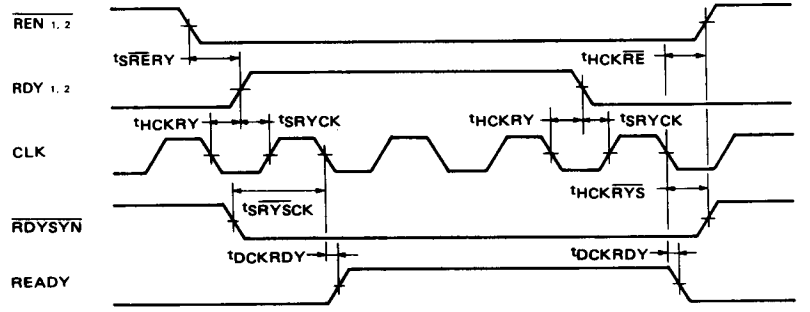
RESET Output



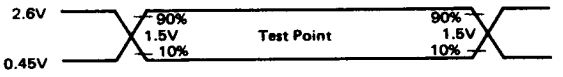
READY Output (RDYSYN High)



READY Output (RDYSYN Low)

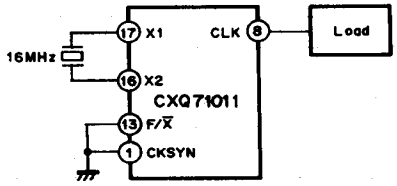


Test Circuit for CLK High or Low Time

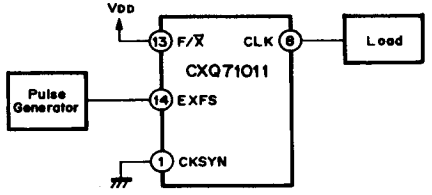


Test Circuits

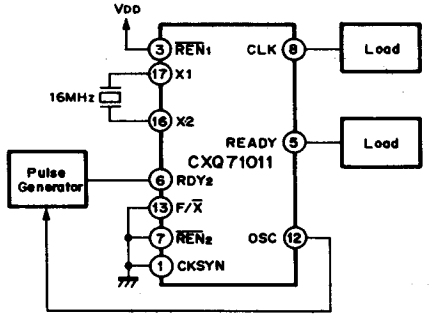
Test Circuit for CLK High or Low Time (in Crystal Oscillation Mode)



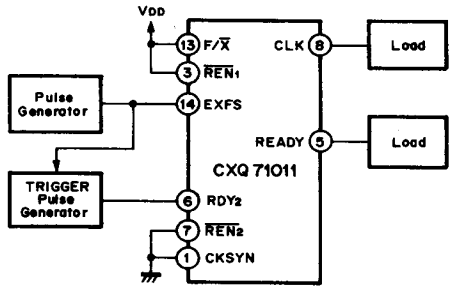
Test Circuit for CLK High or Low Time (in EXFS Oscillation Mode)



Test Circuit for CLK to READY (in Crystal Oscillation Mode)



Test Circuit for CLK to READY (in EXFS Oscillation Mode)



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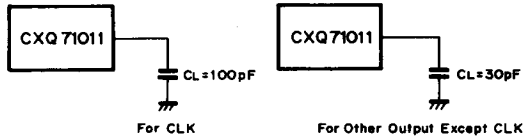

Package Outline

Unit: mm