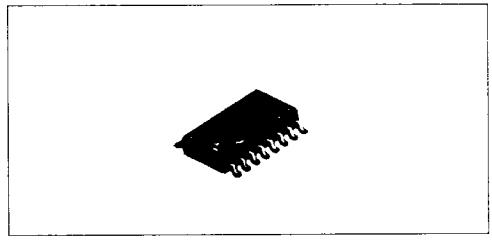
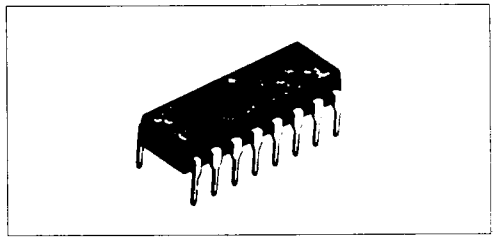
# 6-bit 20MSPS Video A/D Converter (CMOS)

## Description

The CXD1172A is a 6-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low power consumption at a maximum conversion speed of 20MSPS minimum, 35MSPS is typical.



CXD1172AM 16pin SOP (Plastic)



CXD1172AP 16pin DIP (Plastic)

## Features

- Resolution 6-bit ± 1/2 LSB
- Max. sampling frequency 20MSPS
- Low power consumption
  40mW (at 20MSPS Typ.)
  (Reference current excluded)
- Built-in sampling and hold circuit.
- Power supply 5V single
- Low input capacity 4pF
- Reference impedance 300Ω (Typ.)
- Pin replaceable with CXD1172.

## Structure

Silicon gate CMOS monolithic IC.

## Applications

TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

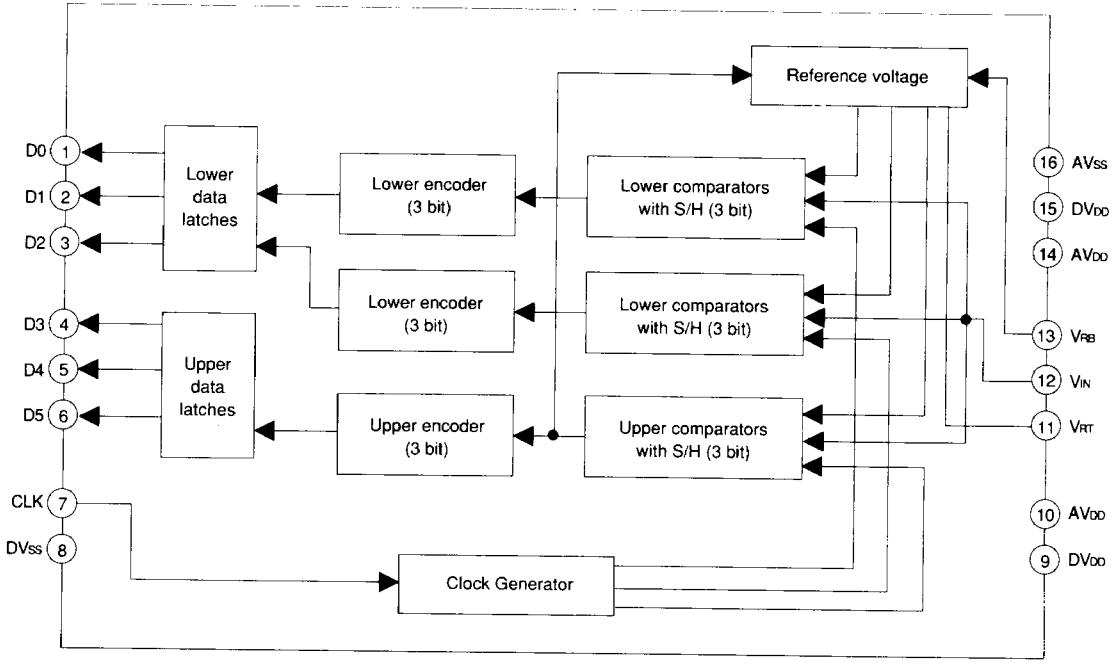
## Absolute Maximum Ratings (Ta=25 °C)

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | 7 | V |
| • Reference voltage | $V_{RT}$, $V_{RS}$ | $V_{DD}$ to $V_{SS}$ | V |
| • Analog Input voltage | $V_{IN}$ | $V_{DD}$ to $V_{SS}$ | V |
| • Digital Input voltage | $C_{LK}$ | $V_{DD}$ to $V_{SS}$ | V |
| • Digital output voltage | $V_{CH}$, $V_{OL}$ | $V_{DD}$ to $V_{SS}$ | V |
| • Storage temperature | Tstg | -55 to +150 | °C |

## Recommended Operating Conditions

| | | | |
|---|---|---|---|
| • Supply voltage | $AV_{DD}$, $AV_{SS}$ | 4.75 to 5.25 | V |
| | $DV_{DD}$, $DV_{SS}$ | 4.75 to 5.25 | |
| • Reference input voltage | $V_{RB}$ | 0 to 4.1 | V |
| | $V_{RT}$ | 0.9 to 5.0 | V |
| | VRT-VRB | 0.9 to $AV_{DD}$ | V |
| • Analog input voltage | $V_{IN}$ | $V_{RB}$ to $V_{RT}$ | |
| • Clock pulse width | $T_{PWI}$ | 25(min.) | ns |
| | $T_{PWO}$ | 25(min) | ns |
| • Operating temperature | $T_{OPR}$ | -20 to +75 | °C |

## Block Diagram and Pin Configuration

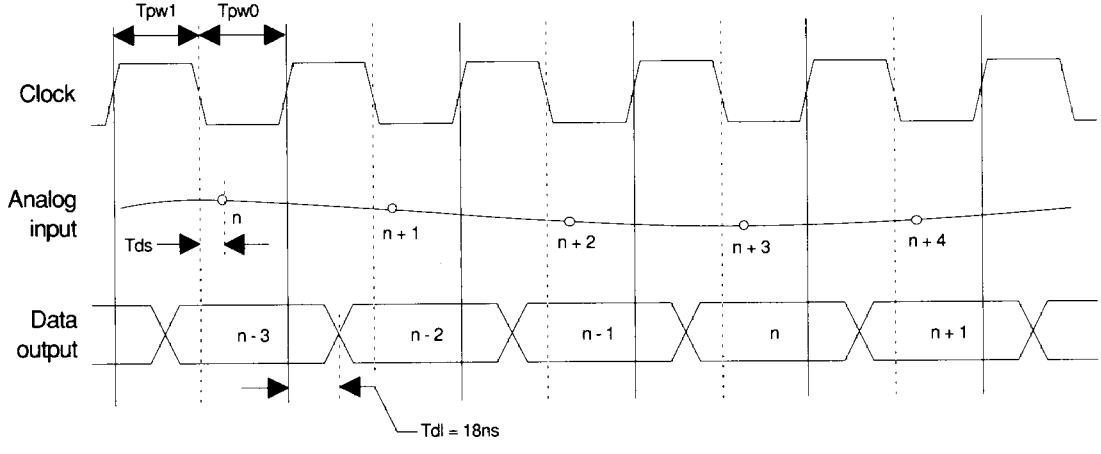


## Digital Output

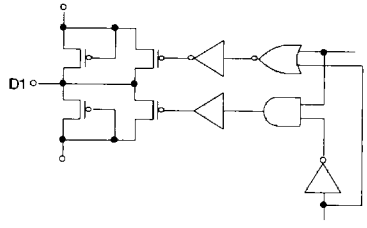
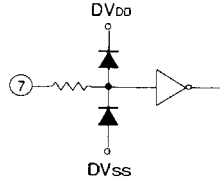
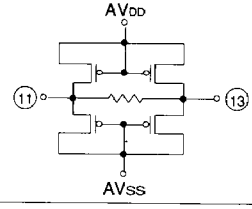
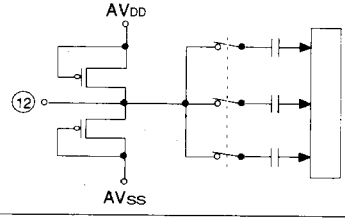
Compatibility between Analog input voltage and the digital output code is indicated in the chart below.

| Input Signal Voltage | Step | Digital Output Code | | | | | |
|---|---|---|---|---|---|---|---|
| | | MSB | | | | | LSB |
| VRT | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 31 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 32 | 0 | 1 | 1 | 1 | 1 | 1 |
| VRB | 63 | 0 | 0 | 0 | 0 | 0 | 0 |

## Timing Chart 1



## Pin Description and Equivalent Circuits

| No. | Symbol | Equivalent Circuit | Description |
|---|---|---|---|
| 1 to 6 | $D_0$ to $D_5$ |  | $D_0$ (LSB) to $D_5$ (MSB) output |
| 7 | CLK |  | Clock input |
| 8 | $DV_{SS}$ | | Digital GND |
| 9, 15 | $DV_{DD}$ | | Digital +5V |
| 10, 14 | $AV_{DD}$ | | Analog +5V |
| 11 | $V_{RT}$ |  | Reference voltage (top) |
| 13 | $V_{RB}$ | | Reference voltage (bottom) |
| 12 | $V_{IN}$ |  | Analog input |
| 16 | $AV_{SS}$ | | Analog GND |

3

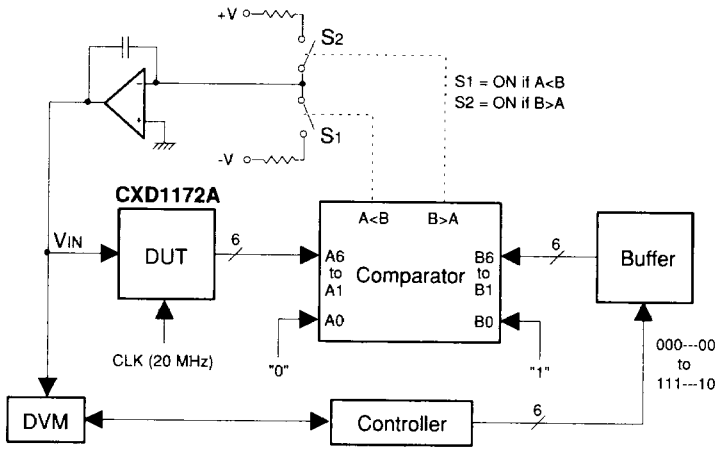
## Electrical Characteristics

$V_{CC}$ = +5V, $V_{RB}$ = 1.0V, $V_{RT}$ = 2.0V, Ta = 25°C

| Item | Symbol | Conditions | Min. | Type | Max. | Unit |
|---|---|---|---|---|---|---|
| Maximum Conversion Speed | $F_C$ | VIN = 1.0V to 2.0V<br>FIN = 1KHz ramp | 20 | 35 | | MSPS |
| Supply Current | $I_{DD}$ | FC = 20MSPS<br>NTSC ramp wave input | | 8 | | mA |
| Reference Pin Current | $I_{REF}$ | | | 3.3 | | mA |
| Analog Input Band (-1dB) | BW | | | 20 | | MHz |
| Analog Input Capacitance | $C_{IN}$ | $V_{IN}$ = 1.5V + 0.07Vrms | | 4 | | pF |
| Reference Resistance ($V_{RT}$ to $V_{RB}$) | $R_{REF}$ | | | 300 | | Ω |
| Offset Voltage | $E_{OT}$ | | | -20 | | mV |
| | $E_{OB}$ | | | 30 | | |
| Digital Input Voltage | $V_{IH}$ | | 4.0 | | | V |
| | $V_{IL}$ | | | | 1.0 | |
| Digital Input Current | $I_{IH}$ | $V_{DD}$ = max., $V_{IH}$ = $V_{DD}$ | | | 5 | μA |
| | $I_{IL}$ | $V_{DD}$ = max., $V_{IL}$ = 0V | | | 5 | |
| Digital Output Delay | $I_{OH}$ | $V_{DD}$ = min., $V_{OH}$ = $V_{DD}$-0.5V | -1.5 | | | mA |
| | $I_{OL}$ | $V_{DD}$ = min., $V_{OL}$ = 0.4V | 4.0 | | | |
| Output Data Delay | $T_{DL}$ | | | 18 | 30 | ns |
| Integral Non-linearity | $E_L$ | FC = 20MSPS<br>$V_{IN}$ = 1.0V to 2.0V | | ±0.3 | ±0.5 | LSB |
| Differential Non-linearity | $E_D$ | FC = 20MSPS<br>$V_{IN}$ = 1.0V to 2.0V | | ±0.3 | ±0.5 | LSB |
| Differential Gain Error | DG | NTSC 40 IRE mod<br>Ramp, FC = 14.3MSPS | | 10 | | % |
| Differential Phase Error | DP | | | 1.0 | | deg |
| Aperture Jitter | Taj | | | 40 | | ps |
| Sampling Delay | Tsd | | | 4 | | ns |

## Electrical Characteristics Test Circuit

Integral non-linearity error
Differenvtial non-linearity Test Circuit
Offset voltage

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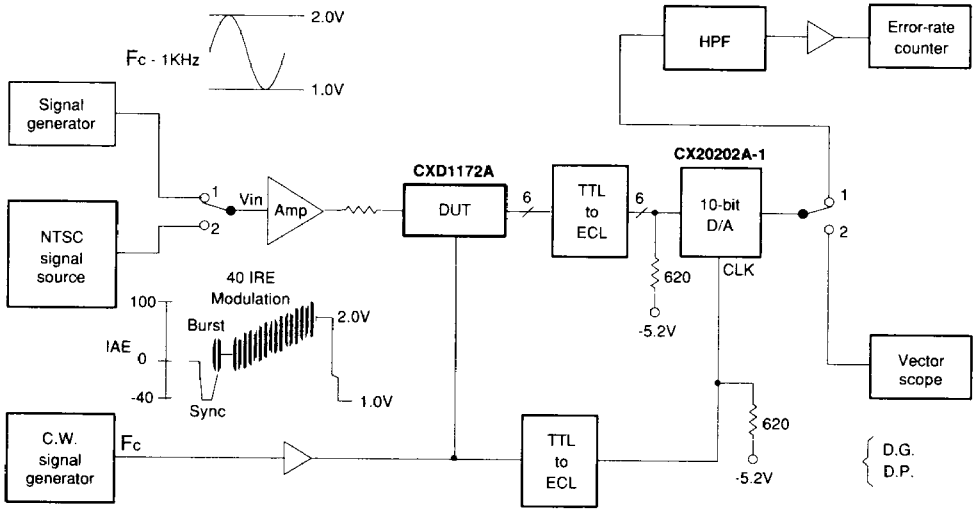
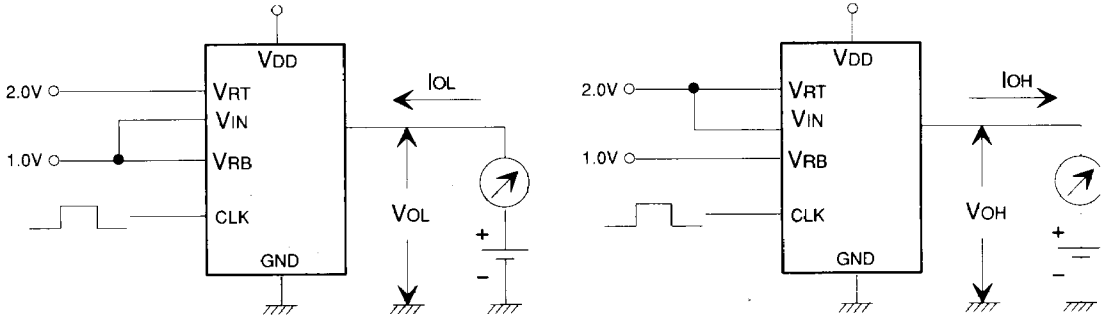
Maximum operational speed
Differential gain error Test Circuit
Differential phase error

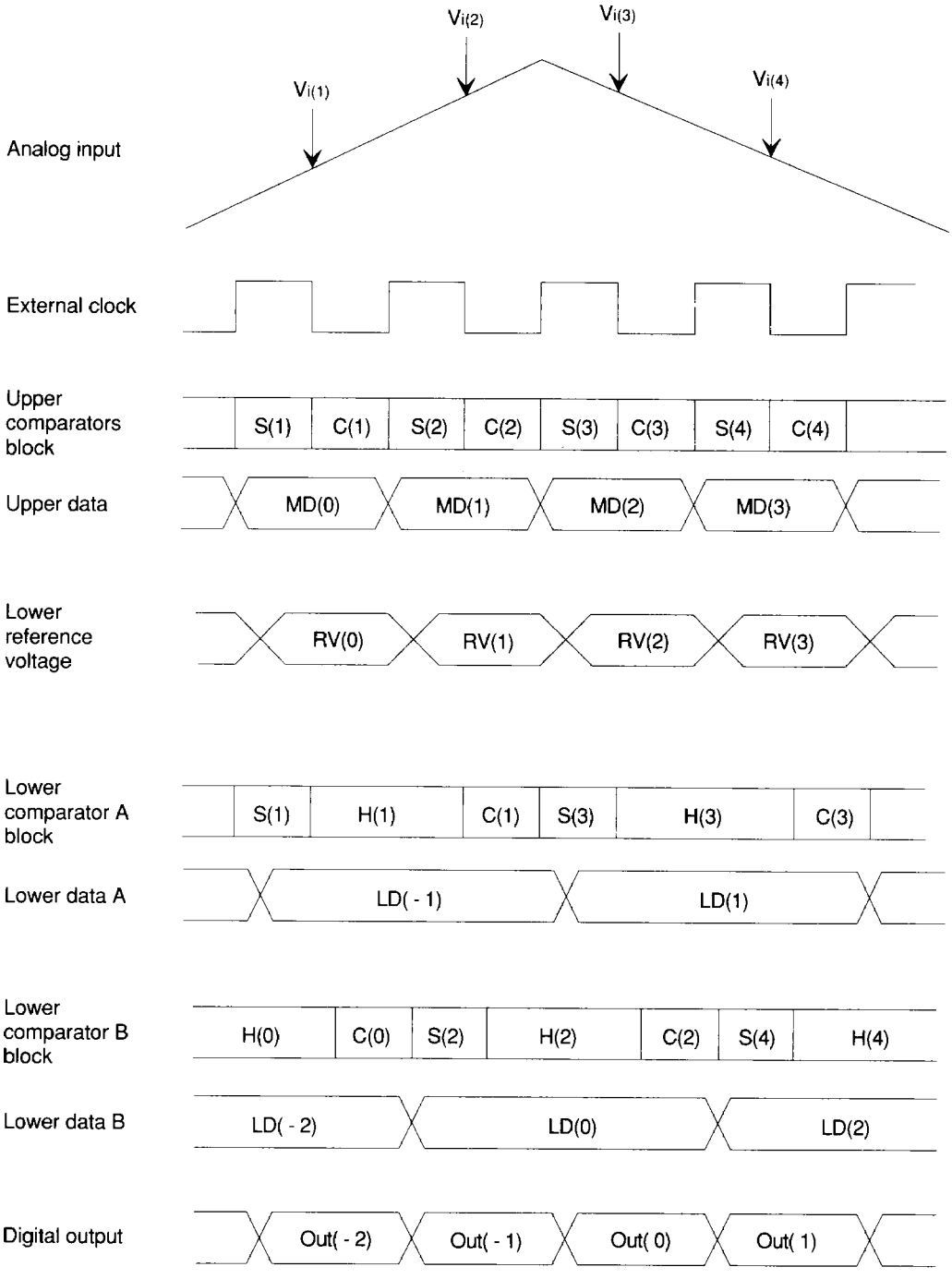


Electrical Characteristics Test Circuit

Digital output current test circuit



## Timing Chart 2

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## Operation (See Black Diagram and Timing Chart)

1. CXD1172AM/AP is a 2-step parallel system A/D converter featuring a 3-bit upper comparators group and 2 lower comparators groups of 3-bit each. The reference voltage that is equal to the voltage between VRT-VRB/8 is constantly applied to the upper 3-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.

2. This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S.H.C. symbols. That is input sampling (auto zero) mode. Input hold mode and comparison mode.

3. The operation of respective parts is as indicated in the chart. For instance input voltage VI (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.

   The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

## Operation Notes

1. $V_{DD}$, $V_{SS}$

   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog VDD pins, use a ceramic capacitor of about 0.1 F set as close as possible to the pin to bypass to the respective GND's.

2. Analog Input

   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. that may be prevented by inserting a resistance of about 100 W in series between the amplifier output and A/D input.

3. Clock Input

   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

4. Reference Input

   Voltage between $V_{RT}$ to $V_{RB}$ is compatible with the dynamic range of the analog input. Bypassing $V_{RT}$ and $V_{RB}$ pins to GND, by means of a capacitor about 0.1 mF, stable characteristics are obtained.

5. Timing

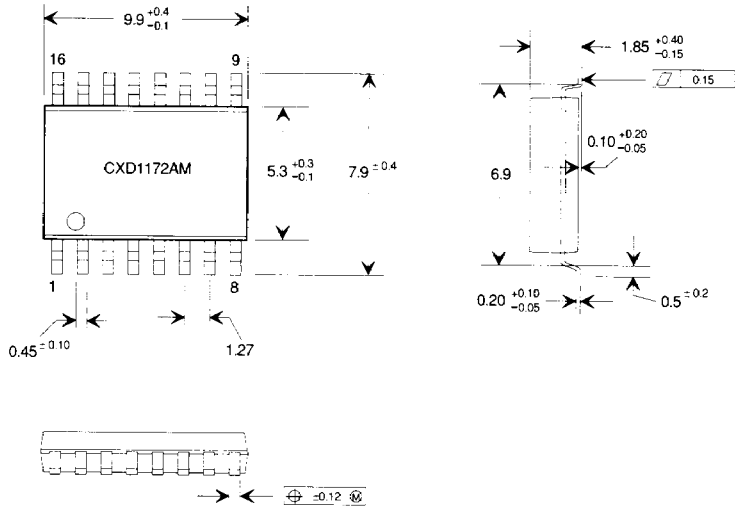
   Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

6. About Latch Up

   It is necessary that $AV_{DD}$ and $DV_{DD}$ pins be the common source of power supply. This is to avoid latch up due to the voltage difference between $AV_{DD}$ and $DV_{DD}$ pins when power is ON. See "For latch up prevention" of CXD1172AP/CXA1106P PCB description (Page 6. 7).

## Package Outline Unit: mm

CXD1172AM 16pin SOP (Plastic) 300mil 0.2g

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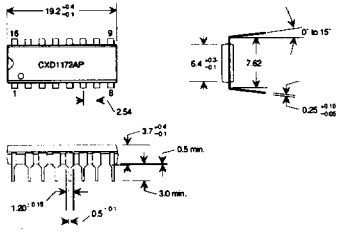
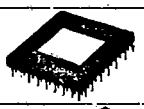
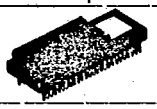
## Package Outline Unit: mm

CXD1172AP 16pin DIP (Plastic) 300mil 1.0g



T-90-20

## Sony Package Product Name

| Type | | Package name | | Package | Features | | | |
|---|---|---|---|---|---|---|---|---|
| | | Symbol | Description | | Material* | Lead pitch | Lead shape | Lead pull out direction |
| Inserted | Standard | DIP | DUAL IN LINE PACKAGE |  | P C | 2.54mm (100MIL) | Through Hole Lead | 2-direction |
| | | SIP | SINGLE IN LINE PACKAGE |  | P | 2.54mm (100MIL) | Through Hole Lead | 1-direction |
| | | ZIP | ZIG ZAG IN LINE PACKAGE |  | P | 2.54mm (100MIL) Zig Zag inline | Through Hole Lead | 1-direction |
| | | PGA | PIN GRID ARRAY |  | C | 2.54mm (100MIL) | Through Hole Lead | 4-direction |
| | | PIGGY BACK | PIGGY BACK |  | C | 2.54mm (100MIL) | Through Hole Lead | 2-direction |
| | Shrink | SDIP | SHRINK DUAL IN LINE PACKAGE |  | P | 1.778mm (70MIL) | Through Hole Lead | 2-direction |
| Surface mounted | Standard flat package | QFP | QUAD FLAT PACKAGE |  | P | 1.0mm 0.8mm | Gull-Wing | 4-direction |
| | | SOP | SMALL OUTLINE PACKAGE |  | P | 1.27mm (50MIL) | Gull-Wing | 2-direction |
| | Shrink flat package | VQFP | VERY SMALL QUAD FLAT PACKAGE |  | P | 0.5mm | Gull-Wing | 4-direction |
| | | VSOP | VERY SMALL OUTLINE PACKAGE |  | P | 0.65mm | Gull Wing | 2-direction |
| | Standard chip carrier | PLCC | PLASTIC LEADED CHIP CARRIER |  | P | 1.27mm (50MIL) | J-bend | 4-direction |
| | | LCC | LEAD LESS CHIP CARRIER |  | C | 1.27mm (50MIL) | Lead less | Package side |
| | Shrink chip carrier | SPLCC (PLCC) | SHRINK PLASTIC LEADED CHIP CARRIER |  | P | 1.27mm Max. (50MIL Max.) | J-bend | 4-direction |
| | Standard 2-direction chip carrier | SOJ | SMALL OUTLINE J-LEAD PACKAGE |  | P | 1.27mm (50MIL) | J-bend | 2-direction |

*P……Plastic, C……Ceramic