CY2280-3
CY2280-2
CY2280-1

100-MHz Pentium® II Clock Synthesizer/Driver with USB and Power-Down for Mobile or Desktop PCs

Features

- **Mixed 2.5V and 3.3V operation**
- **Clock solution for Pentium® II, and other similar processor-based motherboards**
  - **— Four 2.5V CPU clocks up to 100 MHz**
  - **— Eight 3.3V synch. PCI clocks, one free-running**
  - **— Two 3.3V 48 MHz USB clocks**
  - **— Three 3.3V Ref. clocks at 14.318 MHz**
  - **— Two 2.5V APIC clocks at 14.318 MHz or PCI/2**
- **1.5–4.0 ns delay between CPU and PCI clocks (-1, -2)**
- **0-ns delay between CPU and PCI clocks (-3 device)**
- **2–4.5 ns delay between CPU and APIC clocks (-2 only)**
- **Factory-EPROM programmable output drive and slew rate for EMI optimization**
- **Factory-EPROM programmable CPU clock frequencies for custom configurations**
- **Power-down, CPU stop and PCI stop pins**
- **Low skew outputs, ≤ 175 ps between CPU clocks and between APIC clocks**
- **Available in space-saving 48-pin SSOP package**

Functional Description

The CY2280-1 is a clock synthesizer/driver for Pentium II processor-based desktop or mobile PCs requiring up to 100-MHz support. The CY2280-1 outputs four CPU clocks at 2.5V. There are eight PCI clocks, running at one-half or one-third the CPU clock frequency of 66.6 MHz and 100 MHz respectively. One of the PCI clocks is free-running. Additionally, the part outputs two 3.3V USB clocks at 48 MHz, three 3.3V reference clocks at 14.318 MHz, and two 2.5V APIC clocks at 14.318 MHz (-1, -3) or at one-half the PCI frequency (-2). The full selector guide for all options is shown below.

The CY2280 possesses power-down, CPU stop, and PCI stop pins for power management control. The signals are synchronized on-chip, and ensure glitch-free transitions on the outputs. When the CPU_STOP input is asserted, the CPU clock outputs are driven LOW. When the PCI_STOP input is asserted, the PCI clock outputs (except the free-running PCI clock) are driven LOW. When the PWR_DWN pin is asserted, the reference oscillator and PLLs are shut down, and all outputs are driven LOW.

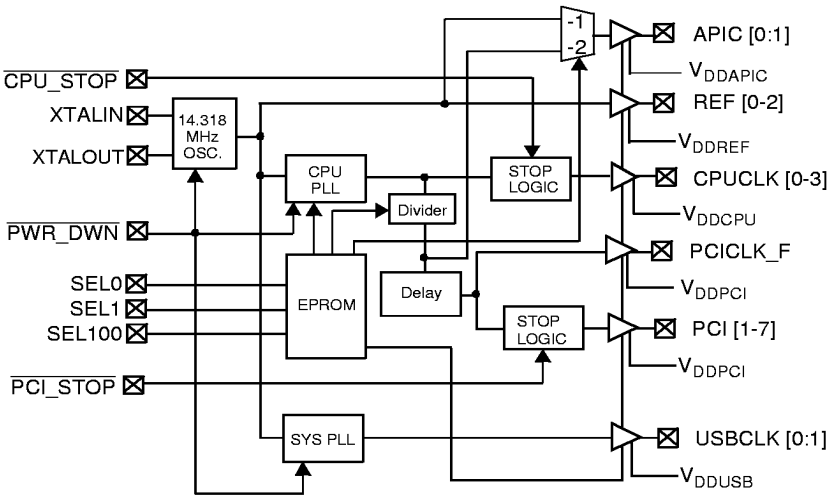
The CY2280-1 outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and factory-EPROM programmable output drive and slew-rate enable optimal configurations for EMI control.

CY2280 Selector Guide

Clock Outputs	-1	-2	-3
CPU (66, 100 MHz)	4	4	4
PCI (CPU/2, CPU/3 MHz)	8[1]	8[1]	8[1]
USB (48 MHz)	2	2	2
APIC (14.318 MHz)	2	--	2
APIC (PCI/2 MHz)	--	2	--
Ref. (14.318 MHz)	3	3	3
CPU-PCI delay	1.5–4.0 ns	1.5–4.0 ns	0 ns
CPU-APIC delay	--	2–4.5 ns	--

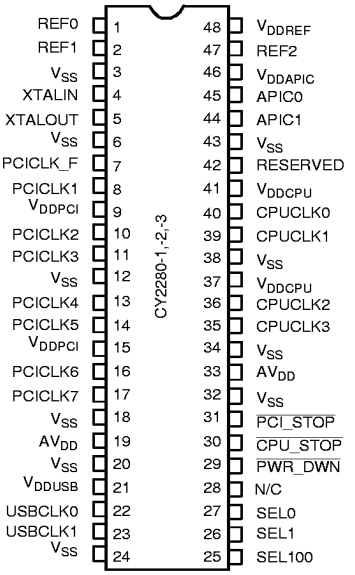
Note:
1. One free-running PCI clock.

Logic Block Diagram



Pin Configuration

SSOP
Top View



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Pin Summary

Name	Pins	Description
V_{DDPCI}	15, 9	3.3V Digital voltage supply for PCI clocks
V_{DDUSB}	21	3.3V Digital voltage supply for USB clocks
V_{DDREF}	48	3.3V Digital voltage supply for REF clocks
V_{DDAPIC}	46	2.5V Digital voltage supply for APIC clocks
V_{DDCPU}	41, 37	2.5V Digital voltage supply for CPU clocks
AV_{DD}	33, 19	Analog voltage supply, 3.3V
V_{SS}	3, 6, 12, 18, 20, 24, 32, 34, 38, 43	Ground
XTALIN[2]	4	Reference crystal input
XTALOUT[2]	5	Reference crystal feedback
$\overline{PCI\_STOP}$	31	Active LOW control input to stop PCI clocks
$\overline{CPU\_STOP}$	30	Active LOW control input to stop CPU clocks
$\overline{PWR\_DWN}$	29	Active LOW control input to power down device
N/C	28	No Connect. Can be driven HIGH or LOW.
SEL0	27	CPU frequency select input, bit 0 (see table below)
SEL1	26	CPU frequency select input, bit 1 (see table below)
SEL100	25	CPU frequency select input, selects between 100 MHz and 66.6 MHz (see table below)
CPUCLK[0:3]	40, 39, 36, 35	CPU clock outputs
PCICLK[1:7]	8, 10, 11, 13, 14, 16, 17	PCI clock outputs, at one-half or one-third the CPU frequency of 66.6 MHz or 100 MHz respectively
PCICLK_F	7	Free-running PCI clock output
APIC[0:1]	45, 44	APIC clock outputs
REF[0:2]	1, 2, 47	3.3V Reference clock outputs
USBCLK[0:1]	22, 23	USB clock outputs
RESERVED	42	Reserved

Function Table

SEL100	SEL1	SEL0	CPU/PCI Ratio	CPUCLK	PCICLK_F PCICLK	REF	APIC (-1, -3)	APIC (-2)	USBCLK
0	0	0	2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	0	1	2	Reserved	Reserved	14.318 MHz	14.318 MHz	Reserved	48 MHz
0	1	0	2	Reserved	Reserved	14.318 MHz	14.318 MHz	Reserved	48 MHz
0	1	1	2	66.66 MHz	33.33 MHz	14.318 MHz	14.318 MHz	16.67 MHz	48 MHz
1	0	0	3	TCLK/2	TCLK/6	TCLK[3]	TCLK[3]	TCLK/12[3]	TCLK/2
1	0	1	3	Reserved	Reserved	14.318 MHz	14.318 MHz	Reserved	48 MHz
1	1	0	3	Reserved	Reserved	14.318 MHz	14.318 MHz	Reserved	48 MHz
1	1	1	3	100 MHz	33.33 MHz	14.318 MHz	14.318 MHz	16.67 MHz	48 MHz

Notes:
2. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.
3. TCLK supplied on the XTALIN pin in Test Mode.

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	–195
CPUCLK	100	99.77	–2346
USBCLK	48.0	48.008	167

Power Management Logic

$\overline{\text{CPU\_STOP}}$	$\overline{\text{PCI\_STOP}}$	$\overline{\text{PWR\_DWN}}$	CPUCLK	PCICLK	PCICLK_F	Other Clocks	Osc.	PLLs
X	X	0	Low	Low	Low	Low	Off	Off
0	0	1	Low	Low	Running	Running	Running	Running
0	1	1	Low	Running	Running	Running	Running	Running
1	0	1	Running	Low	Running	Running	Running	Running
1	1	1	Running	Running	Running	Running	Running	Running

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5 to +7.0V

Input Voltage ..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation 1W

Static Discharge Voltage ..... >2000V
(per MIL-STD-883, Method 3015, like V_{DD} pins tied together)

Operating Conditions[4]

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DDPCI}, V_{DDUSB}, V_{DDREF}	Analog and Digital Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375	2.625	V
V_{DDAPIC}	APIC Supply Voltage	2.375	2.625	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK APIC, REF USB		 20 30 20 20	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Note:
4. Electrical parameters are guaranteed with these operating conditions.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs[5]			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs[5]				0.8	V
V_{OH}	High-level Output Voltage[6]	V_{DDCPU} = V_{DDAPIC} = 2.375V	I_{OH} = 12 mA	CPUCLK	2.0		V
			I_{OH} = 18 mA	APIC			
V_{OL}	Low-level Output Voltage[6]	V_{DDCPU} = V_{DDAPIC} = 2.375V	I_{OL} = 12 mA	CPUCLK		0.4	V
			I_{OL} = 18 mA	APIC			
V_{OH}	High-level Output Voltage[6]	V_{DDPCI}, AV_{DD}, V_{DDREF}, V_{DDUSB} = 3.135V	I_{OH} = 14.5 mA	PCICLK	2.4		V
			I_{OH} = 16 mA	USBCLK			
			I_{OH} = 16 mA	REF			
V_{OL}	Low-level Output Voltage[6]	V_{DDPCI}, AV_{DD}, V_{DDREF}, V_{DDUSB}= 3.135V	I_{OL} = 9.4 mA	PCICLK		0.4V	V
			I_{OL} = 9 mA	USBCLK			
			I_{OL} = 9 mA	REF			
I_{IH}	Input High Current	V_{IH} = V_{DD}			–10	+10	µA
I_{IL}	Input Low Current	V_{IL} = 0V				10	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD25}	Power Supply Current for 2.5V clocks[6]	V_{DDCPU} = 2.625V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU = 66.6 MHz				70	mA
I_{DD25}	Power Supply Current for 2.5V clocks[6]	V_{DDCPU} = 2.625V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU = 100 MHz				100	mA
I_{DD33}	Power Supply Current for 3.3V clocks[6]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Loaded Outputs				170	mA
I_{DDS}	Powerdown Current[6]	Current draw in powerdown state				500	µA

Notes:
5. Crystal Inputs have CMOS thresholds.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

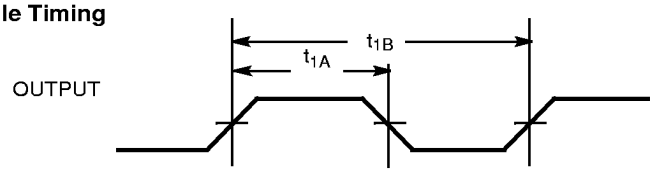
Switching Characteristics[6, 7]

Parameter	Output	Description	Test Conditions		Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle[8]	$t_1 = t_{1A} \div t_{1B}$		45	50	55	%
t_2	CPUCLK, APIC	CPU and APIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V	-1,-2 only	1.0		4.0	V/ns
				-3 only	0.8		4.0	V/ns
t_2	PCICLK	PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	-1,-2 only	1.0		4.0	V/ns
				-3 only	0.9		4.0	V/ns
t_2	USBCLK, REF	USB, REF Rising and Falling Edge Rate	Between 0.4V and 2.4V		0.5		2.0	V/ns
t_3	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V	-1,-2 only	0.4		1.6	ns
				-3 only	0.4		2.0	ns
t_4	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V	-1,-2 only	0.4		1.6	ns
				-3 only	0.4		2.0	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V			100	175	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew[9]	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	-1,-2 only	1.5		4.0	ns
				-3 only	–1		1	ns
t_7	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V				250	ps
t_8	CPUCLK, APIC	CPU-APIC Clock Skew[10]	Measured at 1.25V for 2.5V clocks	-2 only	2.0		4.5	ns
t_9	APIC	APIC-APIC Clock Skew	Measured at 1.25V			100	175	ps
t_{10}	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V	-1,-2 only		200	250	ps
				-3 only		250	350	ps
t_{11}	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			250	500	ps
t_{12}	CPUCLK, PCICLK	Power-up Time	CPU, PCI clock stabilization from power-up				3	ms

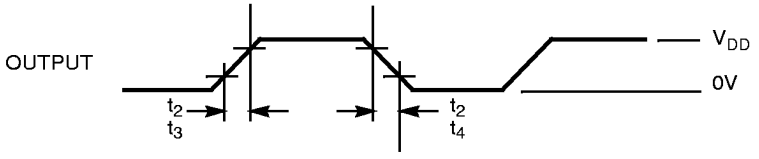
Notes:
7. All parameters specified with loaded outputs.
8. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.
9. PCI lags CPU for -1, -2 options.
10. APIC lags CPU for -2 option.

Switching Waveforms

Duty Cycle Timing

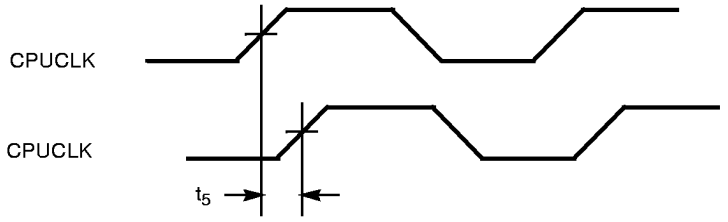


All Outputs Rise/Fall Time

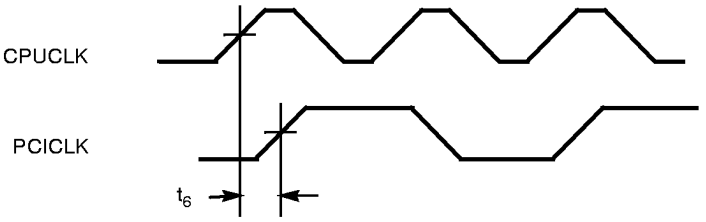


Switching Waveforms (continued)

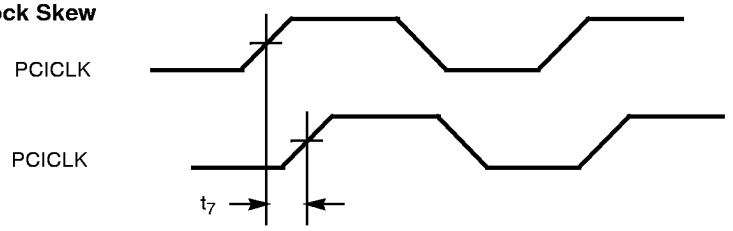
CPU-CPU Clock Skew



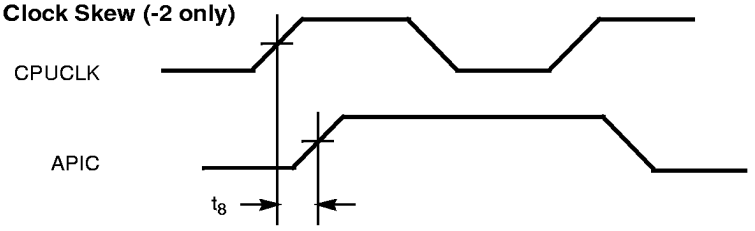
CPU-PCI Clock Skew



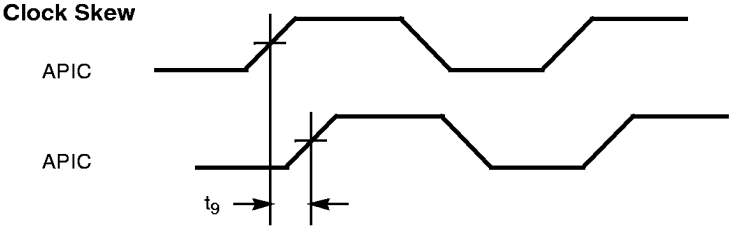
PCI-PCI Clock Skew



CPU-APIC Clock Skew (-2 only)

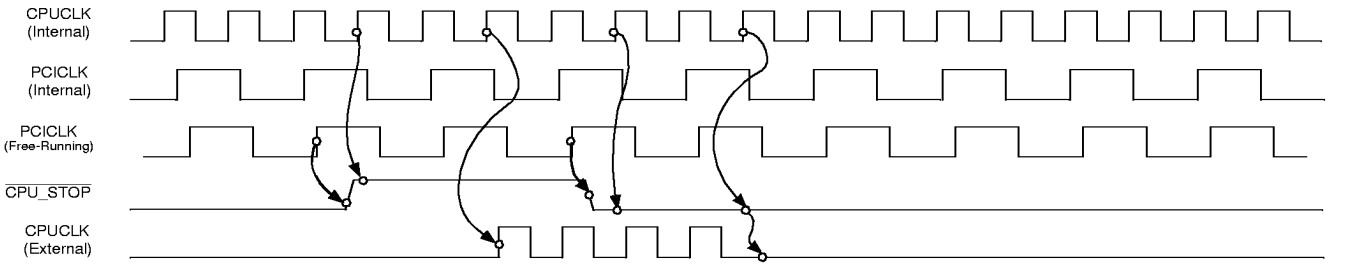


APIC-APIC Clock Skew

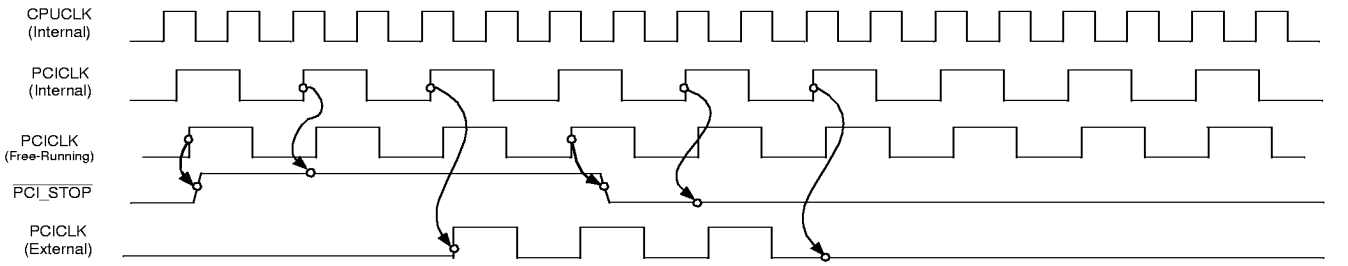


Switching Waveforms (continued)

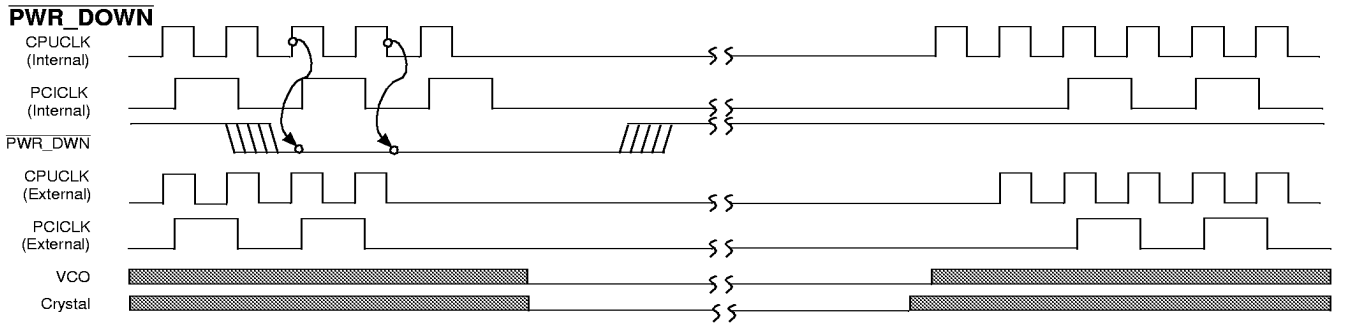
CPU_STOP



PCI_STOP



PWR_DOWN

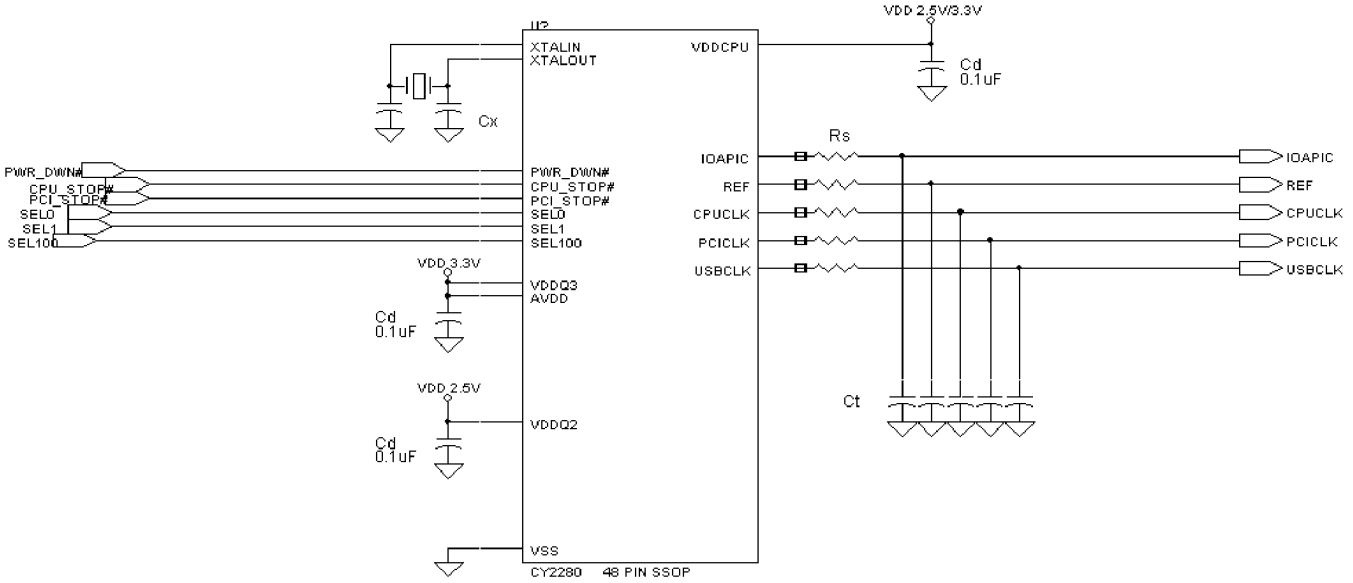


Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit



Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

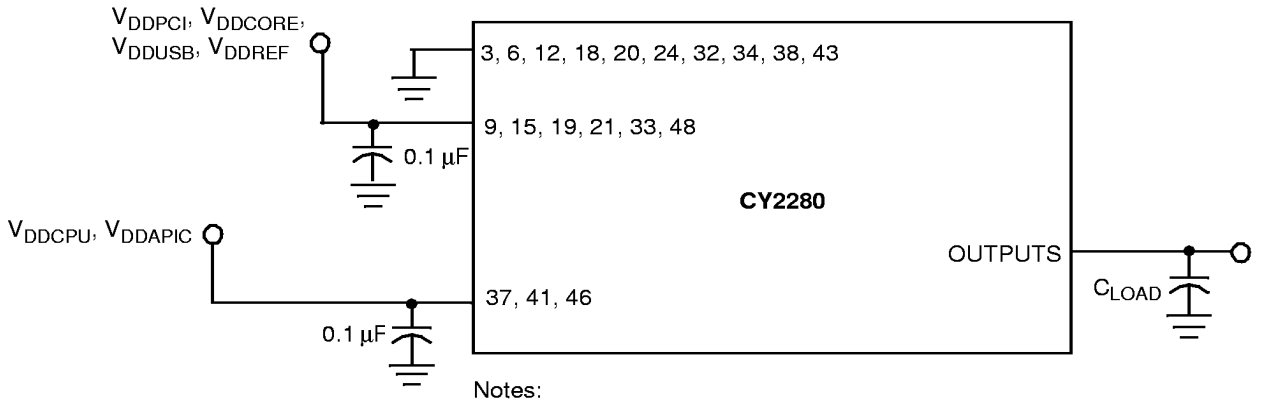
Rs = SERIES TERMINATING RESISTORS

Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and CLOAD of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different CLOAD is used. Footprints must be laid out for flexibility.
- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 µF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the clock generator (specified in the data sheet), and Rseries is the series terminating resistor.

  Rseries > Rtrace – Rout
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead **may** be used to isolate the Board VDD from the clock generator VDD island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note “Layout and Termination Techniques for Cypress Clock Generators” for more details.
- If a Ferrite Bead is used, a 10 µF–22 µF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

Test Circuit



Notes:
Each supply pin must have an individual decoupling capacitor
All capacitors must be placed as close to the pins as is possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2280PVC-1	O48	48-Pin SSOP	Commercial
CY2280PVC-2	O48	48-Pin SSOP	Commercial
CY2280PVC-3	O48	48-Pin SSOP	Commercial

Document #: 38–00596–D

Package Diagram

48-Lead Shrunk Small Outline Package O48