



PRELIMINARY

CY241V08-01,-04,-05,-06

MPEG Clock Generator with VCXO

Features

- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V operation

Benefits

- Highest-performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Application compatibility for a wide variety of designs

Advance Features

- Lower drive strength settings (CY241V08-04, -06)

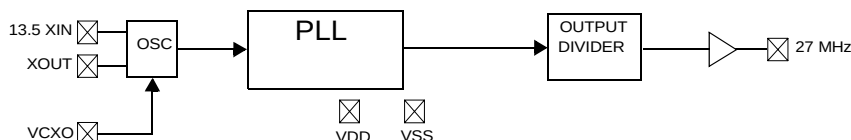
Benefits

- Electromagnetic interference (EMI) reduction for standards compliance

Frequency Table

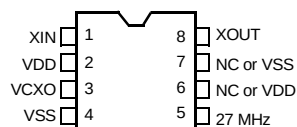
Part Number	Outputs	Input Frequency Range	Output Frequencies	VCXO Control Curve	Other Features
CY241V08-01	1	13.5-MHz pullable crystal input per Cypress specification	One copy of 27 MHz	linear	Pinout compatible with MK3727
CY241V08-04	1	13.5-MHz pullable crystal input per Cypress specification	One copy of 27 MHz	linear	Same as CY241V08-01 except lower drive strength settings
CY241V08-05	1	13.5-MHz pullable crystal input per Cypress specification	One copy of 27 MHz	nonlinear	Mimics MK3727 nonlinear VCXO Control Curve
CY241V08-06	1	13.5-MHz pullable crystal input per Cypress specification	One copy of 27 MHz	nonlinear	Same as CY241V08-05 except lower drive strength settings

Block Diagram



Pin Configuration

CY241V08-01,-04,-05,-06
8-pin SOIC





Pin Descriptions for CY241V08 -01, -04, -05, -06

Name	Pin Number	Description
XIN	1	Reference crystal input
VDD	2	Voltage supply
VCXO	3	Input analog control for VCXO
VSS	4	Ground
27 MHz	5	27-MHz clock output
NC/VDD	6	No connect or voltage supply
NC/VSS	7	No connect or ground
XOUT	8	Reference crystal output

Absolute Maximum Conditions

Supply Voltage (V_{DD}) -0.5 to +7.0V
DC Input Voltage -0.5V to $V_{DD} + 0.5$
Storage Temperature (Non-condensing) -55°C to +125°C
Junction Temperature -40°C to +125°C

Data Retention @ $T_j = 125^\circ\text{C}$ > 10 years
Package Power Dissipation 350 mW
ESD (Human Body Model) MIL-STD-883 > 2000V
(Above which the useful life may be impaired. For user guidelines, not tested.)

Pullable Crystal Specifications^[1]

Parameter	Description	Comments	Min.	Typ.	Max.	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	—	13.5	—	MHz
C_{LNOM}	Nominal load capacitance		—	14	—	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	—	—	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	—	—	—
DL	Crystal drive level	No external series resistor assumed	—	—	150	μW
F_{3SEPHI}	Third overtone separation from $3 \cdot F_{NOM}$	High side	400	—	—	ppm
F_{3SEPLO}	Third overtone separation from $3 \cdot F_{NOM}$	Low side	—	—	-200	ppm
C_0	Crystal shunt capacitance		—	—	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	—	250	—
C_1	Crystal motional capacitance		14.4	18	21.6	fF

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	0	—	70	$^\circ\text{C}$
C_{LOAD}	Max. Load Capacitance	—	—	15	pF
t_{PU}	Power-up time for all VDD pins to reach minimum specified voltage (power ramps must be monotonic)	0.05	—	500	ms

Note:

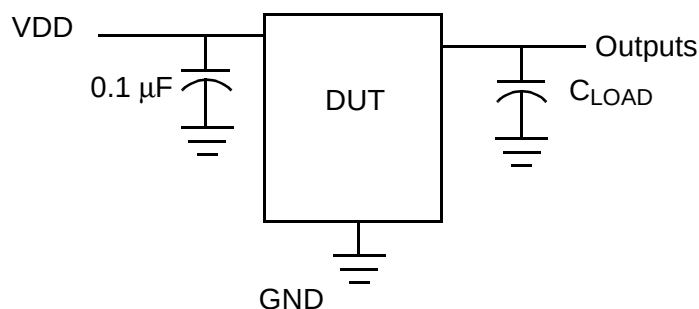
1. Crystals that meet this specification includes: Ecliptek ECX-5788-13.500M, Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL, PDI HA13500XFSA14XC.

DC Electrical Specifications

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output HIGH Current –001, –005	$V_{OH} = V_{DD} - 0.5V$, $V_{DD} = 3.3V$	12	24	–	mA
I_{OL}	Output LOW Current –001, –005	$V_{OL} = 0.5V$, $V_{DD} = 3.3V$	12	24	–	mA
I_{OH}	Output HIGH Current –004, –006	$V_{OH} = V_{DD} - 0.5V$, $V_{DD} = 3.3V$	6	18	–	mA
I_{OL}	Output LOW Current –004, –006	$V_{OL} = 0.5V$, $V_{DD} = 3.3V$	6	18	–	mA
C_{IN}	Input Capacitance	Except XIN, XOUT pins	–	–	7	pF
V_{VCXO}	VCXO Input Range		0	–	V_{DD}	V
$f_{\Delta XO}$	VCXO Pullability Range		± 150	–	–	ppm
I_{VDD}	Supply Current		–	30	35	mA

AC Electrical Specifications ($V_{DD} = 3.3V$)^[2]

Parameter ^[2]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of V_{DD}	45	50	55	%
ER	Rising Edge Rate –001, –005	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15$ pF. See <i>Figure 2</i> .	0.8	1.4	–	V/ns
EF	Falling Edge Rate –001, –005	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , $C_{LOAD} = 15$ pF. See <i>Figure 2</i> .	0.8	1.4	–	V/ns
ER	Rising Edge Rate –004, –006	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15$ pF. See <i>Figure 2</i> .	0.7	1.1	–	V/ns
EF	Falling Edge Rate –004, –006	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , $C_{LOAD} = 15$ pF. See <i>Figure 2</i> .	0.7	1.1	–	V/ns
t_9	Clock Jitter –001, –005	Peak-to-peak period jitter	–	140	–	ps
t_9	Clock Jitter –004, –006	Peak-to-peak period jitter	–	150	–	ps
t_{10}	PLL Lock Time		–	–	3	ms

Test and Measurement Setup

Note:

2. Not 100% tested.

Voltage and Timing Definitions

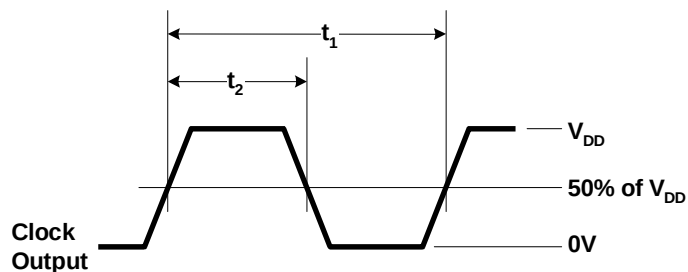


Figure 1. Duty Cycle Definition

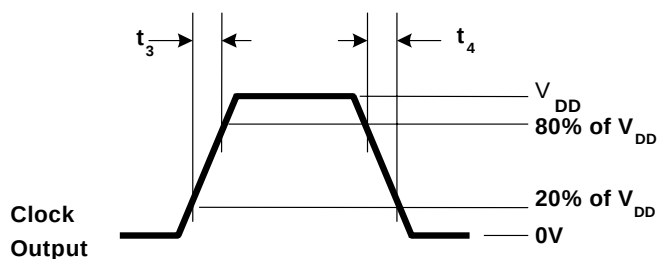


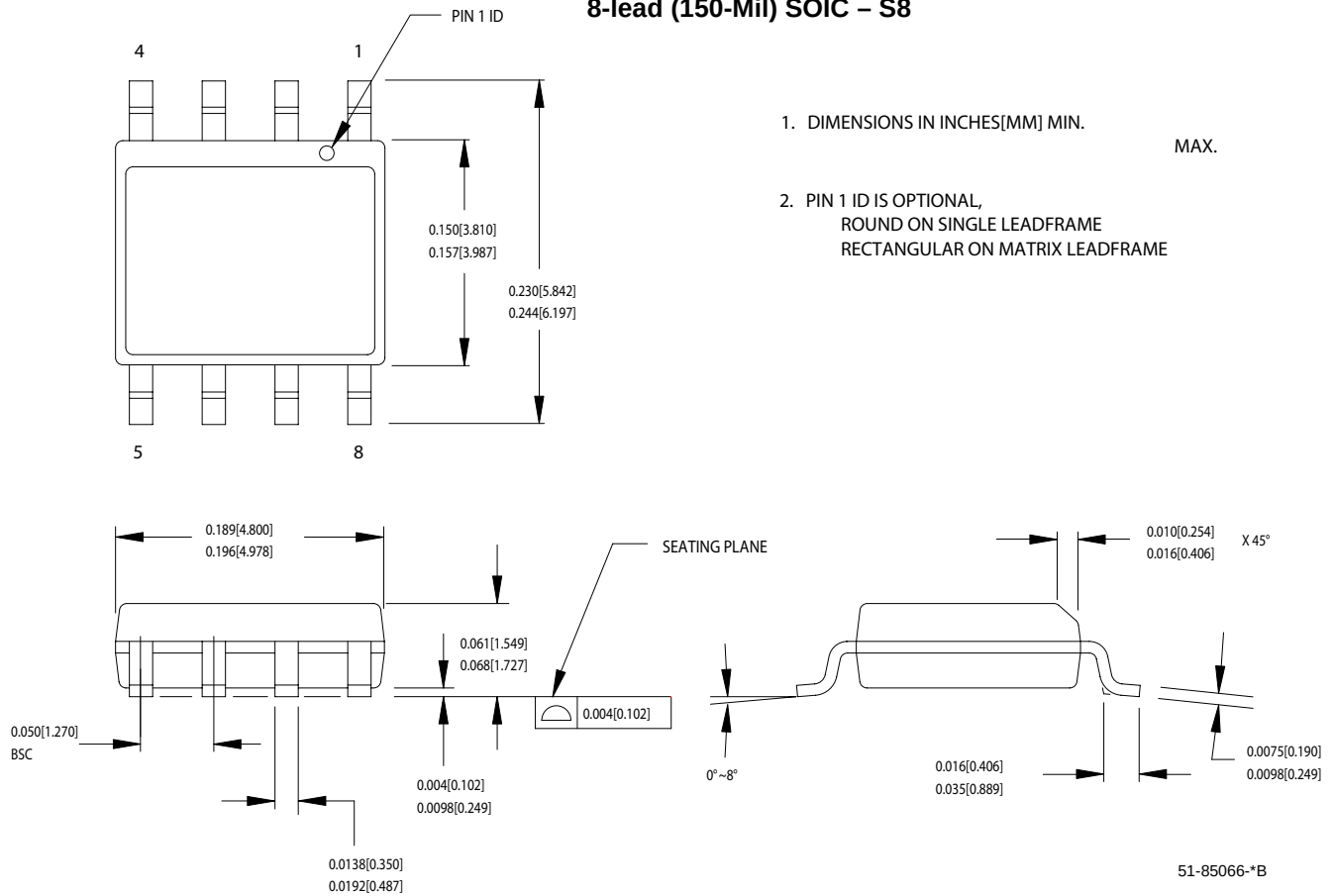
Figure 2. $ER = (0.6 \times V_{DD}) / t_3$, $EF = (0.6 \times V_{DD}) / t_4$

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage	Features
CY241V08SC-01	S8	8-pin SOIC	Commercial	3.3V	Linear VCXO control curve
CY241V08SC-01T	S8	8-pin SOIC – Tape and Reel	Commercial	3.3V	Linear VCXO control curve
CY241V08SC-04	S8	8-pin SOIC	Commercial	3.3V	Lower drive strength version of CY241V08-01
CY241V08SC-04T	S8	8-pin SOIC – Tape and Reel	Commercial	3.3V	Lower drive strength version of CY241V08-01
CY241V08SC-05	S8	8-pin SOIC	Commercial	3.3V	Mimics nonlinear MK3727 VCXO control curve
CY241V08SC-05T	S8	8-pin SOIC – Tape and Reel	Commercial	3.3V	Mimics nonlinear MK3727 VCXO control curve
CY241V08SC-06	S8	8-pin SOIC	Commercial	3.3V	Lower drive strength version of CY241V08-05
CY241V08SC-06T	S8	8-pin SOIC – Tape and Reel	Commercial	3.3V	Lower drive strength version of CY241V08-05

Package Drawing and Dimensions

8-lead (150-Mil) SOIC – S8



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**Document History Page**

Document Title: CY241V08-01,-04,-05,-06 MPEG Clock Generator with VCXO Document Number: 38-07520				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	123982	03/05/03	CKN	New Data Sheet
*A	128430	07/31/03	IJATMP	Changed "Advance Information" to "Preliminary" on top of every page. Added dashes to empty field in tables. Changed Part numbers