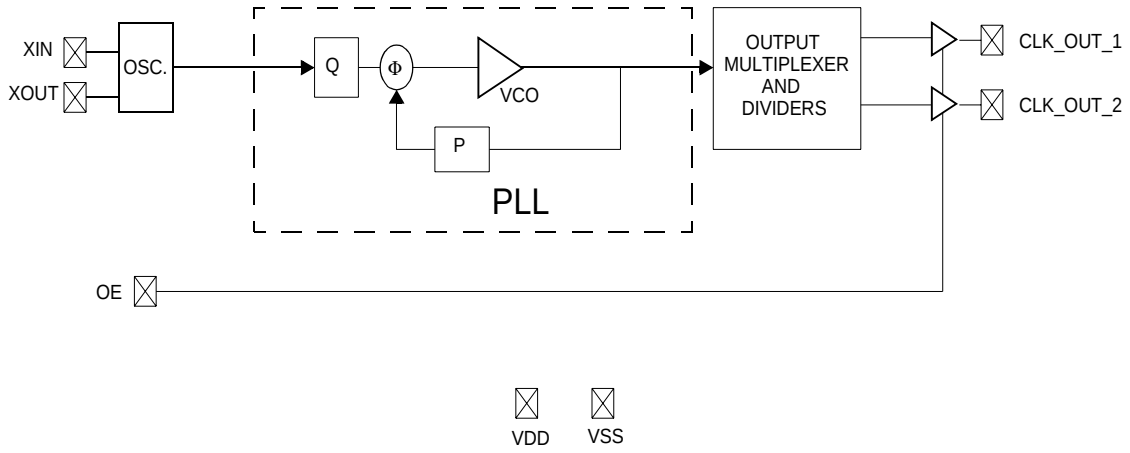
Broadcom Reference Design Clock Generator

Features	Benefits
• **Integrated phase-locked loop**	Highest performance PLL tailored for multimedia applications
• **Low skew, low jitter, high accuracy outputs**	Meets critical timing requirements in complex system designs
• **3.3V Operation**	Enables system and application compatibility

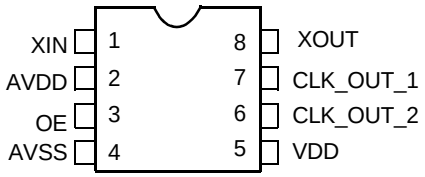
Part Number	Outputs	Broadcom Reference Design	Input Frequency	Output Frequencies
CY26187-1	2	SDK5680	25 MHz	1 copy of 142 MHz, 1 copy 35.5 MHz (3.3V)

Logic Block Diagram - CY26187-1



Pin Configuration

CY26187-1
8-pin SOIC



Pin Summary CY26187-1

Name	Pin Number	Description
XIN	1	25-MHz Reference Crystal Input
AVDD	2	Analog Voltage Supply
OE	3	Output Enable (0 = off; 1 = on)
AVSS	4	Ground
VDD	5	Voltage Supply
CLK_OUT_2	6	35.5-MHz Clock Out
CLK_OUT_1	7	142-MHz Clock Out
XOUT[1]	8	Reference Crystal Output

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage		7.0	V
T_S	Storage Temperature[2]	–65	125	°C
T_J	Junction Temperature		125	°C
	Digital Inputs	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to VDD	V_{SS} – 0.3	V_{DD} + 0.3	V
	Electro-Static Discharge		2000	V

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance			15	pF
f_{REF}	CY26187-1 Reference Frequency		25		MHz
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

DC Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	24		mA
C_{IN}	Input Capacitance				7	pF
I_{IZ}	Input Leakage Current			5		µA
I_{DD}	Supply Current	Sum of core and output current			35	mA

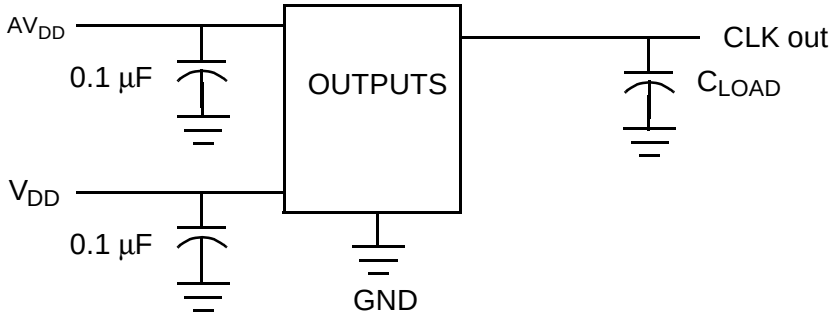
AC Electrical Characteristics ($V_{DD} = 3.3V$)[3]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
	Output Duty Cycle	Duty Cycle is defined in *Figure 1*, 50% of V_{DD}	45	50	55	%
t3	Rising Edge Slew Rate	Output Clock Rise Time, 20% - 80% of V_{DD}	0.8	1.4		V/ns
t4	Falling Edge Slew Rate	Output Clock Fall Time, 80% - 20% of V_{DD}	0.8	1.4		V/ns
t9	Clock Jitter	Peak-to-Peak period jitter			300	ps
t10	PLL Lock Time				3	ms

Notes:

1. Float XOUT pin if XIN is driven by reference clock (as opposed to crystal).
2. Rated for 10 years.
3. Not 100% tested

Test Circuit



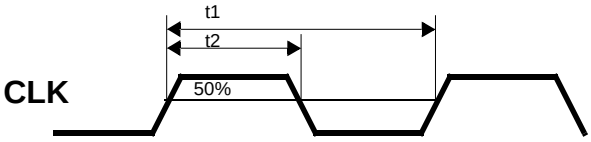


Figure 1. Duty Cycle Definition; DC = t2/t1

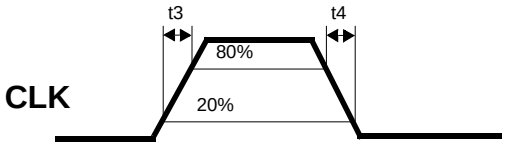


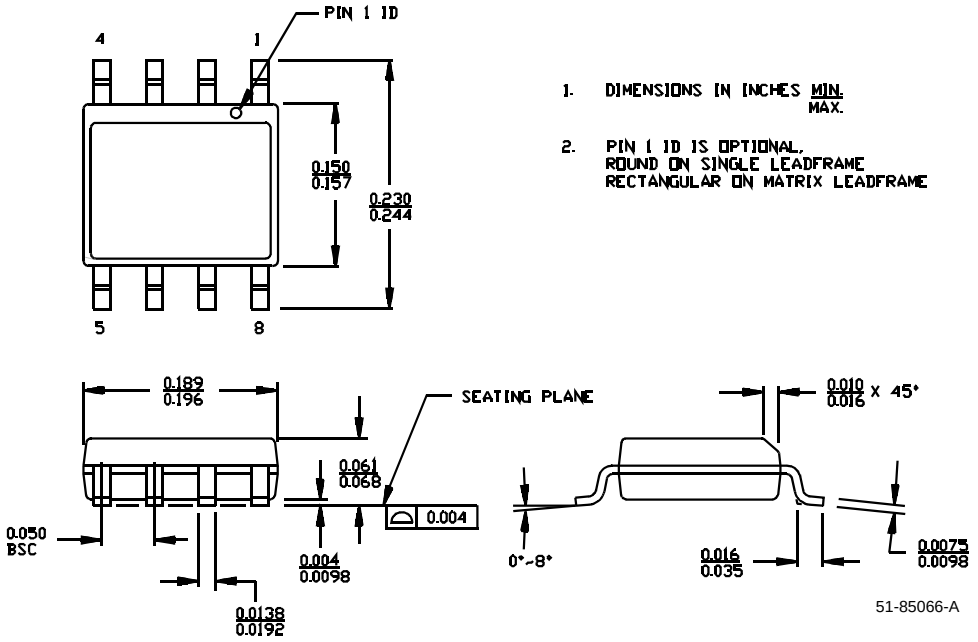
Figure 2. Rise and Fall Time Definitions

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage	Broadcom Reference Design
CY26187SC-1	S8	8-Pin SOIC	Commercial	3.3V	SDK5680

Package Diagram

8-Lead (150-Mil) SOIC S8



Document Title: CY26187-1 Broadcom Reference Design Clock Generator Document Number: 38-07130				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110095	02/19/02	CKN	New data sheet
*A	121871	12/14/02	RBI	Power up requirements added to Operating Conditions Information