# CY74S189, CY27LS03
# CY27S03, CY27S07
## 16 x 4 Static R/W RAM

CYPRESS SEMICONDUCTOR

### Features

- **Fully decoded, 16 word x 4-bit high-speed CMOS RAMs**
- **Inverting outputs 27S03, 27LS03, 74S189**
- **Non-inverting outputs 27S07**
- **High speed**
  **—25 ns**
- **Low power**
  **—210 mW (27LS03)**
- **Power supply 5V ± 10%**
- **Advanced high-speed CMOS processing for optimum speed/power product**
- **Capable of withstanding greater than 2001V static discharge**
- **Three-state outputs**
- **TTL-compatible interface levels**

### Functional Description

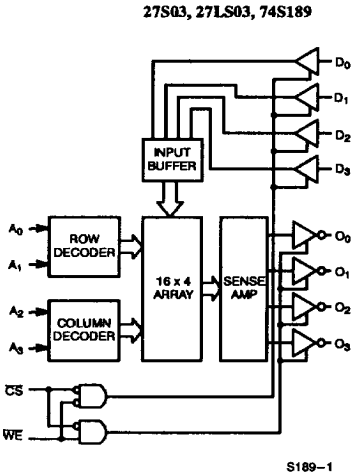
These devices are high-performance 64-bit static RAMs organized as 16 words by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The devices are provided with inverting and non-inverting outputs.

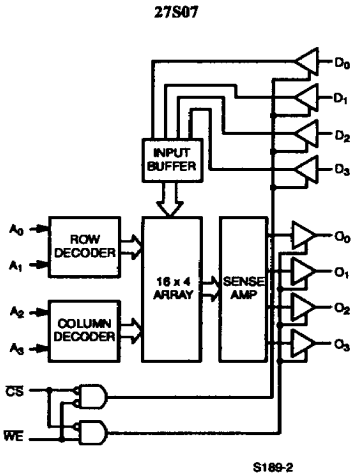
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs ($D_0$ through $D_3$) is written into the memory location specified on the address pins ($A_0$ through $A_3$). The outputs are preconditioned so that the write data is present at the outputs when the write cycle is complete. This precondition operation ensures minimum write recovery times by eliminating the "write recovery glitch."

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins ($O_0$ through $O_3$) in inverted or non-inverted (CY27S07) format.

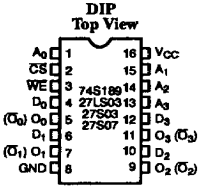
The output pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

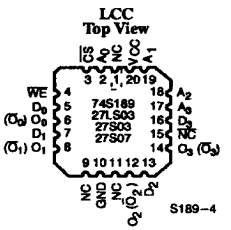
### Logic Block Diagram




### Pin Configurations




**Selection Guide** (For higher performance and lower power, refer to the CY7C189/90 data sheet.)

| | | 27S03 27S07 | 27S03, 27S07 74S189 | 27LS03 |
|---|---|---|---|---|
| Maximum Access Time (ns) | Commercial | 25 | 35 | |
| | Military | 25 | 35 | 65 |
| Maximum Operating Current (mA) | Commercial | 90 | 90 | |
| | Military | 100 | 100 | 38 |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 16 to Pin 8) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current, into Outpus (Low) ..... 10 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001V

Latch-Up Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Military[1] | − 55°C to +125°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range[2]

| Parameters | Description | Test Conditions | | 74S189, 27S03, 27S07 Min. | 74S189, 27S03, 27S07 Max. | 27LS03 Min. | 27LS03 Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = − 5.2 mA | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 16.0 mA | | | 0.45 | | | V |
| | | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | | | | 0.45 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | − 3.0 | 0.8 | − 3.0 | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | − 10 | +10 | − 10 | +10 | µA |
| $V_{CD}$ | Input Diode Clamp Voltage | | | Note 3 | | Note 3 | | |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$ | | − 40 | +40 | − 40 | +40 | µA |
| $I_{OS}$ | Output Short Circuit Current[4] | $V_{CC}$ = Max., $V_{OUT}$ = GND | | | − 90 | | − 90 | mA |
| $I_{OS}$ | Power Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA | Com'l | | 90 | | | mA |
| | | | Mil | | 100 | | 38 | mA |

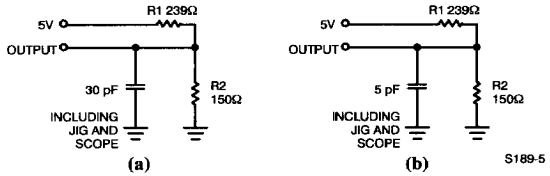
## Capacitance[5]

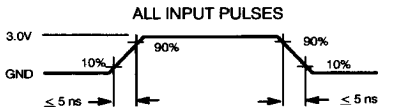
| Parameters | Description | Test Conditions | Max. | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 7 | pF |
| $C_{OUT}$ | Output Capacitance | | 7 | pF |

**Notes:**

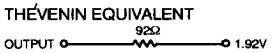
1. $T_A$ is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. The CMOS process does not provide a clamp diode. However these devices are insensitive to − 3V DC input levels and − 5V undershoot pulses of less than 5 ns (measured at 50% points).
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms




Equivalent to: THÉVENIN EQUIVALENT




## Switching Characteristics Over the Operating Range[2,6]

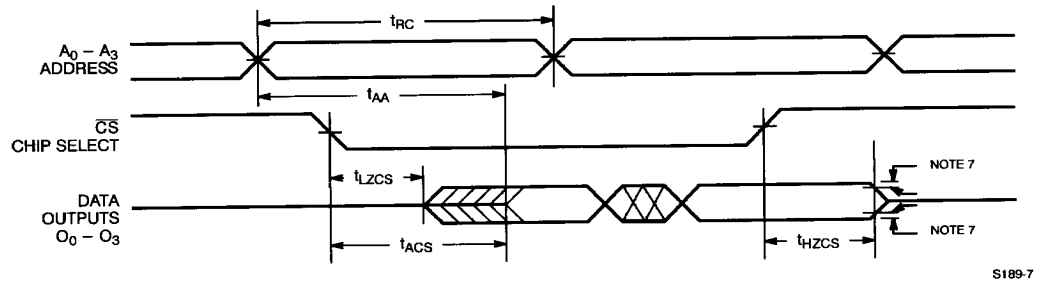
| Parameters | Description | 27S03A 27S07A | | 27S03 27S07 | | 74S189 | | 27LS03 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 25 | | 35 | | 35 | | 65 | | ns |
| $t_{AA}$ | Address to Data Valid[7] | | 25 | | 35 | | 35 | | 65 | ns |
| $t_{ACS}$ | $\overline{CS}$ LOW to Data Valid[7] | | 15 | | 17 | | 22 | | 35 | ns |
| $t_{HZCS}$ | $\overline{CS}$ HIGH to High Z[8, 9, 10] | | 15 | | 20 | | 17 | | 35 | ns |
| **WRITE CYCLE**[6, 11, 12] | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 25 | | 35 | | 35 | | 65 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SCS}$ | $\overline{CS}$ Set-Up to Write Start | | | | | 0 | | | | ns |
| $t_{HCS}$ | $\overline{CS}$ Hold from Write End | | | | | 0 | | | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 20 | | 25 | | 20 | | 55 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 20 | | 25 | | 20 | | 55 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[8, 9, 10] | | 20 | | 25 | | 20 | | 35 | ns |
| $t_{AWE}$ | $\overline{WE}$ HIGH to Output Valid[7] | | 20 | | 35 | | 30 | | 35 | ns |

**Notes:**

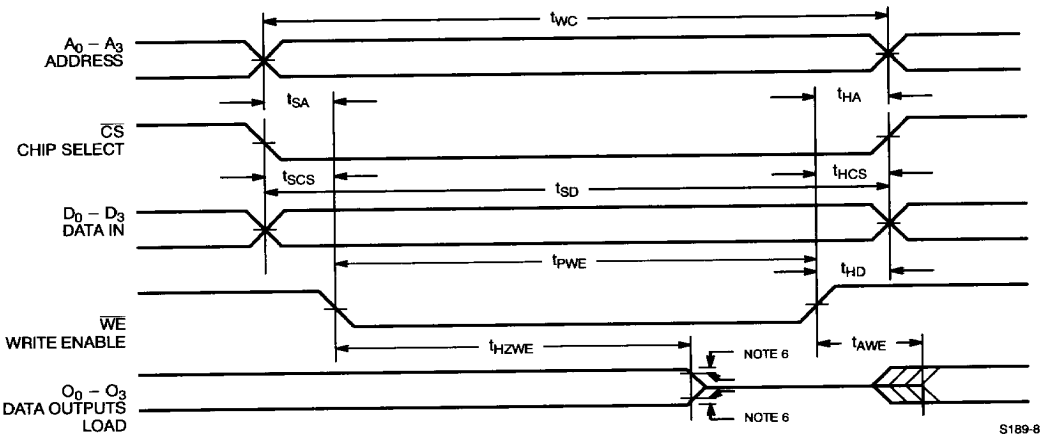
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the spcified $I_{OL}/I_{OH}$ and 30-pF load capacitance.
7. $t_{AA}$, $t_{ACS}$, and $t_{AWE}$ are tested with $C_L$ = 30 pF as in part (a) of AC Test Loads. Timing is referenced to 1.5V on the inputs and outputs.
8. Transition is measured at steady-state HIGH level − 500 mV or steady-state LOW level +500 mV on the output from 1.5V level on the input.
9. $t_{HZCS}$ and $t_{HZWE}$ are tested with $C_L$ = 5 pF as in part (b) of AC Test Loads.
10. At any given temperature and voltage condition, $t_{HZCS}$ is less than $t_{LZCS}$ for any given device.
11. Output is preconditioned to data in (inverted or non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
12. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminates the write.

## Switching Waveforms

### Read Cycle




### Write Cycle [13, 14]




**Notes:**
13. All measurements referenced to 1.5V.
14. Timing diagram represents one solution which results in optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violate.

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|---|---|---|---|
| 25 | CY27S03APC | P1 | Commercial |
| | CY27S03ADC | D2 | |
| | CY27S03ALMB | L61 | Military |
| | CY27S03ADMB | D2 | |
| 35 | CY27S03PC | P1 | Commercial |
| | CY27S03DC | D2 | |
| | CY27S03LC | L61 | |
| | CY27S03LMB | L61 | Military |
| | CY27S03DMB | D2 | |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|---|---|---|---|
| 25 | CY27S07APC | P1 | Commercial |
| | CY27S07ADC | D2 | |
| | CY27S07ALMB | L61 | Military |
| | CY27S07ADMB | D2 | |
| 35 | CY27S07PC | P1 | Commercial |
| | CY27S07DC | D2 | |
| | CY27S07LC | L61 | |
| | CY27S07LMB | L61 | Military |
| | CY27S07DMB | D2 | |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|---|---|---|---|
| 35 | CY74S189PC | P1 | Commercial |
| | CY74S189DC | D2 | |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|---|---|---|---|
| 65 | CY27LS03LMB | L61 | Military |
| | CY27LS03DMB | D2 | |

## MILITARY SPECIFICATIONS
### Group A Subgroup Testing

### DC Characteristics

| Parameters | Subgroups |
|---|---|
| $V_{OH}$ | 1, 2, 3 |
| $V_{OL}$ | 1, 2, 3 |
| $V_{IH}$ | 1, 2, 3 |
| $V_{IL}$ Max. | 1, 2, 3 |
| $I_{IX}$ | 1, 2, 3 |
| $I_{OZ}$ | 1, 2, 3 |
| $I_{CC}$ | 1, 2, 3 |

### Switching Characteristics

| Parameters | Subgroups |
|---|---|
| **READ CYCLE** | |
| $t_{RC}$ | 7, 8, 9, 10, 11 |
| $t_{AA}$ | 7, 8, 9, 10, 11 |
| $t_{ACS}$ | 7, 8, 9, 10, 11 |
| **WRITE CYCLE** | |
| $t_{WC}$ | 7, 8, 9, 10, 11 |
| $t_{SA}$ | 7, 8, 9, 10, 11 |
| $t_{HA}$ | 7, 8, 9, 10, 11 |
| $t_{SCS}$ | 7, 8, 9, 10, 11 |
| $t_{HCS}$ | 7, 8, 9, 10, 11 |
| $t_{SD}$ | 7, 8, 9, 10, 11 |
| $t_{HD}$ | 7, 8, 9, 10, 11 |
| $t_{PWE}$ | 7, 8, 9, 10, 11 |
| $t_{AWE}$ | 7, 8, 9, 10, 11 |

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