Features

- **Pin compatible and functional equivalent to Am2901C**
- **Low power**
- **V_{CC} margin**
  - **— 5V ±10%**
  - **— All parameters guaranteed over commercial and military operating temperature range**
- **Performs eight operations on two 4-bit operands**
- **Infinitely expandable in 4-bit increments**
- **Four status flags: carry, overflow, negative, zero**
- **Capable of withstanding greater than 2001V static discharge voltage**

Functional Description

The CY2901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY2901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY2901, as illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU and the required data manipulation and control logic.

The operation performed is determined by nine input control lines (I_0 to I_8) that are usually inputs from an instruction register.

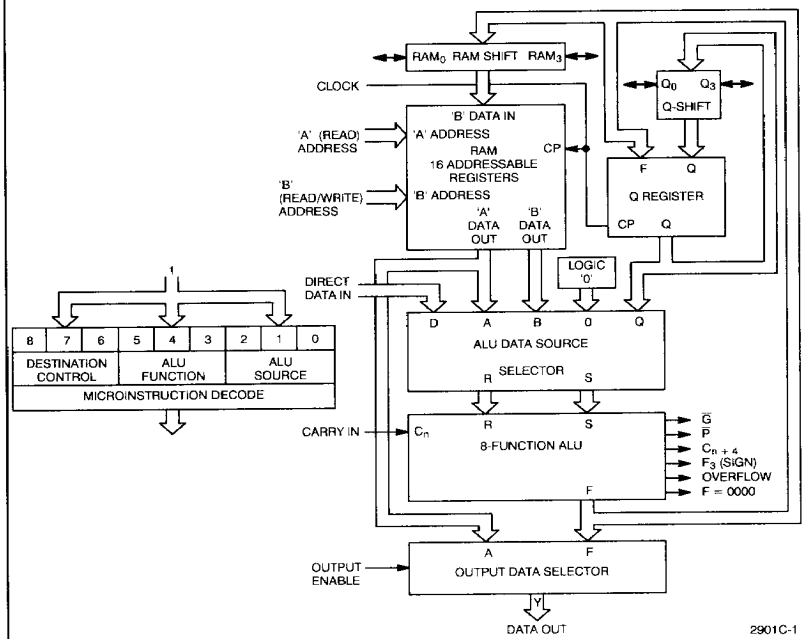
The CY2901 is expandable in 4-bit increments, has three-state data outputs as well as flag outputs, and can use either a full carry look-ahead or a ripple carry.

The CY2901 is a pin-compatible, functionally equivalent, improved-performance replacement for the AM2901.

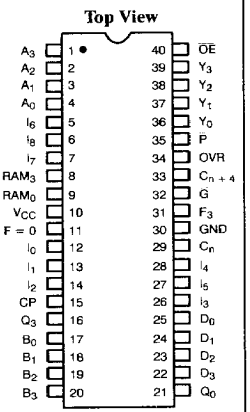
The CY2901 is fabricated using an advanced 1.2-micron CMOS process that eliminates latch-up, provides ESD protection over 2001V, and achieves superior performance at low power dissipation.

6 LOGIC

Logic Block Diagram



Pin Configuration



Selection Guide See last page for ordering information.

Read Modify-Write Cycle (Min.) in ns	Operating I_{CC} (Max.) in mA	Operating Range	Part Number
31	140	Commercial	CY2901C
32	180	Military	CY2901C

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 30 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015)

Latch-Up Current (Outputs) ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	− 55°C to +125°C	5V ±10%

Notes:

1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
$A_0 - A_3$	I	These four address lines select one of the registers in the stack and output its contents on the (internal) A port.
$B_0 - B_3$	I	These four address lines select one of the registers in the sack and output its contents on the (internal) B port. This can also be the destination address when data is written back into the register file.
$I_0 - I_8$	I	These nine instruction lines select the ALU data sources ($I_{0, 1, 2}$), the operation to be performed ($I_{3, 4, 5}$), and what data is to be written into either the Q register or the register file ($I_{6, 7, 8}$).
$D_0 - D_3$	I	These are four data input lines that may be selected by the $I_{0, 1, 2}$ lines as inputs to the ALU.
$Y_0 - Y_3$	O	These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latches, as determined by the code on the $I_{6, 7, 8}$ lines.
$\overline{OE}$	I	Output Enable. This is an active LOW input that controls the $Y_0 - Y_3$ outputs. When this signal is LOW the Y outputs are enabled and when it is HIGH they are in the high-impedance state.
CP	I	Clock Input. The LOW level of the clock writes data to the 16 x 4 RAM. The HIGH level of the clock writes data from the RAM to the A-port and B-port latches. The operation of the Q register is similar. Data is entered into the master latch on the LOW level of the clock and transferred from master to slave when the clock is HIGH.
Q_3 RAM_3	I/O	These two lines are bidirectional and are controlled by the $I_{6, 7, 8}$ inputs. Electrically they are three-state output drivers connected to the TTL-compatible CMOS inputs.
Q_3 RAM_3 (cont.)	I/O	**Outputs:** When the destination code on lines $I_{6, 7, 8}$ indicates a shift left (UP) operation the three-state outputs are enabled and the MSB of the Q register is output on the Q_3 pin and the MSB of the ALU output (F_3) is output on the RAM_3 pin. **Inputs:** When the destination code indicates a shift right (DOWN) the pins are the data inputs to the MSB of the Q register and the MSB of the RAM.
Q_0 RAM_0	I/O	These two lines are bidirectional and function in a manner similar to the Q_3 and RAM_3 lines, except that they are the LSB of the Q register and RAM.
C_n	I	The carry-in to the internal ALU.
C_{n+4}	O	The carry-out from the internal ALU.
$\overline{G}, \overline{P}$	O	The carry generate and the carry propagate outputs of the ALU, which may be used to perform a carry look-ahead operation over the 4 bits of the ALU.
OVR	O	Overflow. This signal is logically the exclusive-OR of the carry-in and the carry-out of the MSB of the ALU. This pin indicates that the result of the ALU operation has exceeded the capacity of the machine. It is valid only for the sign bit and assumes two's complement coding for negative numbers.
F = 0	O	Open collector output that goes HIGH if the data on the ALU outputs ($F_{0, 1, 2, 3}$) are all LOW. It indicates that the result of an ALU operation is zero (positive logic).
F_3	O	The most significant bit of the ALU output.

Electrical Characteristics Over the Operating Range (V_{CC}Min. = 4.5V, V_{CC}Max. = 5.5V)[2]

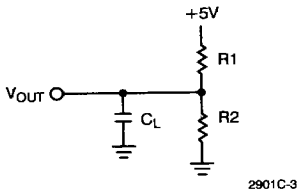
Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −3.4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 20 mA Commercial, 16 mA Military			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			− 3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}			10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND			− 10	µA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V		− 3.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.4V	Commercial	20		mA
			Military	16		mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND or V_{CC}		− 40	+40	µA
I_{SC}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0V		− 30	− 85	mA
I_{CC}	Supply Current	V_{CC} = Max.	Commercial		140	mA
			Military		180	mA

Capacitance[4]

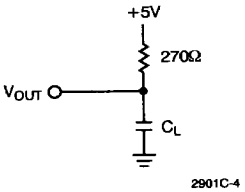
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. Tested initially and after any design or process changes that may affect these parameters.

Output Loads used for AC Performance Characteristics



All outputs except open drain



Open drain (F = 0)

Notes:
1. C_L = 50 pF includes scope probe, wiring and stray capacitance.
2. C_L = 5 pF for output disable tests.
3. Loads shown above are for commercial (20 mA) I_{OL} specifications only.

	Commercial	Military
R_1	203Ω	252Ω
R_2	148Ω	174Ω

CY2901C Guaranteed Commercial Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See previous page for loading circuit information.

This data applies to parts with the following numbers: CY2901CPC, CY2901CDC, CY2901CLC

Cycle Time and Clock Characteristics

CY2901–	C
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	31 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32 MHz
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	15 ns
Minimum Clock Period	31 ns

For faster performance see CY7C901–23 specification.

Combinatorial Propagation Delays. C_L = 50 pF[5]

To Output	Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F = 0	OVR	RAM_0	Q_0
From Input	**Y**	**F_3**	**C_{n+4}**	**$\overline{G}, \overline{P}$**	**F = 0**	**OVR**	**RAM_3**	**Q_3**
A, B Address	40	40	40	37	40	40	40	—
D	30	30	30	30	38	30	30	—
C_n	22	22	20	—	25	22	25	—
I_{012}	35	35	35	37	37	35	35	—
I_{345}	35	35	35	35	38	35	35	—
I_{678}	25	—	—	—	—	—	26	26
A Bypass ALU (I = 2XX)	35	—	—	—	—	—	—	—
Clock (LOW to HIGH)	35	35	35	35	35	35	35	28

Set-Up and Hold Times Relative to Clock (CP) Input[5, 6]

Input	CP: Set-Up Time Before H ⇓ L	Hold Time After H ⇓ L	Set-Up Time Before L ⇑ H	Hold Time After L ⇑ H
A, B Source Address	15	1 (Note 7)	30, 15 + t_{PWL} (Note 8)	1
B Destination Address	15	⇓ Do Not Change ⇑		1
D	—	—	25	0
C_n	—	—	20	0
I_{012}	—	—	30	0
I_{345}	—	—	30	0
I_{678}	10	⇓ Do Not Change ⇑		0
$RAM_{0,3}$, $Q_{0,3}$	—	—	12	0

Output Enable/Disable Times

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY2901C	$\overline{OE}$	Y	23	23

Notes:

5. A dash indicates a propagation delay path or set-up time constraint does not exist.
6. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change."
7. Source addresses must be stable prior to the clock H ⇓ L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
8. The set-up time prior to the clock L ⇑ H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time form stable A and B addresses to the clock L ⇑ H transition, regardless of when the clock H ⇓ L transition occurs.

CY2901C Guaranteed Military Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Military (− 55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" of this data sheet for loading circuit information.

This data applies to parts with the following numbers:
CY2901CDMB

Cycle Time and Clock Characteristics[2]

CY2901 −	C
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	32 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	31 MHz
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	15 ns
Minimum Clock Period	32 ns

For faster performance see CY7C901−27 specification.

Combinatorial Propagation Delays. C_L = 50 pF[2, 5]

To Output	**Y**	**F_3**	**C_{n+4}**	**$\overline{G}, \overline{P}$**	**F = 0**	**OVR**	**RAM_3**	**Q_3**
From Input	**Y**	**F_3**	**C_{n+4}**	**$\overline{G}, \overline{P}$**	**F = 0**	**OVR**	**RAM_0**	**Q_0**
A, B Address	48	48	48	44	48	48	48	—
D	37	37	37	34	40	37	37	—
C_n	25	25	21	—	28	25	28	—
I_{012}	40	40	40	44	44	40	35	—
I_{345}	40	40	40	40	40	40	40	—
I_{678}	29	—	—	—	—	—	29	29
A Bypass ALU (I = 2XX)	40	—	—	—	—	—	—	—
Clock (LOW to HIGH)	40	40	40	40	40	40	40	33

Set-Up and Hold Times Relative to Clock (CP) Input[5, 6]

Input	CP: Set-Up Time Before H ⇂ L	Hold Time After H ⇂ L	Set-Up Time Before L ⇂ H	Hold Time After L ⇂ H
A, B Source Address	15	2 (Note 7)	30, 15 + t_{PWL} (Note 8)	2
B Destination Address	15	⇂ Do Not Change ⇂		2
D	—	—	25	0
C_n	—	—	20	0
I_{012}	—	—	30	0
I_{345}	—	—	30	0
I_{678}	10	⇂ Do Not Change ⇂		0
$RAM_{0,3}$, $Q_{0,3}$	—	—	12	0

Output Enable/Disable Times

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY2901C	$\overline{OE}$	Y	25	25

Ordering Information

Read Modify-Write Cycle (ns)	Ordering Code	Package Type	Operating Range
31	CY2901CDC	D18	Commercial
	CY2901CPC	P17	
32	CY2901CDMB	D18	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3

Cycle Time and Clock Characteristics

Parameters	Subgroups
Minimum Clock LOW Time	7, 8, 9, 10, 11
Minimum Clock HIGH Time	7, 8, 9, 10, 11

Combinational Propagation Delays

Parameters	Subgroups
From A, B Address to Y	7, 8, 9, 10, 11
From A, B Address to F_3	7, 8, 9, 10, 11
From A, B Address to C_{n+4}	7, 8, 9, 10, 11
From A, B Address to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From A, B Address to F = 0	7, 8, 9, 10, 11
From A, B Address to OVR	7, 8, 9, 10, 11
From A, B Address to $RAM_{0,3}$	7, 8, 9, 10, 11
From D to Y	7, 8, 9, 10, 11
From D to F_3	7, 8, 9, 10, 11
From D to C_{n+4}	7, 8, 9, 10, 11
From D to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From D to F = 0	7, 8, 9, 10, 11
From D to OVR	7, 8, 9, 10, 11
From D to $RAM_{0,3}$	7, 8, 9, 10, 11

Combinational Propagation Delays (Continued)

Parameters	Subgroups
From C_n to Y	7, 8, 9, 10, 11
From C_n to F_3	7, 8, 9, 10, 11
From C_n to C_{n+4}	7, 8, 9, 10, 11
From C_n to F = 0	7, 8, 9, 10, 11
From C_n to OVR	7, 8, 9, 10, 11
From C_n to $RAM_{0,3}$	7, 8, 9, 10, 11
From I_{012} to Y	7, 8, 9, 10, 11
From I_{012} to F_3	7, 8, 9, 10, 11
From I_{012} to C_{n+4}	7, 8, 9, 10, 11
From I_{012} to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From I_{012} to F = 0	7, 8, 9, 10, 11
From I_{012} to OVR	7, 8, 9, 10, 11
From I_{012} to $RAM_{0,3}$	7, 8, 9, 10, 11
From I_{345} to Y	7, 8, 9, 10, 11
From I_{345} to F_3	7, 8, 9, 10, 11
From I_{345} to C_{n+4}	7, 8, 9, 10, 11
From I_{345} to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From I_{345} to F = 0	7, 8, 9, 10, 11
From I_{345} to OVR	7, 8, 9, 10, 11
From I_{345} to $RAM_{0,3}$	7, 8, 9, 10, 11
From I_{678} to Y	7, 8, 9, 10, 11
From I_{678} to $RAM_{0,3}$	7, 8, 9, 10, 11
From I_{678} to $Q_{0,3}$	7, 8, 9, 10, 11
From A Bypass ALU to Y (I = 2XX)	7, 8, 9, 10, 11
From Clock LOW to HIGH to Y	7, 8, 9, 10, 11
From Clock LOW to HIGH to F_3	7, 8, 9, 10, 11
From Clock LOW to HIGH to C_{n+4}	7, 8, 9, 10, 11
From Clock LOW to HIGH to $\overline{G}$, $\overline{P}$	7, 8, 9, 10, 11
From Clock LOW to HIGH to F = 0	7, 8, 9, 10, 11
From Clock LOW to HIGH to OVR	7, 8, 9, 10, 11
From Clock LOW to HIGH to $RAM_{0,3}$	7, 8, 9, 10, 11
From Clock LOW to HIGH to $Q_{0,3}$	7, 8, 9, 10, 11

Set-Up and Hold Times Relative to Clock (CP) Input

Parameters	Subgroups
A, B Source Address Set-Up Time Before H ⧫ L	7, 8, 9, 10, 11
A, B Source Address Hold Time After H ⧫ L	7, 8, 9, 10, 11
A, B Source Address Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
A, B Source Address Hold Time After L ⧫ H	7, 8, 9, 10, 11
B Destination Address Set-Up Time Before H ⧫ L	7, 8, 9, 10, 11
B Destination Address Hold Time After H ⧫ L	7, 8, 9, 10, 11
B Destination Address Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
B Destination Address Hold Time After L ⧫ H	7, 8, 9, 10, 11
D Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
D Hold Time After L ⧫ H	7, 8, 9, 10, 11
C_n Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
C_n Hold Time After L ⧫ H	7, 8, 9, 10, 11
I_{012} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
I_{012} Hold Time After L ⧫ H	7, 8, 9, 10, 11
I_{345} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
I_{345} Hold Time After L ⧫ H	7, 8, 9, 10, 11
I_{678} Set-Up Time Before H ⧫ L	7, 8, 9, 10, 11
I_{678} Hold Time After H ⧫ L	7, 8, 9, 10, 11
I_{678} Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
I_{678} Hold Time After L ⧫ H	7, 8, 9, 10, 11
RAM_0, RAM_3, Q_0, Q_3 Set-Up Time Before L ⧫ H	7, 8, 9, 10, 11
RAM_0, RAM_3, Q_0, Q_3 Hold Time After L ⧫ H	7, 8, 9, 10, 11

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