PRELIMINARY

FastEdge™ Series
CY2PP3220

Dual 1:10 Differential Fanout Buffer

Features

- **Two sets of ten ECL/PECL differential outputs**
- **Two ECL-/PECL-differential inputs**
- **Hot-swappable/-insertable**
- **50-ps output-to-output skew**
- **< 500-ps device-to-device skew**
- **Less than 10-ps intrinsic jitter**
- **500-ps propagation delay (typical)**
- **Operation from DC to 1.5 GHz**
- **PECL supply range: V_{CC} = 2.375V to 3.465V with V_{EE} = 0V**
- **ECL mode supply range: V_{EE} = –2.375V to –3.465V with V_{CC} = 0V**
- **Industrial temperature range: –40°C to 85°C**
- **52-pin 1.4-mm TQFP package**
- **Temperature compensation like 100K ECL**

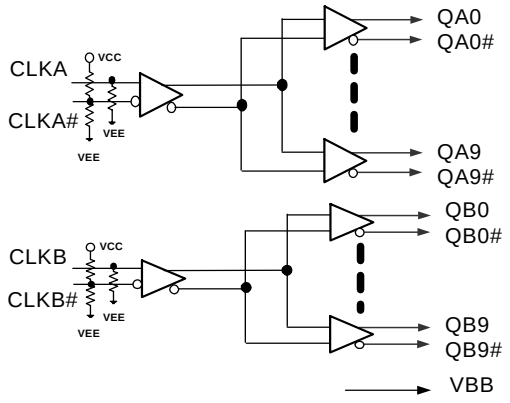
Description

The CY2PP3220 is a low-skew, low propagation delay, dual 1-to-10 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.5 GHz.

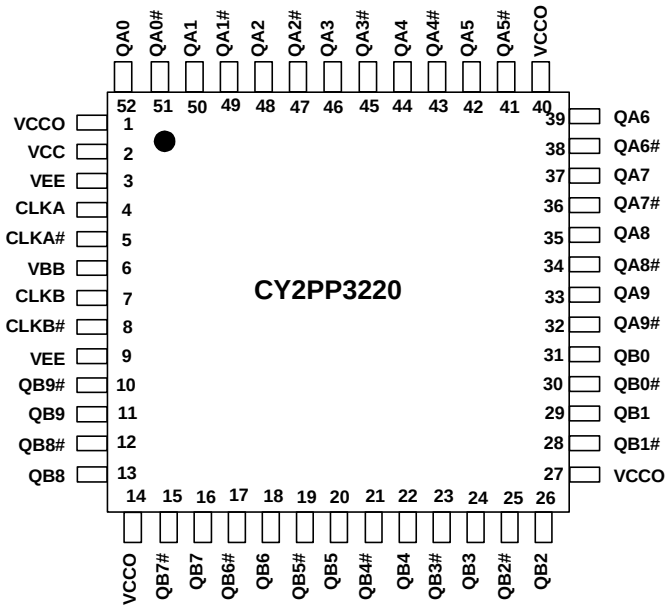
The device features two differential input paths which are differential internally. The CY2PP3220 may function not only as a differential clock buffer but also as a signal level translator and fanout ECL/PECL single-ended or differential signals to twenty ECL/PECL differential loads. An external bias pin, VBB, is provided for distributing a single-ended signal. In such an application, the VBB pin should be connected to either one of the CLKA# or CLKB# inputs and bypassed to V_{CC} via a 0.01-µF capacitor. Traditionally, in ECL, it is used to provide the reference level to a receiving single ended input that might have a different self bias point.

Since the CY2PP3220 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high-frequency, high-precision clocks across backplanes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2PP3220 delivers consistent, guaranteed performance over differing platforms.

Block Diagram



Pin Configuration



Pin Description

Pin	Name	I/O	Type	Description
4,5	CLKA, CLKA#	I,PD[1] I,PC	ECL/PECL	**Default Differential clock input pair**
7,8	CLKB, CLKB#	I,PD I,PC	ECL/PECL	**Alternate Differential clock input pair**
52,50,48,46,44,42,39,37,35,33	QA(0:9)	O,OS	ECL/PECL	**True output**
51,49,47,45,43,41,38,36,34,32	QA#(0:9)	O,OS	ECL/PECL	**Complement output**
31,29,26,24,22,20,18,16,13,11	QB(0:9)	O,OS	ECL/PECL	**True output**
30,28,25,23,21,19,17,15,12,10	QB#(0:9)	O,OS	ECL/PECL	**Complement output**
6	VBB[3]	O	Bias	**Reference voltage output for single ended ECL or PECL operation**
3,9	VEE[2]	–PWR	Power	**Power supply, negative connection**
2	VCC	+PWR	Power	**Power supply, positive connection**
1,14,27,40	VCCO	+PWR	Power	**Power supply, positive connection**

Governing Agencies

The following agencies provide specifications that apply to the CY2PP3220. The agency name and relevant specification is listed below.

Agency Name	Specification
JEDEC	JESD 51 (Theta JA) JESD 8–2 (ECL) JESD 65–A (skew,jitter)
IEEE	1596.3 (Jitter specs)
UL	94 (Flammability)
Mil–Spec	883E Method 1012.1 (Thermal Theta JC)

Notes:

1. In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-down, PU for Pull-up, PC for Pull Center, O for output, OS for open source and PWR for Power.
2. In ECL mode (negative power supply mode), V_{EE} is either –3.3V or –2.5V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}) and are between VCC and VEE.
3. V_{BB} is available for use for single ended bias mode when V_{CC} is +3.3V.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Supply Voltage	Non-functional	–0.3	4.6	VDC
V_{CC}	Operating Voltage	Functional	2.5 – 5%	3.3 + 5%	VDC
V_{BB}	Output Reference Voltage	Relative to V_{CC}	V_{CC}–1.525	V_{CC}–1.325	VDC
I_{BB}	Output Reference Current	Relative to V_{BB}		200	uA
VTT	Output Termination Voltage	VTT = 0V for V_{CC} = 2.5V		V_{CC}–2	VDC
V_{IN}	Input Voltage	Relative to V_{CC}	–0.3	V_{CC}+0.3	VDC
V_{OUT}	Output Voltage	Relative to V_{CC}	–0.3	V_{CC}+0.3	VDC
LU_I	Latch Up Immunity	Functional	300		mA
T_S	Temperature, Storage	Non-Functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	–40	85	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	TBD	TBD	°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	40	60	°C/W
ESD_h	ESD Protection (Human Body Model)		2000		V
M_{SL}	Moisture Sensitivity Level		TBD		N.A.
G_{ATES}	Total Functional Gate Count	Assembled Die	50		Ea.
UL–94	Flammability Rating	At 1/8 in.	V–0		N.A.
FIT	Failure in Time	Manufacturing test	1		ppm

PECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
$V_{CC2.5V}$	2.5 Operating Voltage	2.5V ± 5%, V_{EE} = 0.0V	2.375	2.625	V
$V_{CC3.3V}$	3.3 Operating Voltage	3.3V ± 5%, V_{EE} = 0.0V	3.135	3.465	V
V_{IL}	Input Voltage, Low		V_{CC}–1.945	V_{CC}–1.625	V
V_{IH}	Input Voltage, High	Define V_{CC} and load current	V_{CC}–1.165	V_{CC}–0.880	V
I_{IN}	Input Current[4]	V_{IN} = [VILmin=2.406V or V_{IH}–ax=1.655V] at VCC=3.6V		200	uA
Clock Input Pair CLKA, CLKA#, CLKB1, CLKB1#(PECL Differential Signals)					
V_{PP}	Differential input voltage[5]	Differential operation	0.1	1.3	V
V_{CMR}	Differential cross point voltage[6]	Differential operation	1.2	V_{CC}	V
I_{IN}	Input Current[4]	V_{IN} = V_{IL} or V_{IN} = V_{IH}		200	uA
PECL Outputs QA((0:9),#),QB((0:9),#)(PECL Differential Signals)					
V_{OH}	Output High Voltage	I_{OH} = –30 mA[7] (50Ω Load)	V_{CC}–1.145	V_{CC}–0.895	V
V_{OL}	Output Low Voltage V_{CC} = 3.3V ± 5% V_{CC} = 2.5V ± 5%	I_{OL} = –5 ma[7] (50Ω Load)	V_{CC}–1.945 V_{CC}–1.945	V_{CC}–1.695 V_{CC}–1.695	V
Supply Current and VBB					
I_{EE}	Maximum Quiescent Supply Current without output termination current[7]	VEE pin	–	260	mA
V_{BB}	Output reference voltage	IBB = 200 uA	V_{CC}–1.525	V_{CC}–1.325	V
I_{PUP}	Internal Pull-up Current		TBD	TBD	mA
I_{PDWN}	Internal Pull-down Current		TBD	TBD	mA.

Notes:

4. Input have internal pullup / pulldown or biasing resistors which affect the input current.
5. VPP (DC) is the minimum differential input voltage swing required to maintain device functionality.
6. VCMR (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the VCMR (DC) range and the input swing lies within the VPP (DC) specification.
7. Equivalent to a termination of 50 Ω to VTT.

PECL DC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
C_{IN}	Input pin capacitance		TBD	TBD	pF
C_{OUT}	Output pin capacitance		TBD	TBD	pF
L_{IN}	Pin Inductance		TBD	TBD	nH
Z_{OUT}	Output impedance		TBD	TBD	Ω

ECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{EE}	–2.5 Negative Power Supply	–2.5V ± 5%, V_{EE} = 0.0V	–2.375	–2.625	V
V_{EE}	–3.3 Negative Power Supply	–3.3V ± 5%, V_{EE} = 0.0V	–3.135	–3.465	V
V_{IL}	Input Voltage, Low		–1.945	–1.625	V
V_{IH}	Input Voltage, High	Define V_{CC} and load current	–1.165	–0.880	V
I_{IN}	Input Current[4]	V_{IN} = V_{IL} or Vin = V_{IH}		200	uA
Clock Input Pair CLKA,CLKA#,CLKB,CLKB# (ECL Differential Signals)					
V_{PP}	Differential input voltage[5]	Differential operation	0.1	1.3	V
V_{CMR}	Differential cross point voltage[6]	Differential operation	V_{EE}+1.2	0	V
I_{IN}	Input Current[4]	V_{IN} = V_{IL} or V_{IN} = V_{IH}		200	uA
ECL Outputs QA((0:9),#),QB((0:9),#) (ECL Differential Signals)					
V_{OH}	Output High Voltage	I_{OH} = –30 mA[7]	–1.145	–0.895	V
V_{OL}	Output Low Voltage V_{EE} = –3.3V ± 5% V_{EE} = –2.5V ± 5%	I_{OL} = –5 ma[7]	–1.945 –1.945	–1.695 –1.3	V
Supply Current and VBB					
I_{EE}	Maximum Quiescent Supply Current without output termination current [8]	V_{EE} pin		130	mA
V_{BB}	Output reference voltage	I_{BB}=200 uA	–1.525	–1.325	V

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Clock input pair CLKA, CLKA#, CLKB,CLKB# (PECL or ECL differential signals)					
V_{PP}	Differential input voltage[10]	Differential Operation	0.1	1.3	V
V_{CMR}	Differential cross point voltage[11]	Differential Operation	V_{EE}+1.2	0	V
F_{IN}	Input Frequency[12]	50% Duty Cycle Standard load		1500	MHz
T_{PD}	Propagation Delay CLKA or CLKB to QA((0:4),#),QB((0:4),#) pairs	660-MHz 50% Duty Cycle Standard Load Differential Operation	400	750	ps
Clock Outputs QA((0:9),#),QB((0:9),#)					
$Vo_{(P-P)}$	Differential output voltage (peak-to-peak)	Differential PRBS fo < 50 MHz fo < 0.8 GHz fo < 1.0 GHz	0.45 0.4 0.375	–	V
V_{CMR}	Common Voltage Range		V_{CC}–1.425		V

Notes:

8. I_{CC} Calculation: ICC = (number of differential output pairs used) x (I_{OH} + I_{OL}) + IEE or I_{CC} = (number of differential output pairs used) x (V_{OH} –VTT)/Rload + (V_{OL} –VTT)/Rload +I_{EE}.
9. AC characteristics apply for parallel output termination of 50Ω to VTT.
10. VPP (AC) is the minimum differential ECL/PECL input swing required to maintain AC characteristics including tpd and device-to-device skew.
11. VCMR (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the VCMR(AC) range and the input swing lies within the VPP(AC) specification. Violation of VCMR(AC) or VPP(AC) impacts the device propagation delay, device and part-to-part skew.
12. The CY2PP3220 is fully operation up to 1.5 GHz.

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$tsk_{(O)}$	Output-to-output skew	660-MHz 50% duty cycle Standard load Differential Operation	–	50	ps
$tsk_{(PP)}$	Output-to-output skew (part-to-part)	660-MHz 50% duty cycle Standard load Differential Operation	–	500	ps
t_{CCJ}	Output cycle-to-cycle jitter (Intrinsic)	660-MHz 50% duty cycle Standard load Differential Operation	TBD	TBD	ps
$tsk_{(P)}$	Output pulse skew [13]	660-MHz 50% duty cycle Standard load Differential Operation	TBD	TBD	ps
T_R,T_F	Output Rise/Fall time	660-MHz 50% duty cycle Differential 20% to 80%	–	0.3	ns
TTB	Total Timing Budget	660-MHz 50% duty cycle Standard load	TBD	TBD	ps
D_J	Deterministic/Intrinsic Jitter	660-MHz 50% duty cycle Standard load	–	10	ps r.m.s.

Timing Definitions

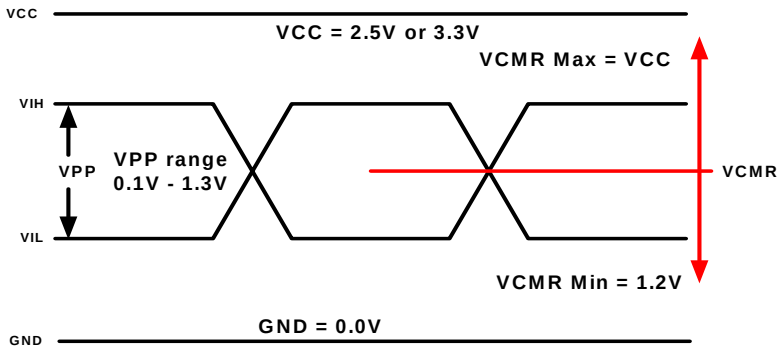


Figure 1. PECL Waveform Definitions

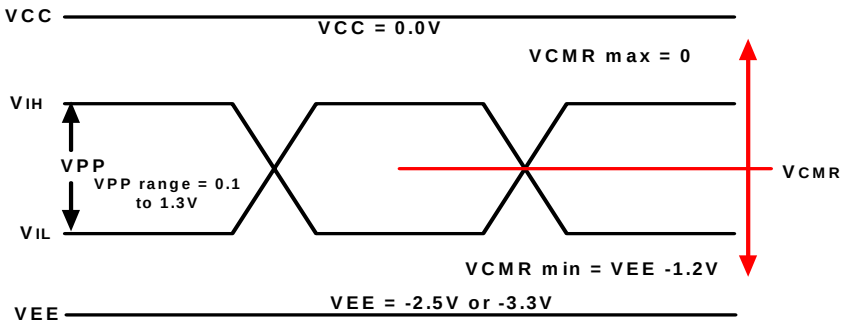


Figure 2. ECL Differential Waveform Definitions

Note:
13. Output pulse skew is the absolute difference of the propagation delay times: | tPLH – tPHL |.

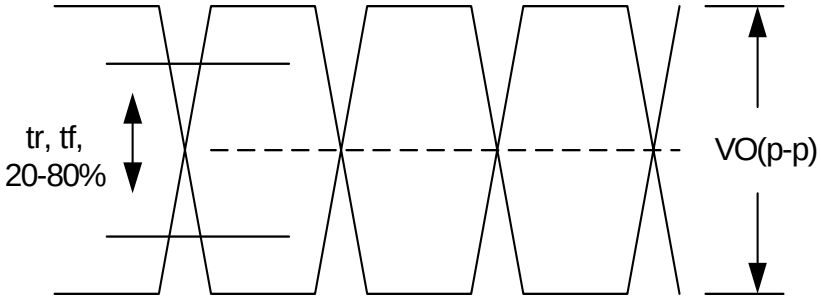


Figure 3. Rise and Fall Time with Reference to the Output

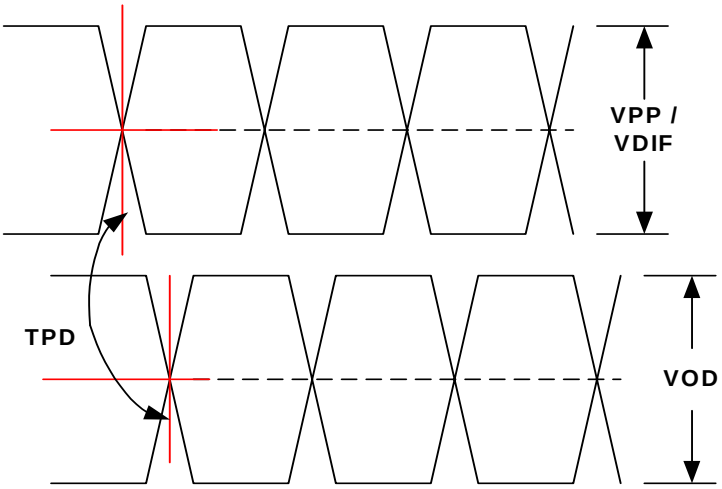
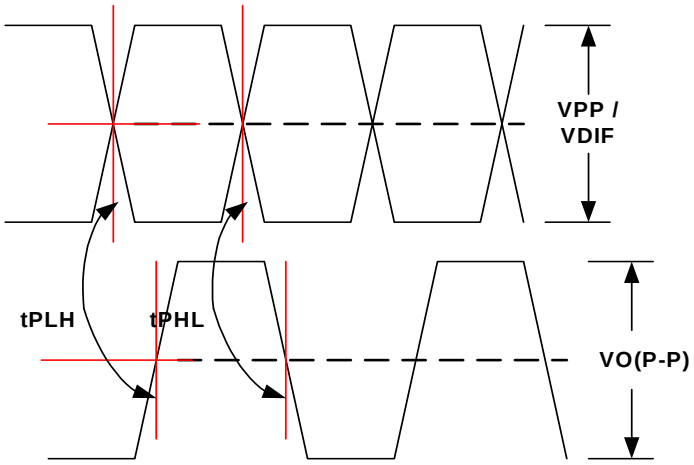


Figure 4. TPD Propagation Delay of Both CLKA or CLKA to QA((0:9),#),QB((0:9),#) Pair ECL/PECL to ECL/PECL



tsk(P) Output pulse skew = | tPLH - tPHL |

Figure 5. Output Pulse Skew

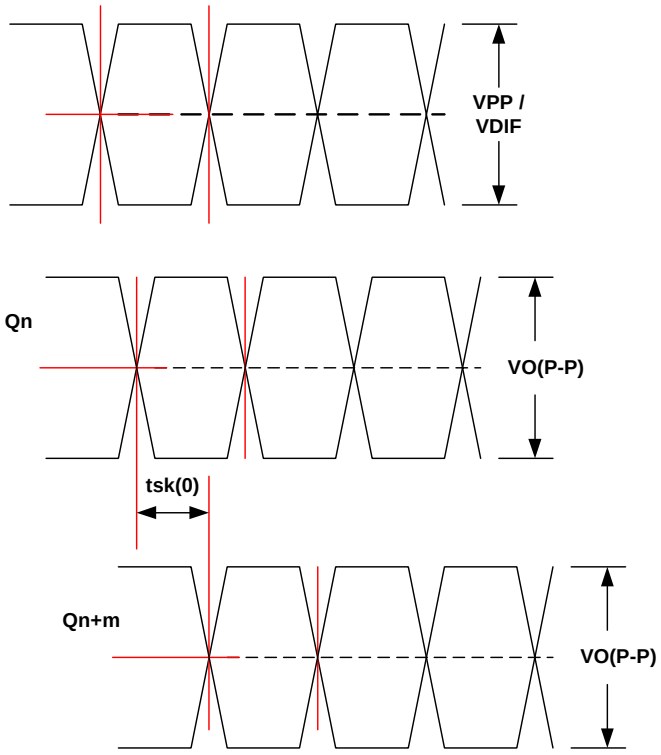


Figure 6. Output-to-Output Skew

Test Configurations

Standard test load using a differential pulse generator and differential measurement instrument.

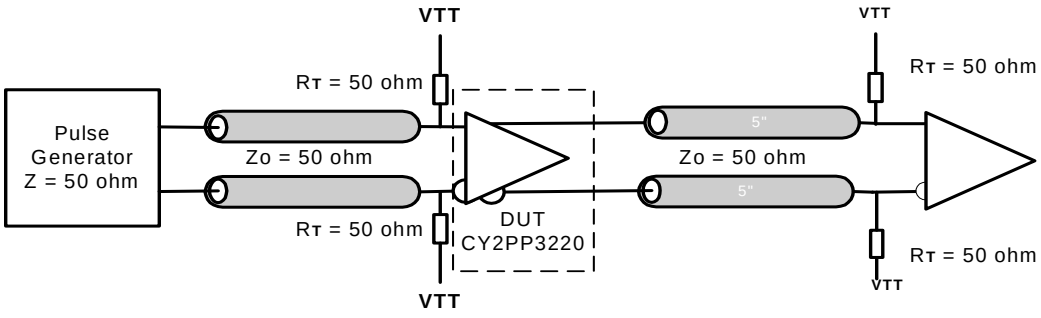


Figure 7. CY2PP3220 AC Test Reference

Applications Information

Termination Examples

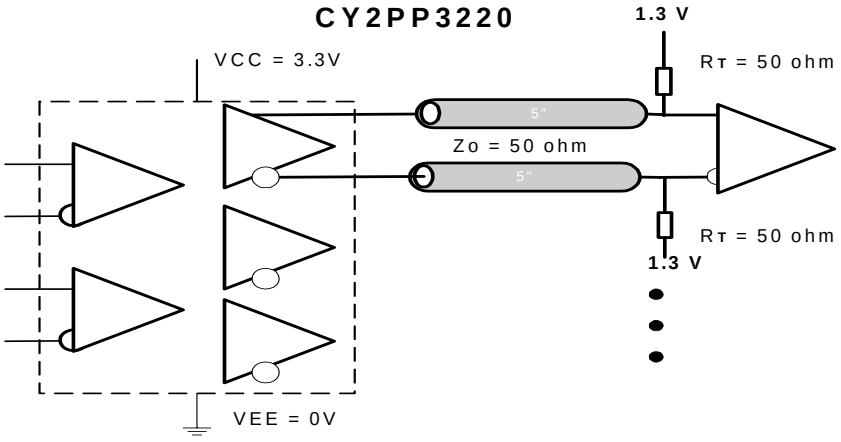


Figure 8. Standard LVPECL – PECL Output Termination

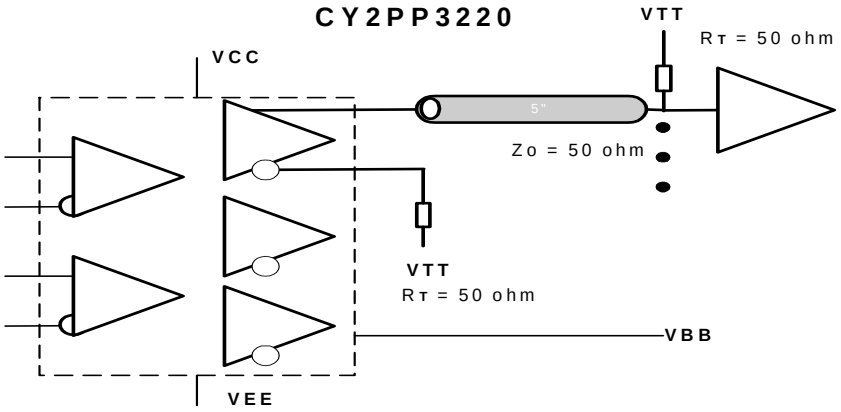


Figure 9. Driving a PECL Single-Ended Input

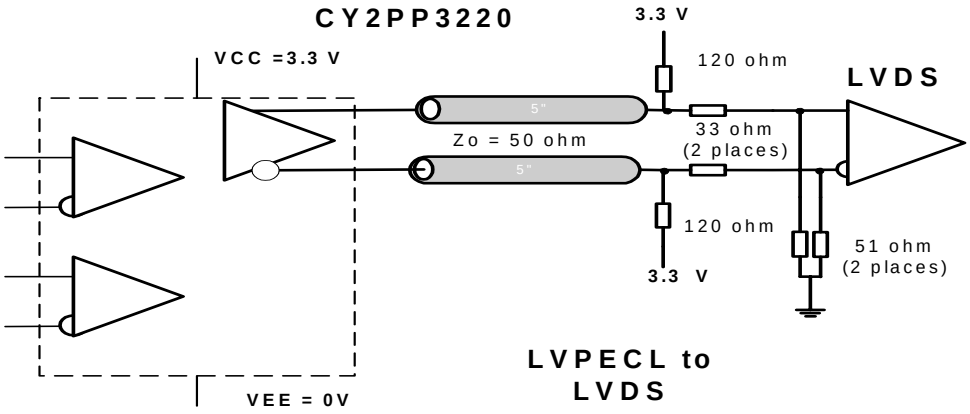


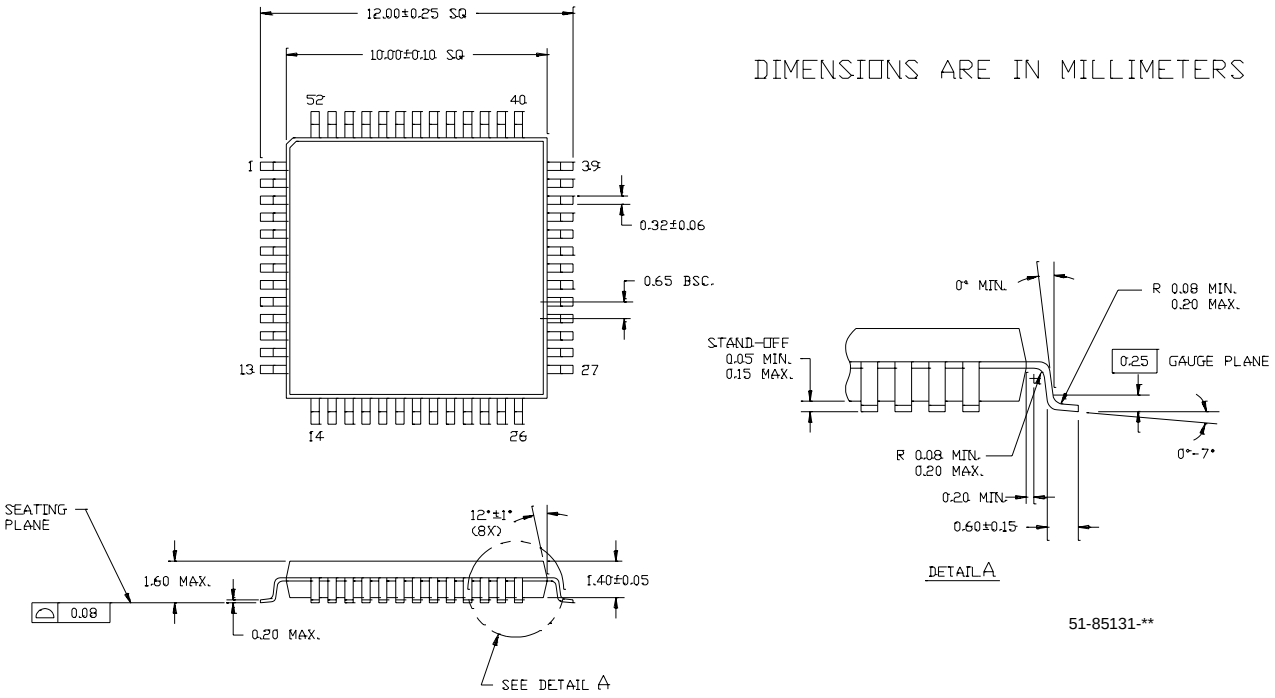
Figure 10. Low-Voltage Positive Emitter-coupled Logic (LVPECL) to a Low-Voltage Differential Signaling (LVDS) Interface

Ordering Information

Part Number	Package Type	Product Flow
CY2PP3220AI	52-pin TQFP	Industrial, –40° to 85°C
CY2PP3220AIT	52-pin TQFP – Tape and Reel	Industrial, –40° to 85°C

Package Drawing and Dimensions

52-lead Thin Plastic Quad Flat Pack (10 x 10 x 1.4 mm) A52



Document History Page

Document Title: CY2PP3220 FastEdge™ Series Dual 1:10 Differential Fanout Buffer Document Number: 38-07513				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	122437	02/13/03	RGL	New Data Sheet
*A	125459	04/16/03	RGL	Interchanged Pin 30 and 31 from QB0 /QB0# to QB0#/QB0 Changed the title to FastEdge™ Series Dual 1:10 Differential Fanout Buffer