



## 256K x 16 Static RAM

### Features

- **Low voltage range:**  
— CY62146V18: 1.75V–1.95V
- **Ultra-low active, standby power**
- **Easy memory expansion with CE and OE features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

### Functional Description

The CY62146V18 is a high-performance CMOS static RAM organized as 262,144 words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (CE HIGH). The input/output pins (I/O<sub>0</sub> through

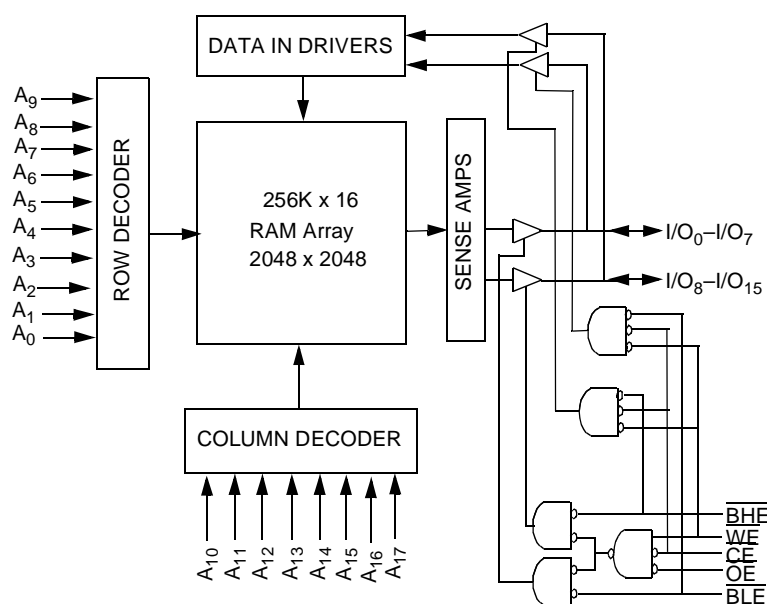
I/O<sub>15</sub>) are placed in a high-impedance state when deselected (CE HIGH), outputs are disabled ( $\overline{OE}$  HIGH),  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation (CE LOW, and WE LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

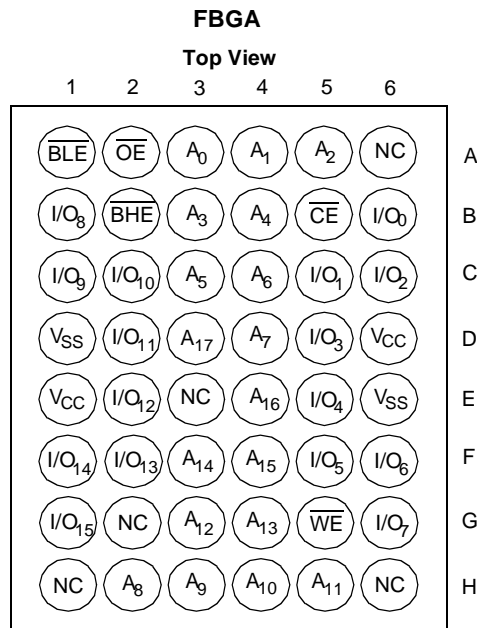
The CY62146V18 is available in 48-Ball FBGA packaging.

### Logic Block Diagram



MoBL2 and More Battery Life are trademarks of Cypress Semiconductor Corporation.

## Pin Configurations



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +2.4V

DC Voltage Applied to Outputs

in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub>
CY62146V18	Industrial	-40°C to +85°C	1.75V to 1.95V

## Product Portfolio

Product	V <sub>CC</sub> Range			Power	Power Dissipation (Industrial)			
					Operating (I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )	
	V <sub>CC(min.)</sub>	V <sub>CC(typ.)</sub> <sup>[2]</sup>	V <sub>CC(max.)</sub>		Typ. <sup>[2]</sup>	Maximum	Typ. <sup>[2]</sup>	Maximum
CY62146V18	1.75V	1.80V	1.95V	Std	3 mA	7 mA	20 µA	50 µA

### Notes:

1. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CY62146V18			Unit	
				Min.	Typ. <sup>[2]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = −0.1 mA	V <sub>CC</sub> = 1.75V	1.5			V	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	V <sub>CC</sub> = 1.75V			0.2	V	
V <sub>IH</sub>	Input HIGH Voltage		V <sub>CC</sub> = 1.95V	1.4		V <sub>CC</sub> + 0.3V	V	
V <sub>IL</sub>	Input LOW Voltage		V <sub>CC</sub> = 1.75V	−0.5		0.4	V	
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		−1	±1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		−1	+1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS Levels	V <sub>CC</sub> = 1.95V		7	15	mA	
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA	
I <sub>SB1</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = f <sub>MAX</sub>				100	μA	
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = 0	V <sub>CC</sub> = 1.95V	Std.		20	50	μA

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ.)</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

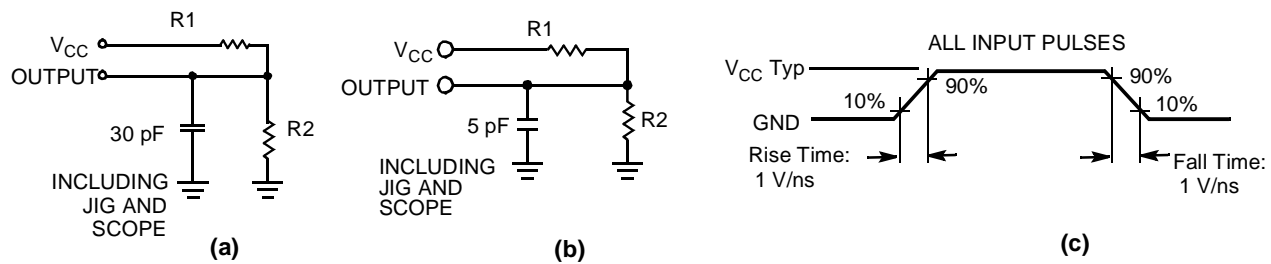
**Thermal Resistance**

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient) <sup>[3]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ <sub>JA</sub>	55	°C/W
Thermal Resistance (Junction to Case) <sup>[3]</sup>		Θ <sub>JC</sub>	16	°C/W

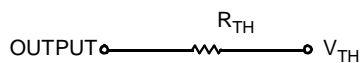
**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameters	1.8V	Unit
R1	15294	Ohms
R2	11300	Ohms
$R_{TH}$	6500	Ohms
$V_{TH}$	0.85V	Volts

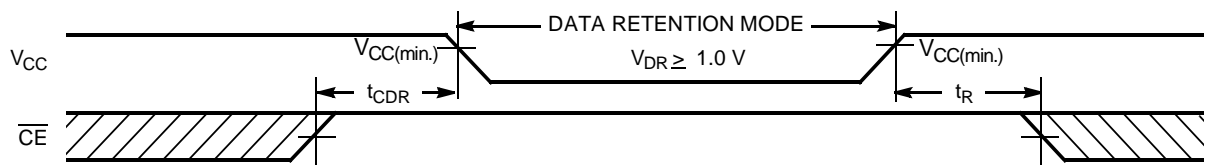
## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.0		1.95	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.0V$ $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ No input may exceed $V_{CC} + 0.3V$	Std	10	25	$\mu A$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[4]}$	Operation Recovery Time		85			ns

### Note:

4. Full Device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 10 \mu s$  or stable  $V_{CC(min.)} \geq 10 \mu s$ .

## Data Retention Waveform



**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

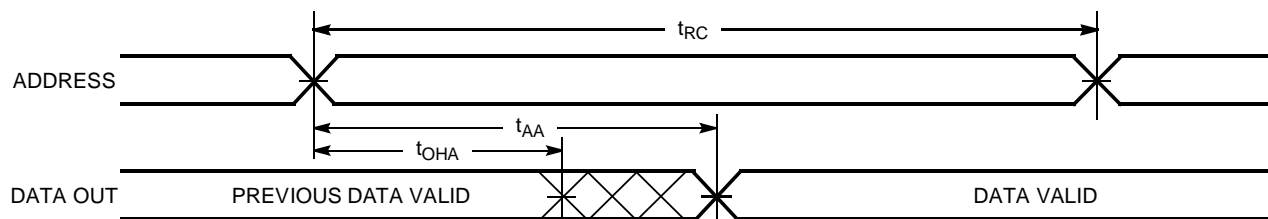
Parameter	Description	85 ns		Unit
		Min.	Max.	
READ CYCLE				
t <sub>RC</sub>	Read Cycle Time	85		ns
t <sub>AA</sub>	Address to Data Valid		85	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid		85	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		45	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low Z <sup>[6, 7]</sup>	5		ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High Z <sup>[7]</sup>		25	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low Z <sup>[6]</sup>	10		ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High Z <sup>[6, 7]</sup>		25	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to Power-Up	0		ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to Power-Down		85	ns
t <sub>DBE</sub>	$\overline{\text{BHE}}$ / $\overline{\text{BLE}}$ LOW to Data Valid		45	ns
t <sub>LZBE</sub>	$\overline{\text{BHE}}$ / $\overline{\text{BLE}}$ LOW to Low Z	5		ns
t <sub>HZBE</sub>	$\overline{\text{BHE}}$ / $\overline{\text{BLE}}$ HIGH to High Z		25	ns
WRITE CYCLE <sup>[8, 9]</sup>				
t <sub>WC</sub>	Write Cycle Time	85		ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	75		ns
t <sub>AW</sub>	Address Set-Up to Write End	75		ns
t <sub>HA</sub>	Address Hold from Write End	0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	65		ns
t <sub>BW</sub>	$\overline{\text{BHE}}$ / $\overline{\text{BLE}}$ Pulse Width	75		ns
t <sub>SD</sub>	Data Set-Up to Write End	45		ns
t <sub>HD</sub>	Data Hold from Write End	0		ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High Z <sup>[6, 7]</sup>		35	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low Z <sup>[6]</sup>	10		ns

**Notes:**

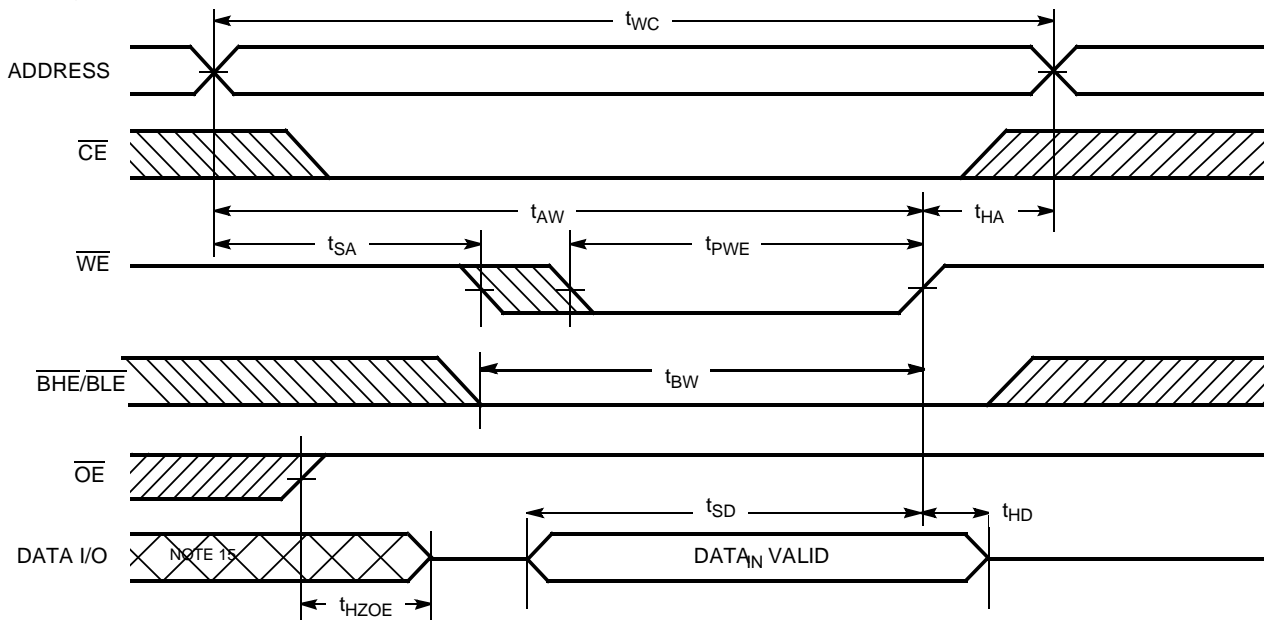
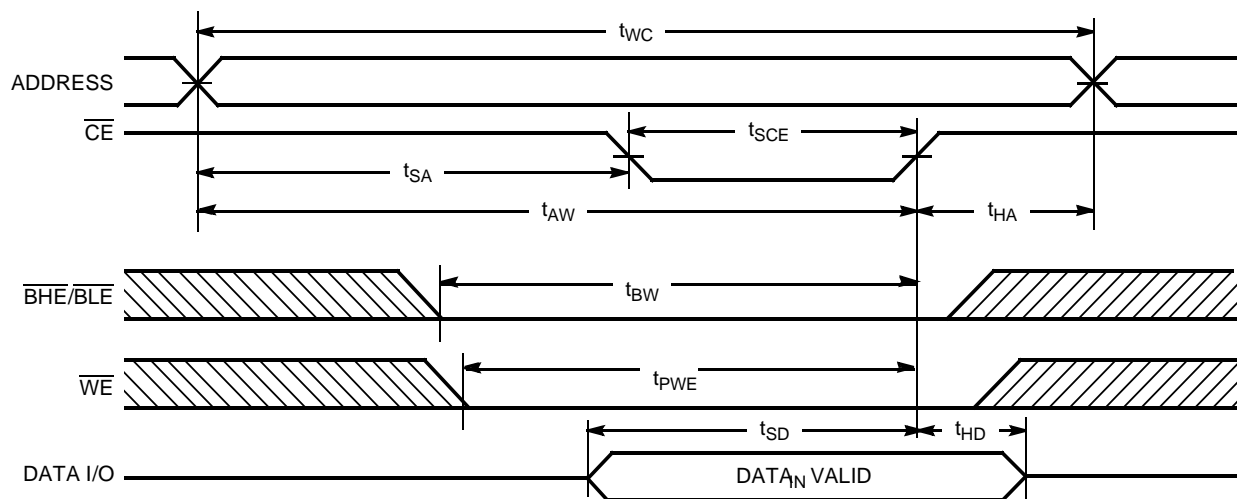
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V<sub>CC(typ.)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle #3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.



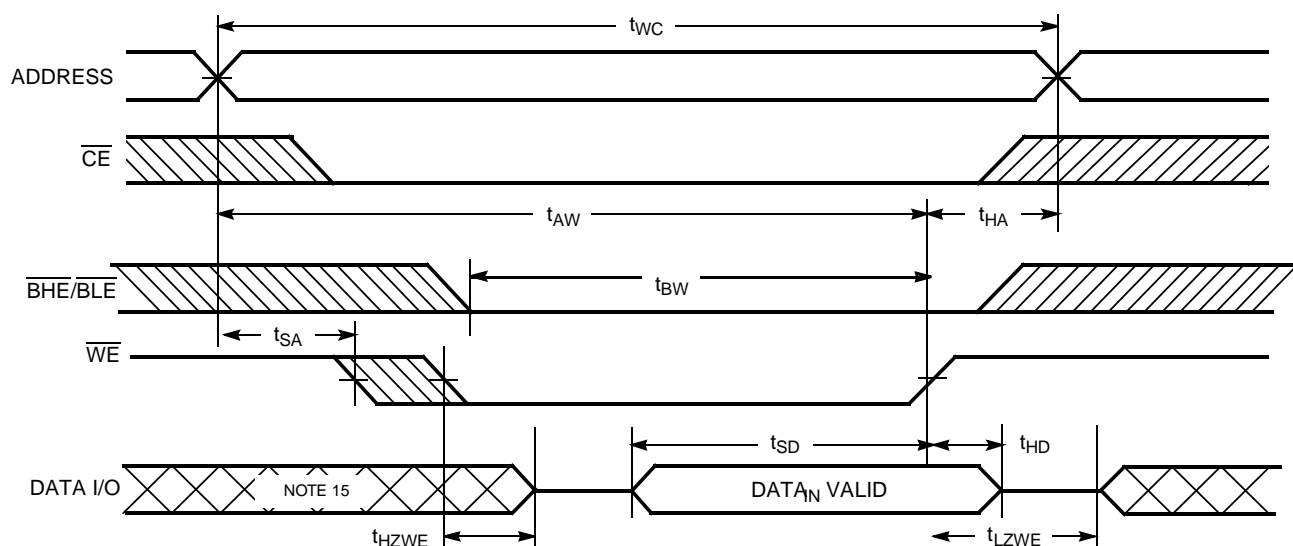
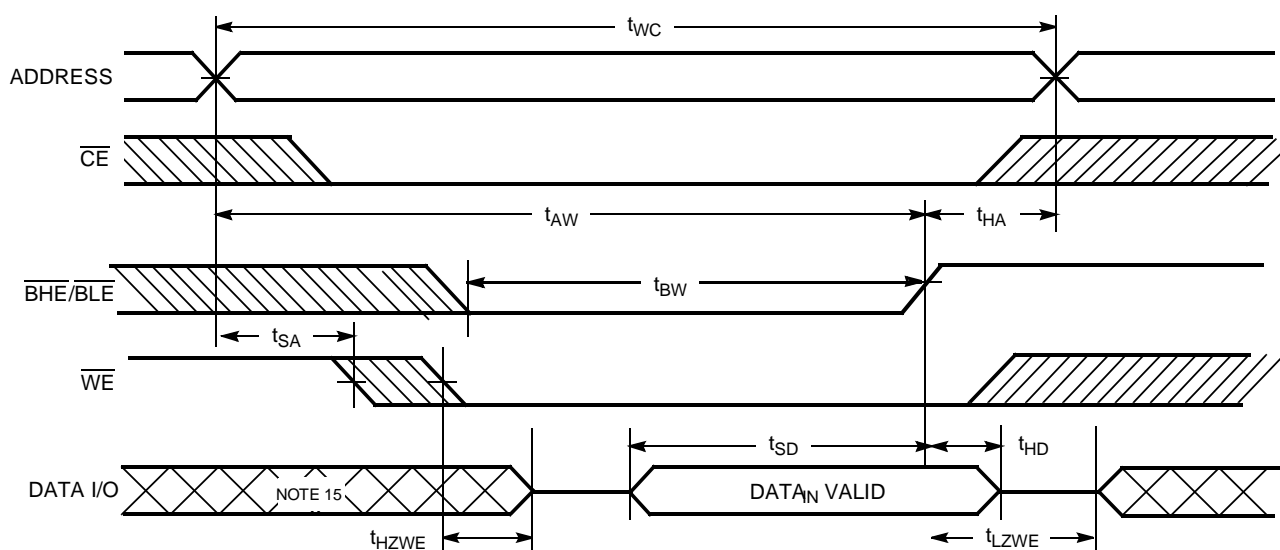
### Read Cycle No. 1<sup>[10, 11]</sup>



10. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

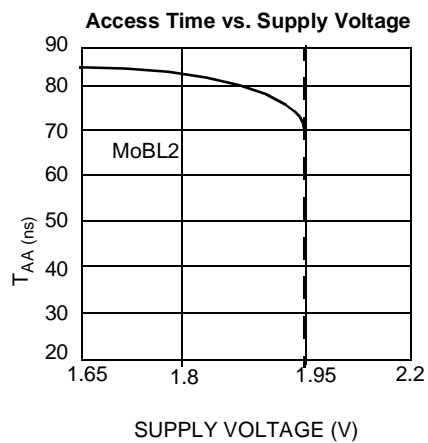
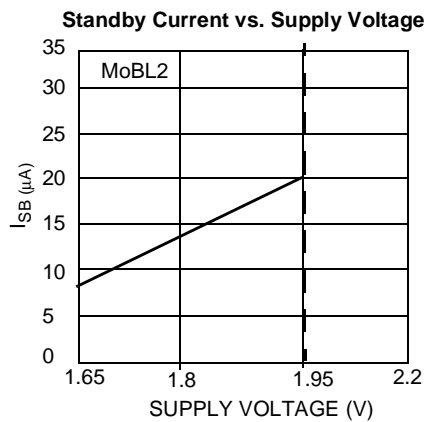
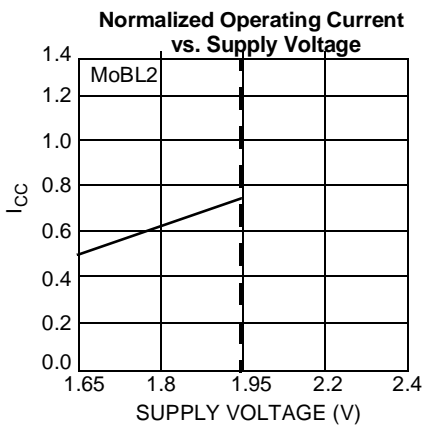
**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)** <sup>[8, 13, 14]</sup>

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)** <sup>[8, 13, 14]</sup>

**Notes:**

13. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[9, 14]</sup>**

**Write Cycle No. 4 ( $\overline{\text{BHE/BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[15]</sup>**




## Typical DC and AC Characteristics



## Truth Table

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	L	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write	Active ( $I_{CC}$ )
L	L	X	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )

## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
85	CY62146V18 -85BAI	BA49	48-Ball Fine Pitch BGA	Industrial

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## Package Diagrams

### 48-Ball (7.00 mm x 8.5 mm x 1.10 mm) Fine Pitch BGA BA49

