

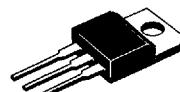
**VN46AFD****N-Channel Enhancement-Mode  
MOS Transistor**
 Siliconix  
incorporated

T-39-07

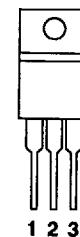
**PRODUCT SUMMARY**

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ ( $\Omega$ )	$I_D$ (A)
40	3	1.46

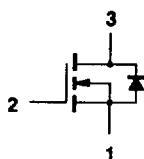
TO-220SD



FRONT VIEW



Performance Curves: VNDQ06


 1 SOURCE  
 2 GATE  
 3 & TAB - DRAIN
**ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$  Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage	$T_C = 25^\circ\text{C}$	$V_{DS}$	40	V
Gate-Source Voltage		$V_{GS}$	$\pm 30$	
Continuous Drain Current	$T_C = 25^\circ\text{C}$	$I_D$	1.46	A
			0.92	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	3	W
Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	15	
			6	
Operating Junction Temperature Range		$T_J$	-55 to 150	°C
Storage Temperature Range		$T_{stg}$	-55 to 150	
Lead Temperature (1/16" from case for 10 sec.)		$T_L$	300	

**THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE		SYMBOL	LIMITS	UNITS
Junction-to-Case		$R_{thJC}$	8.3	K/W

<sup>1</sup>Pulse width limited by maximum junction temperature

SPECIFICATIONS <sup>a</sup>			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP <sup>b</sup>	MIN	MAX	UNIT
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 10 \mu A, V_{GS} = 0 V$	70	40		V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1 mA$	1.5	0.8	2.5	
Gate-Body Leakage	$I_{GSS}$	$V_{GS} = \pm 15 V, V_{DS} = 0 V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40 V, V_{GS} = 0 V$			10	$\mu A$
		$V_{DS} = 32 V, V_{GS} = 0 V, T_C = 125^\circ C$			500	
On-State Drain Current <sup>c</sup>	$I_{D(ON)}$	$V_{DS} = 10 V, V_{GS} = 10 V$	1.8	1		A
		$V_{GS} = 5 V, I_D = 0.3 A$	1.8		5	
Drain-Source On-Resistance <sup>c</sup>	$r_{DS(ON)}$	$V_{GS} = 10 V, I_D = 1 A$	1.3		3	$\Omega$
		$T_C = 125^\circ C$	2.6		6	
Forward Transconductance <sup>c</sup>	$g_{FS}$	$V_{DS} = 10 V, I_D = 0.5 A$	350	170		mS
Common Source Output Conductance <sup>c</sup>	$g_{OS}$	$V_{DS} = 10 V, I_D = 0.1 A$	1100			$\mu S$
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz$	35		50	pF
Output Capacitance	$C_{oss}$		25		65	
Reverse Transfer Capacitance	$C_{rss}$		5		10	
<b>SWITCHING</b>						
Turn-On Time	$t_{ON}$	$V_{DD} = 25 V, R_L = 32 \Omega, I_D = 1 A$ $V_{GEN} = 10 V, R_G = 25 \Omega$ (Switching time is essentially independent of operating temperature)	8		15	nS
Turn-Off Time	$t_{OFF}$		9.5		15	

## NOTES:

- a.  $T_C = 25^\circ C$  unless otherwise noted.
- b. For design aid only, not subject to production testing.
- c. Pulse test;  $PW = \leq 300 \mu s$ , duty cycle  $\leq 2\%$ .