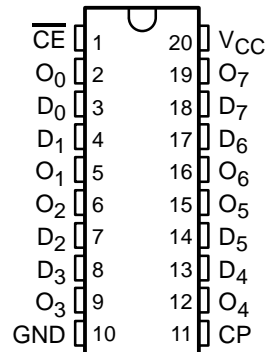
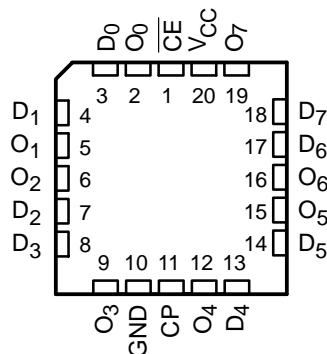


- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- Clock Enable for Address and Data Synchronization Application
- Eight Edge-Triggered D-Type Flip-Flops
- CY54FCT377T
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT377T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current

SN74FCT377T . . . Q OR SO PACKAGE  
(TOP VIEW)



SN54FCT377T . . . L PACKAGE  
(TOP VIEW)



## description

The 'FCT377T devices have eight triggered D-type flip-flops with individual data (D) inputs. The common buffered clock (CP) inputs load all flip-flops simultaneously when the clock-enable ( $\overline{CE}$ ) input is low. The register is fully edge triggered. The state of each D input at one setup time before the low-to-high clock transition is transferred to the corresponding flip-flop output (O).  $\overline{CE}$  must be stable only one setup time prior to the low-to-high clock transition for predictable operation.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



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**TEXAS  
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CY54FCT377T, CY74FCT377T  
8-BIT REGISTERS

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ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.2	CY74FCT377CTQCT	FCT377C
	SOIC – SO	Tube	5.2	CY74FCT377CTSOC	FCT377C
		Tape and reel	5.2	CY74FCT377CTSOCT	
	QSOP – Q	Tape and reel	7.2	CY74FCT377ATQCT	FCT377A
	SOIC – SO	Tube	7.2	CY74FCT377ATSOC	FCT377A
		Tape and reel	7.2	CY74FCT377ATSOCT	
–55°C to 125°C	LCC – L	Tape and reel	13	CY74FCT377TQCT	FCT377
		Tube	5.5	CY54FCT377CTLMB	
		Tube	8.3	CY54FCT377ATLMB	

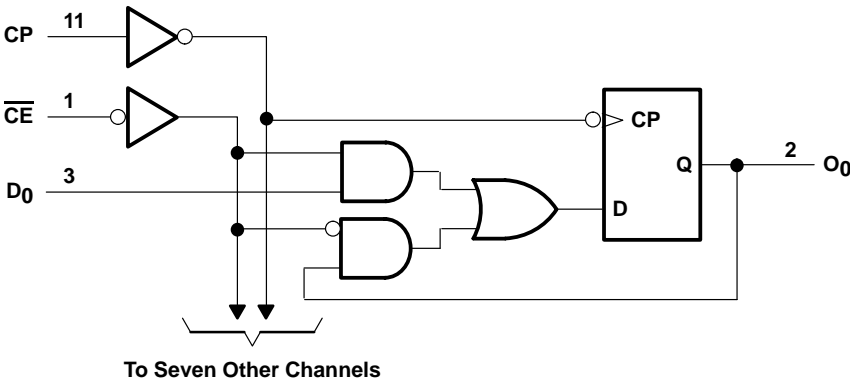
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE

INPUTS			OUTPUT O	OPERATING MODE
CP	CE	D		
↑	L	h	H	Load 1
↑	L	L	L	Load 0
↑	h	X	No change	Hold
X	H	X		

H = High logic level, h = High logic level one setup time prior to the low-to-high clock transition, L = Low logic level, l = Low logic level one setup time prior to the low-to-high clock transition, X = Don't care, ↑ = Low-to-high clock transition

logic diagram



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential .....	–0.5 V to 7 V
DC input voltage range .....	–0.5 V to 7 V
DC output voltage range .....	–0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package .....	68°C/W
SO package .....	58°C/W
Ambient temperature range with power applied, $T_A$ .....	–65°C to 135°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 2)**

	CY54FCT377T			CY74FCT377T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$I_{OH}$ High-level output current			–12			–32	mA
$I_{OL}$ Low-level output current			32			64	mA
$T_A$ Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

# CY54FCT377T, CY74FCT377T

## 8-BIT REGISTERS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	CY54FCT377T			CY74FCT377T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_{IN} = -18 \text{ mA}$	-0.7	-1.2					V
	$V_{CC} = 4.75 \text{ V}$ , $I_{IN} = -18 \text{ mA}$				-0.7	-1.2		
$V_{OH}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -12 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75 \text{ V}$	$I_{OH} = -32 \text{ mA}$			2			
		$I_{OH} = -15 \text{ mA}$			2.4	3.3		
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 32 \text{ mA}$	0.3	0.55					V
	$V_{CC} = 4.75 \text{ V}$ , $I_{OL} = 64 \text{ mA}$				0.3	0.55		
$V_{hys}$	All inputs	0.2			0.2			V
$I_I$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = V_{CC}$		5					$\mu\text{A}$
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} = V_{CC}$					5		
$I_{IH}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 2.7 \text{ V}$		$\pm 1$					$\mu\text{A}$
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} = 2.7 \text{ V}$					$\pm 1$		
$I_{IL}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0.5 \text{ V}$		$\pm 1$					$\mu\text{A}$
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} = 0.5 \text{ V}$					$\pm 1$		
$I_{OS}^\ddagger$	$V_{CC} = 5.5 \text{ V}$ , $V_{OUT} = 0 \text{ V}$	-60	-120	-225				mA
	$V_{CC} = 5.25 \text{ V}$ , $V_{OUT} = 0 \text{ V}$				-60	-120	-225	
$I_{off}$	$V_{CC} = 0 \text{ V}$ , $V_{OUT} = 4.5 \text{ V}$		$\pm 1$			$\pm 1$		$\mu\text{A}$
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} \leq 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.1	0.2					mA
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} \leq 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.1	0.2		
$\Delta I_{CC}$	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 3.4 \text{ V}^\S$ , $f_1 = 0$ , Outputs open	0.5	2					mA
	$V_{CC} = 5.25 \text{ V}$ , $V_{IN} = 3.4 \text{ V}^\S$ , $f_1 = 0$ , Outputs open				0.5	2		

† Typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4 \text{ V}$ ); all other inputs at  $V_{CC}$  or GND

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS			CY54FCT377T			CY74FCT377T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I <sub>CCD</sub> ¶	V <sub>CC</sub> = 5.5 V, Outputs open, One bit switching at 50% duty cycle, $\overline{CE}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V				0.06	0.12				mA/ MHz
	V <sub>CC</sub> = 5.25 V, Outputs open, One bit switching at 50% duty cycle, $\overline{CE}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V							0.06	0.12	
I <sub>C</sub> #	V <sub>CC</sub> = 5.5 V, Outputs open, f <sub>0</sub> = 10 MHz, $\overline{CE}$ = GND	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V		0.7	1.4				mA
			V <sub>IN</sub> = 3.4 V or GND		1.2	3.4				
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V		1.6	3.2				
			V <sub>IN</sub> = 3.4 V or GND		3.9	12.2				
	V <sub>CC</sub> = 5.25 V, Outputs open, f <sub>0</sub> = 10 MHz, $\overline{CE}$ = GND	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V				0.7	1.4		
			V <sub>IN</sub> = 3.4 V or GND				1.2	3.4		
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V				1.6	3.2		
			V <sub>IN</sub> = 3.4 V or GND				3.9	12.2		
C <sub>i</sub>					5	10		5	10	pF
C <sub>O</sub>					9	12		9	12	pF

† Typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

¶ This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4$  V)

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.

# CY54FCT377T, CY74FCT377T 8-BIT REGISTERS

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**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

			CY54FCT377AT CY54FCT377CT		CY74FCT377T CY74FCT377AT CY74FCT377CT		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, CP high or low <sup>†</sup>		7		6		ns
t <sub>su</sub>	Setup time, high or low		Data before CP <sup>↑</sup>		2		ns
			$\overline{CE}$ before CP <sup>↑</sup>		3.5		
t <sub>h</sub>	Hold time, high or low		Data after CP <sup>↑</sup>		1.5		ns
			$\overline{CE}$ after CP <sup>↑</sup>		1.5		

<sup>†</sup> With one data channel switching,  $t_{w(L)} = t_{w(H)} = 4$  ns and  $t_r = t_f = 1$  ns.

**switching characteristics over operating free-air temperature range (see Figure 1)**

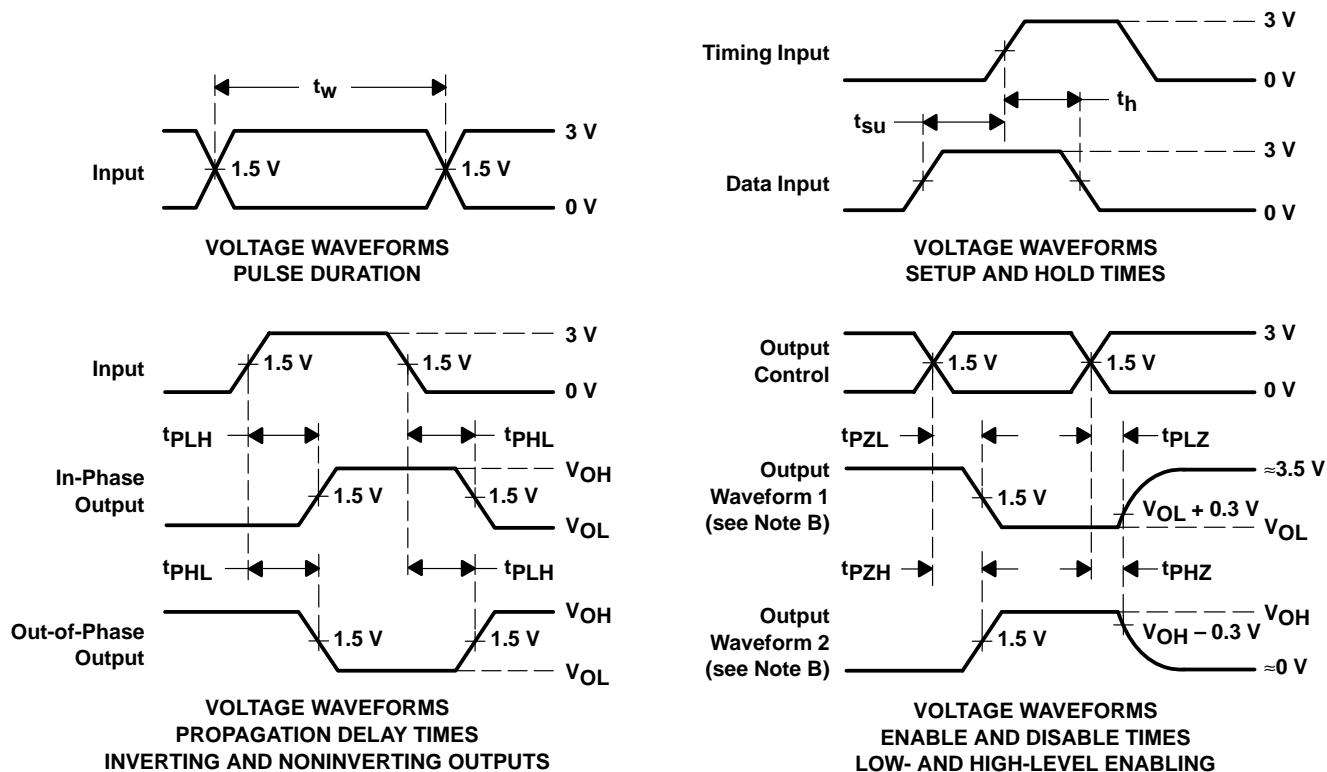
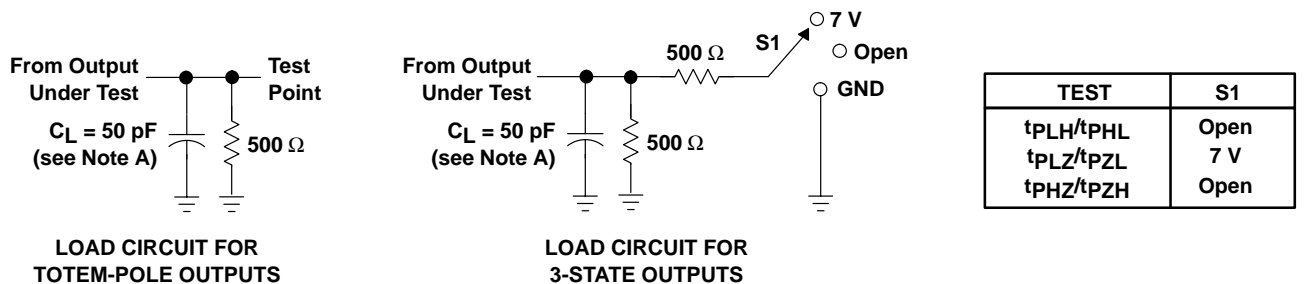
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT377AT		CY54FCT377CT		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	CP	O	2	8.3	2	5.5	ns
$t_{PHL}$			2	8.3	2	5.5	

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT377T		CY74FCT377AT		CY74FCT377CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	CP	O	2	13	2	7.2	2	5.2	ns
$t_{PHL}$			2	13	2	7.2	2	5.2	



# PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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