# CY7B173
# CY7B174

## 32K x 9 Synchronous Cache R/W RAM

### Features

- **Supports 50-MHz cache systems**
- **32K by 9 common I/O**
- **BiCMOS for optimum speed/power**
- **14-ns access delay (clock to output)**
- **Two-bit wraparound counter supporting the 486 burst sequence (7B173)**
- **Two-bit wraparound counter supporting the linear burst sequence (7B174)**
- **Separate address strobes from processor and from cache controller**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Two complementary synchronous chip selects**
- **Asynchronous output enable**

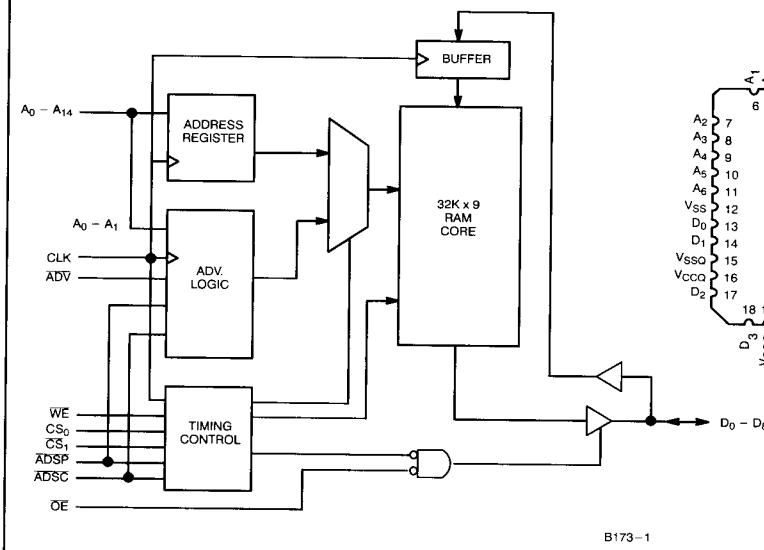
### Functional Description

The CY7B173 and CY7B174 are 32K by 9 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 14 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7B173 is designed for Intel i486-based systems; its counter follows the burst sequence of the i486. The CY7B174 is architected for other processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

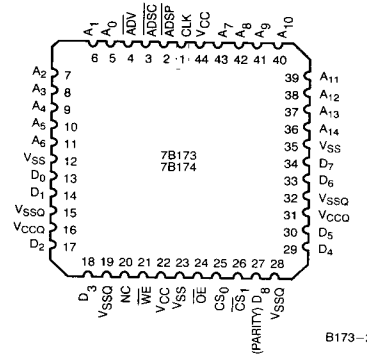
A synchronous self-timed write mechanism is provided to simplify the write interface. Two complementary synchronous chip select inputs are provided to support two banks of memory (256 Kbytes) with no external logic. These signals, in conjunction with the asynchronous output enable ($\overline{OE}$) signal, greatly simplify memory bank selection.

### Logic Block Diagram




### Pin Configurations

LCC/PLCC
Top View




### Selector Guide

| | | 7B173–14<br>7B174–14 | 7B173–18<br>7B174–18 | 7B173–21<br>7B174–21 |
|---|---|---|---|---|
| Maximum Access Time (ns) | | 14 | 18 | 21 |
| Maximum Operating Current (mA) | Commercial | 210 | 210 | 210 |
| | Military | | 230 | 230 |

## Functional Description (continued)

### Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $CS_0$ = 1 and $\overline{CS_1}$ = 0 and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at $A_0$ through $A_{14}$ is loaded into the address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic use this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7B173 and CY7B174 will be pulled LOW before the next clock rise.

If $\overline{WE}$ is LOW at the next clock rise, information presented at $D_0$ through $D_8$ will be stored into the location specified by the address advancement logic. Because the CY7B173 and CY7B174 are common I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to $D_0$ through $D_8$. As a safety precaution, the data lines ($D_0$ through $D_8$) are three-stated in the cycle where $\overline{WE}$ is sampled LOW, regardless of the state of the $\overline{OE}$ input.

### Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) $CS_0$ = 1 and $\overline{CS_1}$ = 0, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is LOW. $\overline{ADSC}$ trigger accesses are completed in a single clock cycle.

The address at $A_0$ through $A_{14}$ is loaded into the address advancement logic and delivered to the RAM core. Information presented at $D_0$ through $D_8$ will be stored into the location specified by the address advancement logic. Since the CY7B173 and CY7B174 are common I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to $D_0$ through $D_8$. As a safety precaution, the data lines ($D_0$ through $D_8$) are three-stated in the cycle where $\overline{WE}$ is sampled LOW regardless of the state of the $\overline{OE}$ input.

### Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $CS_0$ = 1 and $\overline{CS_1}$ = 0, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is HIGH. The address at $A_0$ through $A_{14}$ is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at $D_0$ through $D_8$ a maximum of 14 ns after clock rise.

## Burst Sequences

The CY7B173 provides a 2-bit wraparound counter implementing the Intel 80486 sequence (see *Table 1*). Note that the burst sequence depends on the location of the first burst address.

**Table 1. Counter Implementation for the Intel 80486 Sequence**

| First Address | | Second Address | | Third Address | | Fourth Address | |
|---|---|---|---|---|---|---|---|
| $A_X + 1$ | $A_X$ | $A_X + 1$ | $A_X$ | $A_X + 1$ | $A_X$ | $A_X + 1$ | $A_X$ |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

The CY7B174 provides a two-bit wraparound counter implementing a linear sequence (see *Table 2*).

**Table 2. Counter Implementation for a Linear Sequence**

| First Address | | Second Address | | Third Address | | Fourth Address | |
|---|---|---|---|---|---|---|---|
| $A_X + 1$ | $A_X$ | $A_X + 1$ | $A_X$ | $A_X + 1$ | $A_X$ | $A_X + 1$ | $A_X$ |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

## Application Example

*Figure 1* shows a 128-Kbyte secondary cache for the i486 using four CY7B173 cache RAMs and a CY7B181 cache tag. Address from the i486 is checked by the cache tag at the beginning of each access. Match reset is delivered to the cache controller after 12 ns.

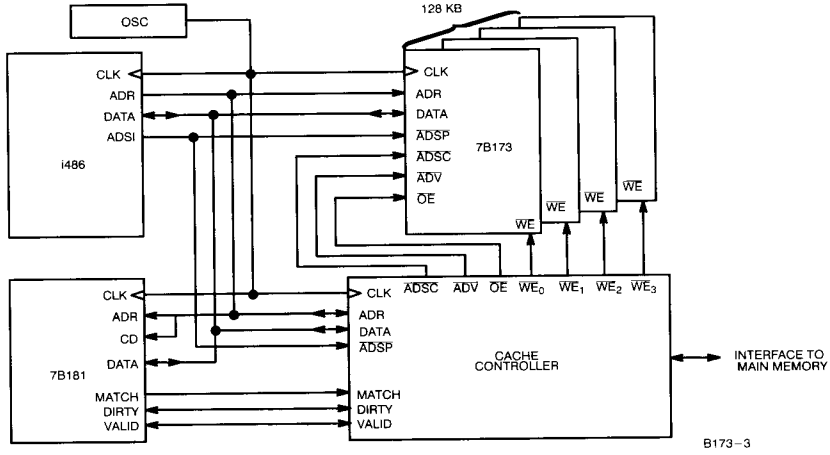



**Figure 1. Cache Using Four CY7B173s**

## Pin Definitions

| Signal Name | I/O | Description |
|---|---|---|
| $A_0 - A_{14}$ | I | Address Inputs |
| CLK | I | Clock |
| $\overline{WE}$ | I | Write Enable |
| $\overline{OE}$ | I | Output Enable |
| $CS_0$, $\overline{CS_1}$ | I | Chip Select |
| $\overline{ADV}$ | I | Address Advance |
| $\overline{ADSP}$ | I | Processor Address Strobe |
| $\overline{ADSC}$ | I | Cache Controller Address Strobe |
| $D_0 - D_8$ | I/O | Data I/O |
| $V_{CC}$ | – | +5V Power Supply |
| $V_{SS}$ | – | Ground |
| $V_{CCQ}$ | – | Output Buffer (Driver) Power Supply |
| $V_{SSQ}$ | – | Output Buffer (Driver) Ground |
| RESV | – | Reserved |

## Pin Descriptions

| | |
|---|---|
| **Input Signals** | |
| CLK | Clock signal used as the reference for most on-chip operations. |
| $\overline{ADSP}$ | Address strobe signal from the processor: $\overline{ADSP}$ is asserted when the processor address is valid. If $\overline{ADSP}$ is LOW at clock rise, the address at $A_0$ through $A_{14}$ will be loaded into the address register and the address advancement logic. The write signal, $\overline{WE}$, is ignored in the clock cycle where $\overline{ADSP}$ is asserted. If both $\overline{ADSP}$ or $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized. |
| $\overline{ADSC}$ | Address strobe signal from the cache controller: $\overline{ADSC}$ is asserted when a new address generated by the cache controller is ready to be strobed into the CY7B173/4. The write signal, $\overline{WE}$, is recognized in the clock cycle where $\overline{ADSC}$ is asserted. If both $\overline{ADSP}$ and $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized. |
| $A_0 - A_{14}$ | Address lines: These address inputs are loaded into the address register and the address advancement logic at clock rise if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. They are used to select one of the 32K locations. |
| $\overline{WE}$ | Write Enable: This signal is sampled at the rising edge of the clock signal. If $\overline{WE} = 0$, a self-timed write operation will be initiated and data on $D_0 - D_8$ will be stored into the selected memory location. The only exception occurs if both $\overline{ADSP}$ and $\overline{WE}$ are LOW at clock rise. In this case, the write signal is ignored. |
| $\overline{ADV}$ | Address Advance input: $\overline{ADV}$ is sampled at the rising edge of the clock. In the case of the CY7B173, LOW at this input will advance the address in the advancement logic according to the Intel 80486 burst sequence. In the case of the CY7B174, the addresses will be advanced linearly. This input is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is active (LOW). |
| $CS_0 - \overline{CS_1}$ | Chip Select inputs: $CS_0$ is active HIGH and $\overline{CS_1}$ is active LOW. Both inputs are sampled at clock rise if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The RAM is selected if $CS_0 = 1$ and $\overline{CS_1} = 0$. |
| $\overline{OE}$ | Output Enable: $\overline{OE}$ is an asynchronous signal that disables all output drivers ($D_0 - D_8$) when it is deasserted. $\overline{OE}$ should be deasserted during write cycles because the CY7B173/4 is a common I/O device and three-state conflict may occur at the data pins. |
| NC | No Connect: This input can be left floating or tied to $V_{SS}$ or $V_{CC}$. |
| **Bidirectional Signals** | |
| $D_0 - D_8$ | Data I/O lines: During a read cycle, if $\overline{OE}$ is asserted, data in the selected location will appear at these pins. During a write cycle, data presented at these pins is captured at clock rise and stored into the selected RAM location if $\overline{WE}$ is LOW. All nine outputs will be placed in a three-state condition when $\overline{OE}$ is deasserted, when the RAM is deselected via the chip select inputs, or during a write cycle. |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on $V_{CC}$ Relative to GND ... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to $V_{CC}$ + 0.5V

DC Input Voltage[1] ..... − 0.5V to $V_{CC}$ + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature[2] | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Military | − 55°C to +125°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | 7B173−14 7B174−14 Min. | 7B173−14 7B174−14 Max. | 7B173−18, 21 7B174−18, 21 Min. | 7B173−18, 21 7B174−18, 21 Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = − 4.0 mA | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.2 | $V_{CC}$ | 2.2 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage[1] | | | −0.5 | 0.8 | −0.5 | 0.8 | V |
| $I_{IX}$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | − 10 | +10 | − 10 | +10 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$, Output Disabled | | − 100 | +100 | − 100 | +100 | µA |
| $I_{OS}$ | Output Short Circuit Current[3] | $V_{CC}$ = Max., $V_{OUT}$ = GND | | | −300 | | −300 | mA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | Com'l | | 210 | | 210 | mA |
| | | | Mil | | | | 230 | |

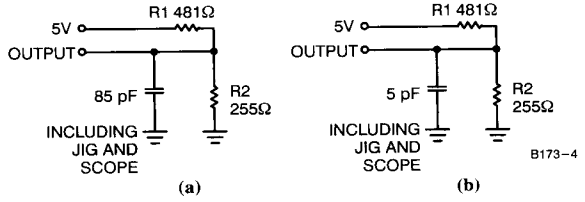
## Capacitance[4]

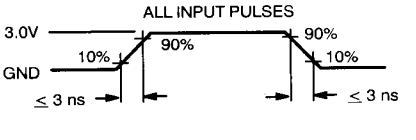
| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$: Addresses | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 4.5 | pF |
| $C_{IN}$: Other Inputs | | | 6 | pF |
| $C_{OUT}$ | Output Capacitance | | 13 | pF |

**Notes:**

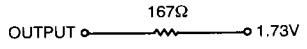
1. $V_{IL}$ (min.) = − 1.5V for pulse durations of less than 20 ns.
2. $T_A$ is the "instant on" case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters (PLCC package).

## AC Test Loads and Waveforms




Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics Over the Operating Range[5]

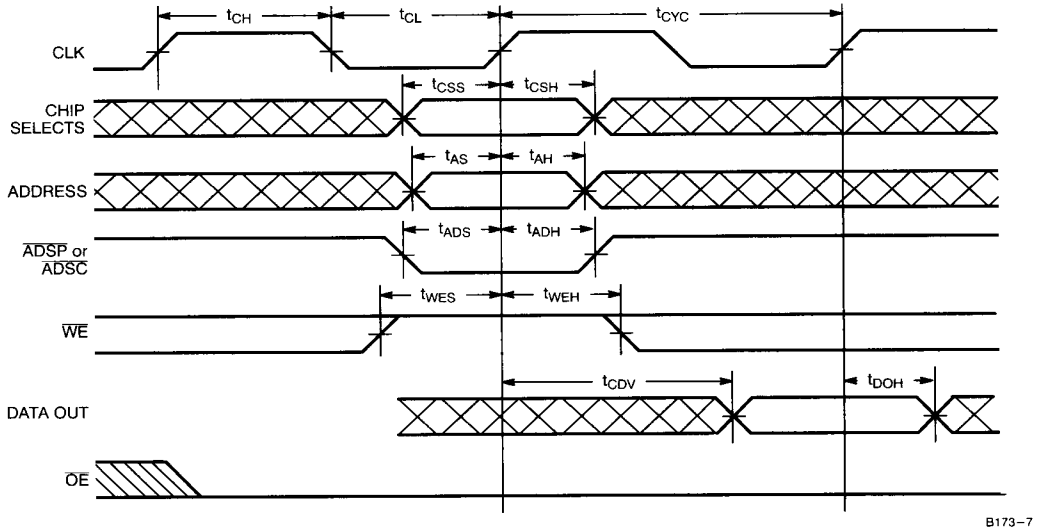
| Parameter | Description | 7B173–14 7B174–14 | | 7B173–18 7B174–18 | | 7B173–21 7B173–21 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{CYC}$ | Clock Cycle Time | 20 | | 25 | | 30 | | ns |
| $f_{MAX}$ | Maximum Frequency | | 50 | | 40 | | 33 | MHz |
| $t_{CH}$ | Clock HIGH | 8 | | 10 | | 12 | | ns |
| $t_{CL}$ | Clock LOW | 8 | | 10 | | 12 | | ns |
| $t_{AS}$ | Address Set-Up Before CLK Rise | 2 | | 4 | | 5 | | ns |
| $t_{AH}$ | Address Hold After CLK Rise | 2 | | 3 | | 4 | | ns |
| $t_{CDV}$ | Data Output Valid After CLK Rise | | 14 | | 18 | | 21 | ns |
| $t_{DOH}$ | Data Output Hold After CLK Rise | 3 | | 3 | | 3 | | ns |
| $t_{ADS}$ | $\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise | 3 | | 4 | | 5 | | ns |
| $t_{ADH}$ | $\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise | 2 | | 3 | | 4 | | ns |
| $t_{WES}$ | $\overline{WE}$ Set-Up Before CLK Rise | 3 | | 4 | | 5 | | ns |
| $t_{WEH}$ | $\overline{WE}$ Hold After CLK Rise | 2 | | 3 | | 4 | | ns |
| $t_{ADVS}$ | $\overline{ADV}$ Set-Up Before CLK Rise | 3 | | 4 | | 5 | | ns |
| $t_{ADVH}$ | $\overline{ADV}$ Hold After CLK Rise | 2 | | 3 | | 4 | | ns |
| $t_{DS}$ | Data Input Set-Up Before CLK Rise | 3 | | 4 | | 5 | | ns |
| $t_{DH}$ | Data Input Hold After CLK Rise | 2 | | 3 | | 4 | | ns |
| $t_{CSS}$ | Chip Select Set-Up | 3 | | 4 | | 5 | | ns |
| $t_{CSH}$ | Chip Select Hold After CLK Rise | 2 | | 3 | | 4 | | ns |
| $t_{CSOZ}$ | Chip Select Sampled to Output High Z[6, 7] | | 10 | | 12 | | 14 | ns |
| $t_{CSOV}$ | Chip Select Sampled to Output Valid | 3 | 14 | 3 | 18 | 3 | 21 | ns |
| $t_{EOZ}$ | $\overline{OE}$ HIGH to Output High Z[6] | | 7 | | 9 | | 11 | ns |
| $t_{EOV}$ | $\overline{OE}$ LOW to Output Valid | | 7 | | 9 | | 11 | ns |
| $t_{WEOZ}$ | $\overline{WE}$ Sampled LOW to Output High Z[6] | | 10 | | 12 | | 14 | ns |
| $t_{WEOV}$ | $\overline{WE}$ Sampled HIGH to Output Valid | 3 | 14 | 3 | 18 | 3 | 21 | ns |

**Notes:**

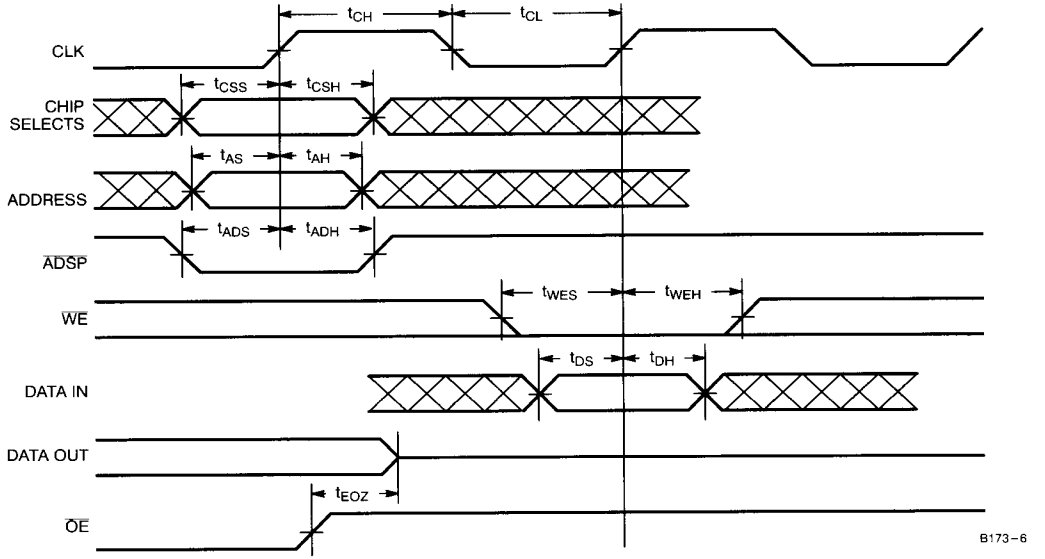
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{OL}/I_{OH}$ and 85-pF load capacitance.
6. $t_{CSOZ}$, $t_{EOZ}$, and $t_{WEOZ}$ are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
7. At any given voltage and temperature, $t_{CSOZ}$ ($t_{WEOZ}$) min. is less than $t_{CSOV}$ ($t_{WEOV}$) min.

## Switching Waveforms

### Single Read

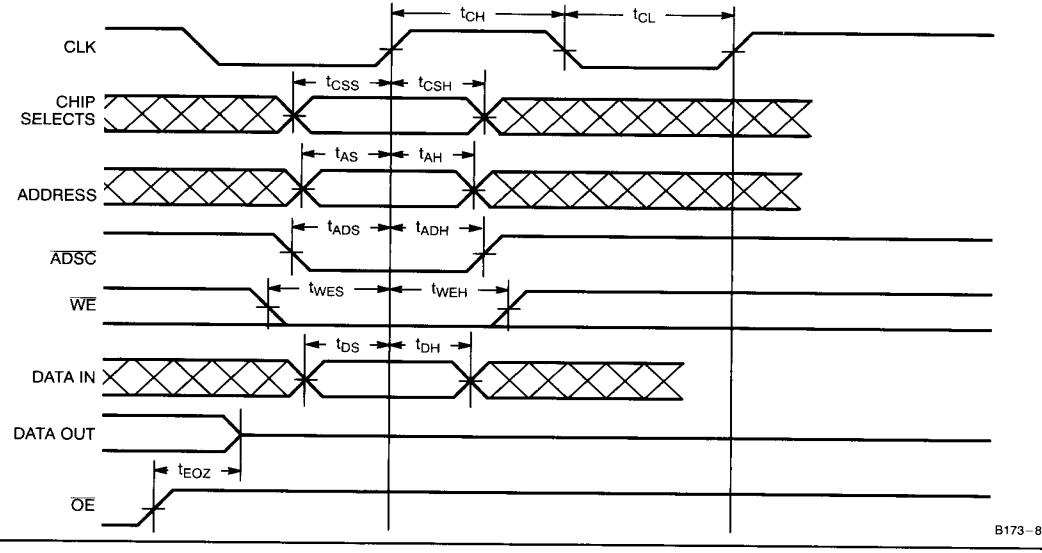



### Single 486 Write

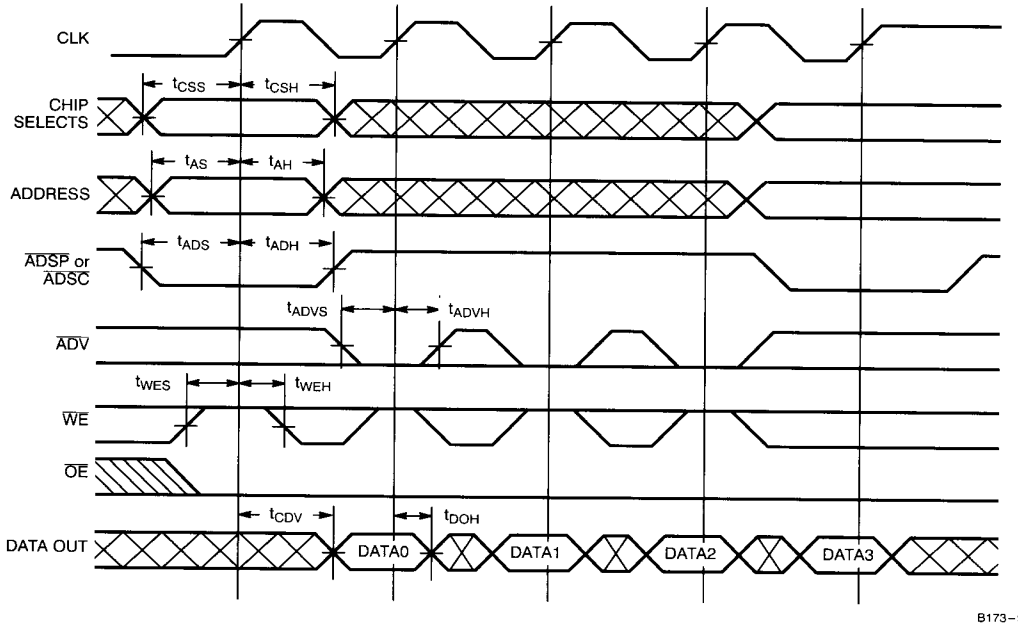


## Switching Waveforms (continued)

### Single Cache Controller Write

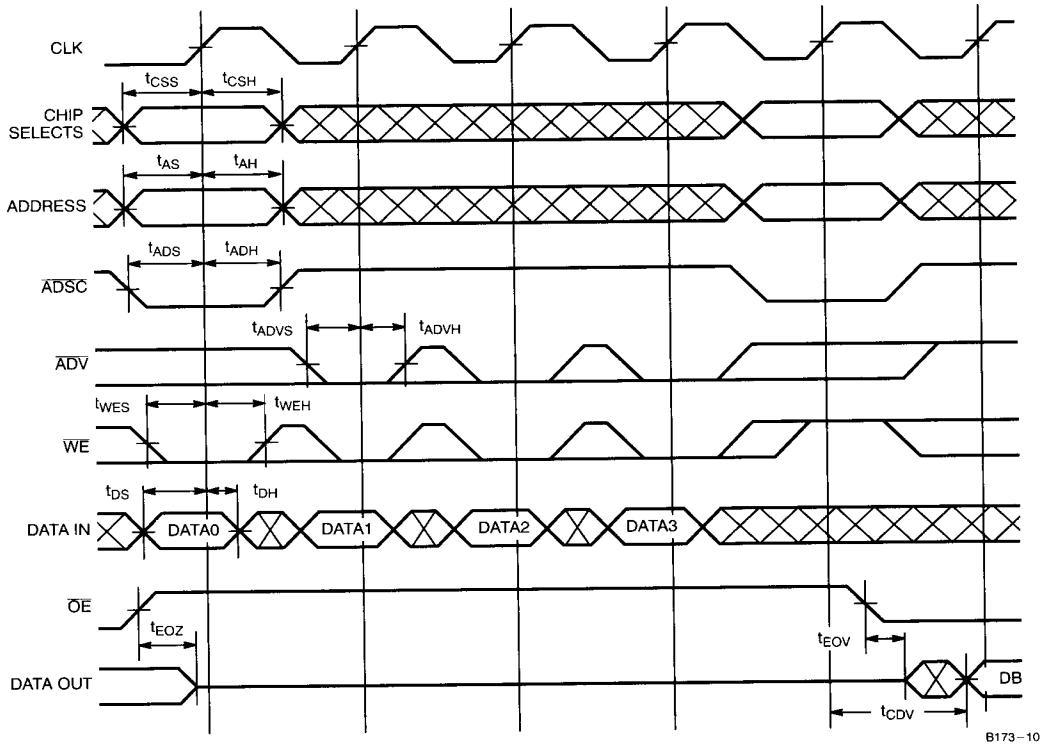



### Burst Read Sequence with Four Accesses

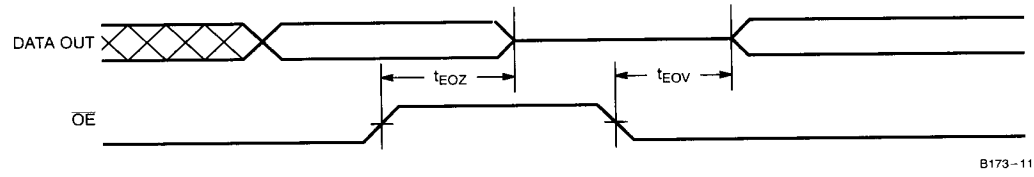


## Switching Waveforms (continued)

**Cache Controller Burst Write Sequence with Four Accesses Followed by a Single Read Cycle**

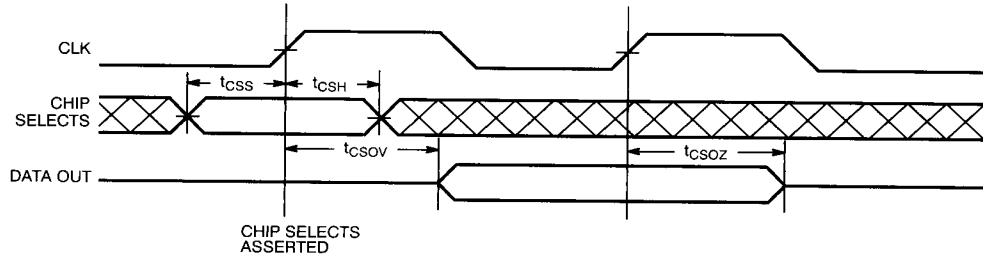



**Output (Controlled by $\overline{OE}$)**



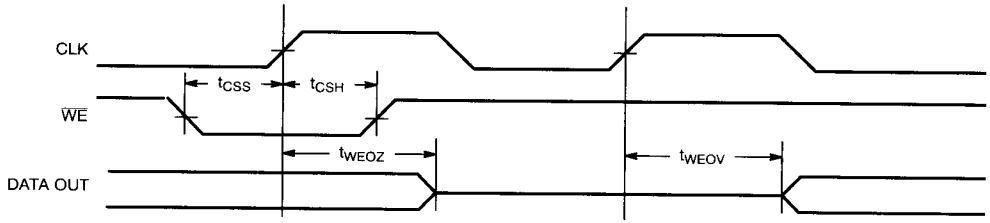
## Switching Waveforms (continued)

**Output Timing (Controlled by CS)**




B173-12

**Output Timing (Controlled by $\overline{WE}$)**




B173-13

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 14 | CY7B173-14JC | J67 | 44-Lead Plastic Leaded Chip Carrier | Commercial |
| 18 | CY7B173-18JC | J67 | 44-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7B173-18LC | L67 | 44-Square Leadless Chip Carrier | |
| | CY7B173-18LMB | L67 | 44-Square Leadless Chip Carrier | Military |
| 21 | CY7B173-21JC | J67 | 44-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7B173-21LC | L67 | 44-Square Leadless Chip Carrier | |
| | CY7B173-21LMB | L67 | 44-Square Leadless Chip Carrier | Military |

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 14 | CY7B174-14JC | J67 | 44-Lead Plastic Leaded Chip Carrier | Commercial |
| 18 | CY7B174-18JC | J67 | 44-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7B174-18LC | L67 | 44-Square Leadless Chip Carrier | |
| | CY7B174-18LMB | L67 | 44-Square Leadless Chip Carrier | Military |
| 21 | CY7B174-21JC | J67 | 44-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7B174-21LC | L67 | 44-Square Leadless Chip Carrier | |
| | CY7B174-21LMB | L67 | 44-Square Leadless Chip Carrier | Military |

Document #: 38-00154-B