Eletech

VP1870
CVSD Codec Adaptor

Features:

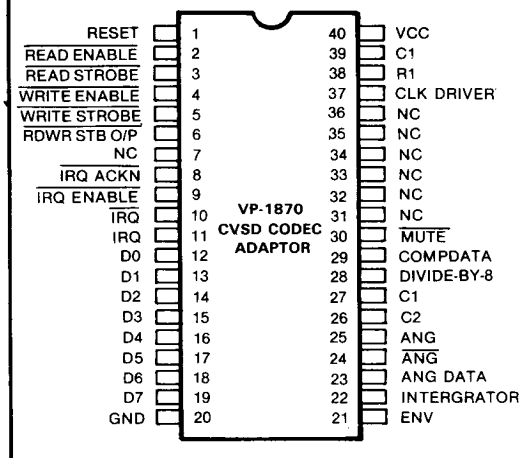
- High quality speech encoding/decoding technique
- 8-bit bidirectional interface to external CPU.
- Self-generated IRQ siganl.
- Single +3V ~ +6 Volt power supply with low power consumption
- Inexpensive RC oscillator.
- Bit rate adjustable from 9.6K to 128k bps.
- Compatible to Eletech SF-700 Filter Hybrid.
- Easy to integrate with any digital voice system.

General Description:

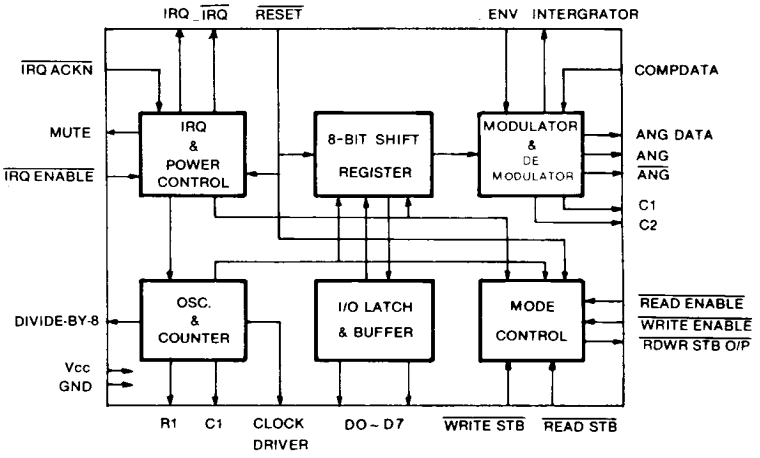
VP-1870 is a CMOS LSI for digital audio signal processing in a μp—based system. When running with Eletech's SF700 Filter Hybrid, the chip constitutes a CVSD (Continuous Variable Slope Delta Modulation) signal convertor in both encoding and decoding way. SF-700 is a voice band filter (300 ~ 3.4KHz) specially designed for VP-1870 and a limited PCB space. When VP-1870 is adapted as main component of PC voice I/O device, detailed circuit diagram is revealed for designer's reference. The related operation software is available for such development when purchasing the chip set. Once developed, the complete source code and software drivers can be licensed from Eletech for mass production.

In an "economic" digitized speech system, the sampling rate of the chip can be varied by external RC components. However, the recommended trade-off sampling rate is 32K bps which produces an acceptable level of voice quality for most of people.

Pin Assignment



Block Diagram



Absolute Maximum Ratings*

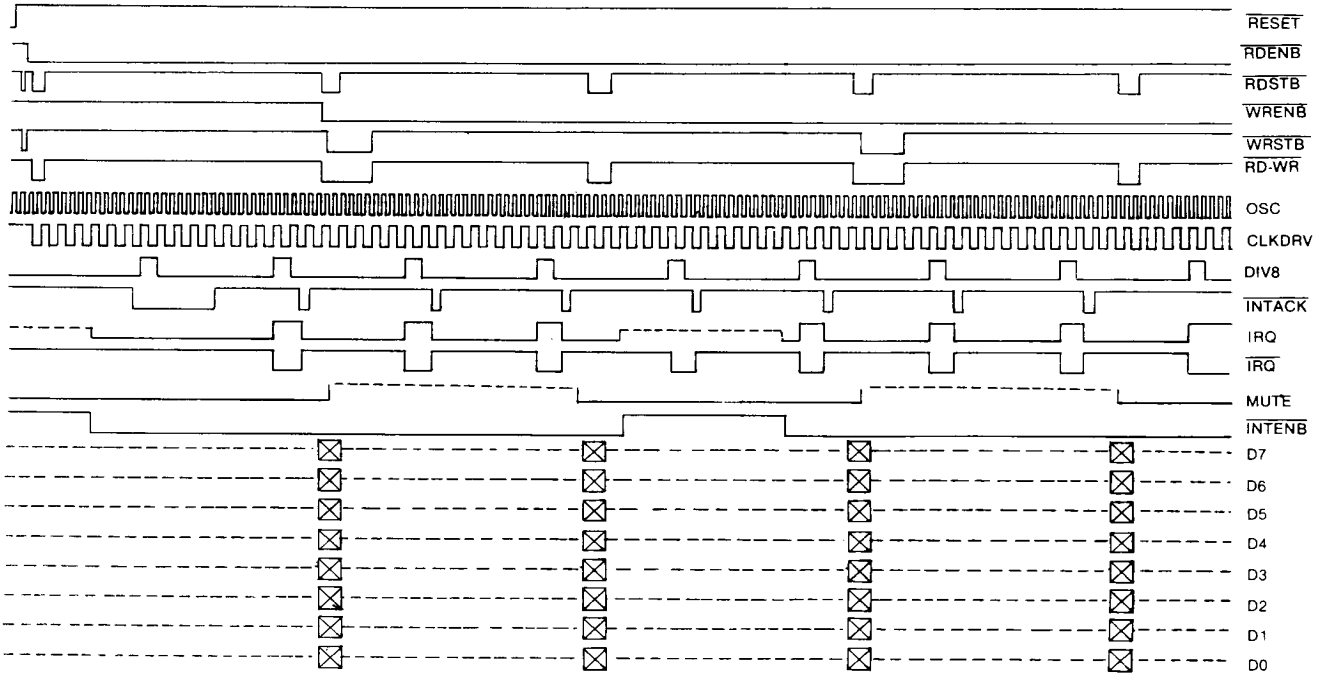
Supply Voltage, $V_{DD}-V_{SS}$.....0 to 7V
Input Voltage, V_{IN}.....V_{SS} to V_{DD}
Operating Temperature, T_{OP}..... −10°C to 60°C
Storage Temperature, T_{ST}..... −20°C to 80°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Eletrical Characteristics (V_{DD} = 5V, Fosc = 64KHz, Fciock = 32K Hz, unless otherwise specified.)

Symbol	Parameter		Limit			Units
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage		3	5	6	V
I_{DD}	Stand-by Current			50		μA
I_{drive}	Clock Drive Current		12			mA
I_{sink}	Clock Sink Current		12			mA
V_{IH}	Input Voltage	High	3.5		5	V
V_{IL}		Low	0		1.5	V
I_{drive}	Output Current	Drive	3	4		mA
I_{sink}		Sink	3	4		mA
Treset	Reset Pulse		500			nS
Tstrobe	Strobe Pulse Width		150			nS
S/N	Signal-to-Quantizied Noise (1KHz)			30		dB
Taccess	Date Accesss Time		150			nS

Timing Diagram



Pin Name Description

DO-D7:
Bidirectional Data input/output.

$\overline{\text{RESET}}$:
Input, active low. When activated, all the internal counters are cleared and the chip is disabled.

$\overline{\text{READ STROBE}}$:
Input, active low. When $\overline{\text{READ ENABLE}}$ is low, triggering on this input shall 1. put the chip into "ENCODE" mode so that the serial encoded data will be sent to internal 8-bit shift register, 2. Output the 8-bit data after acknowledgment of the IRQ signal.

$\overline{\text{READ ENABLE}}$:
Input, active low, This pin is provided to enable any valid $\overline{\text{READ STROBE}}$ signal

$\overline{\text{WRITE STROBE}}$:
Input, active low. When $\overline{\text{WRITE ENABLE}}$ is low, triggering on this input shall, 1. put the chip into "DECODE" mode so that the chip can be ready to receive the input data (DO ~ D7) 2. latch the 8-bit data into the input buffer after acknowledgement of the IRQ signal.

$\overline{\text{WRITE ENABLE}}$:
Input, active low. This pin is provided to enable any valid $\overline{\text{WRITE STROBE}}$ signal.

$\overline{\text{RD-WR STB O/P}}$:
Output, active low. This pin indicates the chip is experiencing either a valid $\overline{\text{READ STROBE}}$ or $\overline{\text{WRITE STROBE}}$ signal.

DIVIDE-BY-8:
Output, active high. When the chip is activated, this pin will generate a clock pulse each time the internal counter advances to eight.

$\overline{\text{IRQ}}$:
Output, active low. The chip will send out an IRQ signal at the rising edge of DIVIDE-BY-8 signal and wait to be reset by IRQ ACKN signal. An IRQ signal indicates that the chip is ready for the data transfer (DO-D7) either in "ENCODE" or "DECODE" mode.

IRQ
Tri-state output, active high. This pin is an inverted output of IRQ but gated by $\overline{\text{IRQ ENABLE}}$ signal.

$\overline{\text{IRQ ENABLE}}$:
Input, active low. This pin is provided to enable any valid IRQ signal.

$\overline{\text{IRQ ACKN}}$:
Input, active low. Once the IRQ signal is recognized by external microprocessor, $\overline{\text{IRQ ACKN}}$ should be received before the data bus can proceed any data exchange.

$\overline{\text{MUTE}}$:
Silent control for external audio circuit. Tri-state output, activated only in "ENCODE" mode.

ANG AND $\overline{\text{ANG}}$:
Analog signal outputs with opposite phase.

INTERGATOR:
Output connected to external intergrator to produce envelope waveform.

ENVELOPE:
Input to be connected to external intergrator output.

C1, C2
Auxilary outputs for signal modulation.

COMPDATA:
Input feedback signal from the external comparator output.

R1,C1:
Oscillator pins. Use C1 as the input when employing external clock.

CLOCK DRIVER:
Output pin for the generation of negative voltage.

V_{DD} & GND:
+3V ~ +6V power inputs.

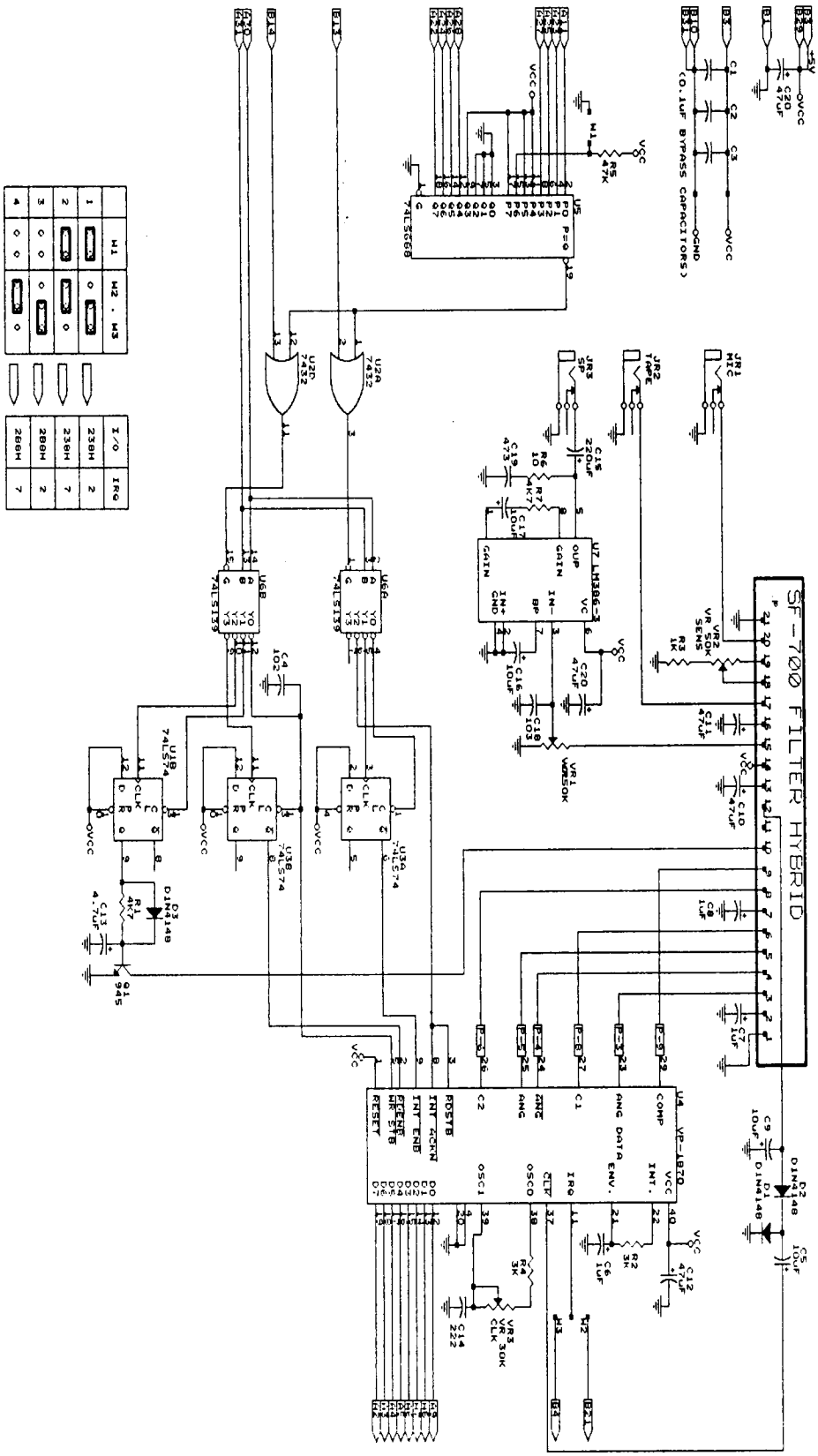


FIGURE 1: PC VOICE I/O DEVICE USING VP-1870&SF-700

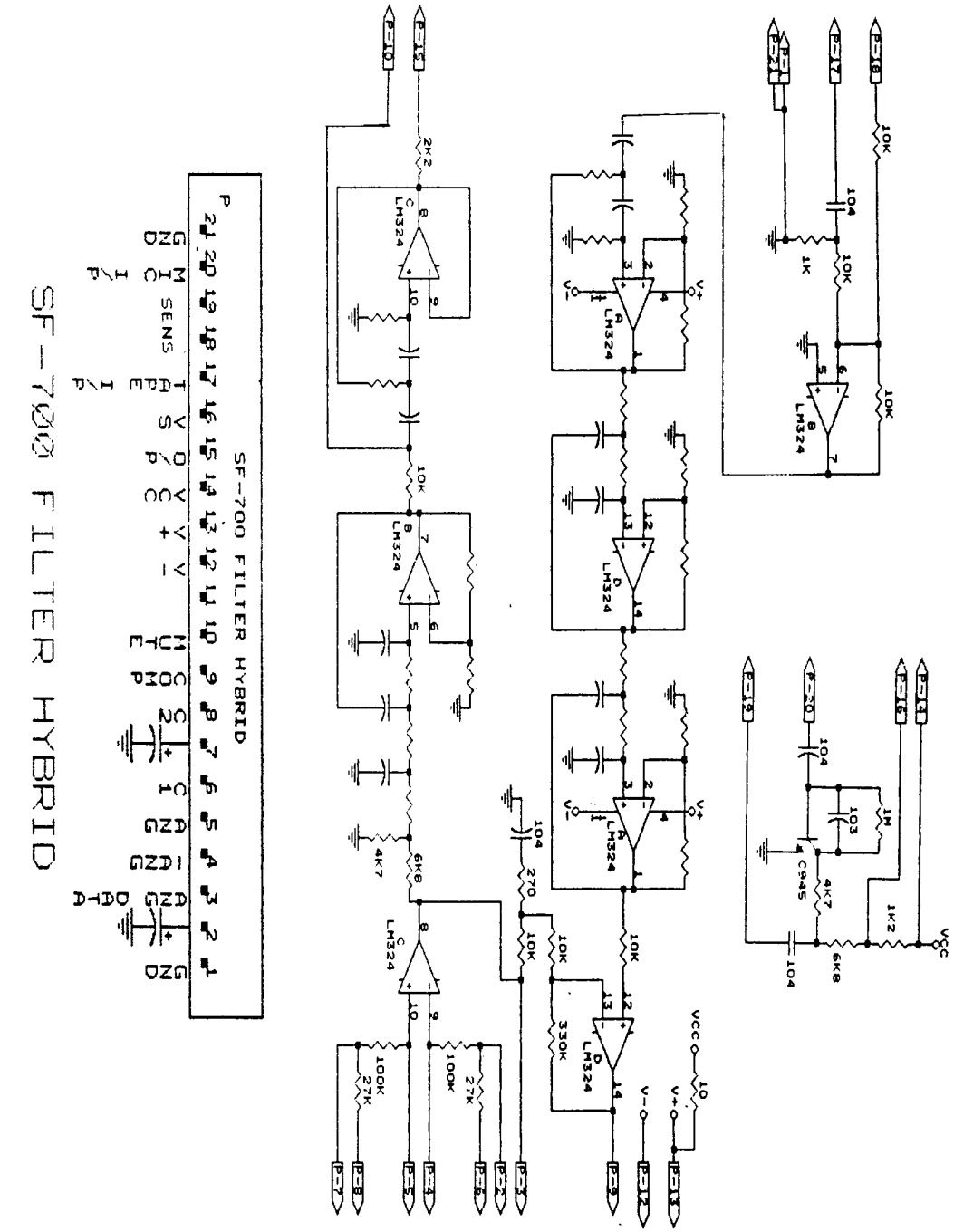
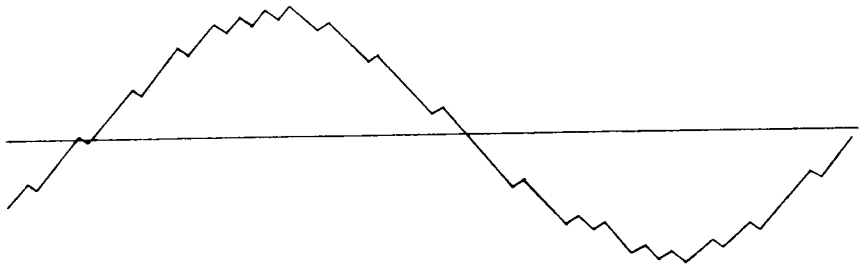


FIGURE 2 : CIRCUIT DIAGRAM OF SF-700 FILTER HYBRID

FIGURE 3 : QUANTIZIED SINEWAVE SIGNAL AT DEMODULATOR OUTPUT (1kHZ)



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