CY7B194
CY7B195
CY7B196

64K x 4 Static R/W RAM

Features

- **High speed**
  — t_{AA} = 10 ns
- **BiCMOS for optimum speed/power**
- **Low active power**
  — 850 mW
- **Low standby power**
  — 160 mW
- **Automatic power-down when deselected**
- **Output enable ($\overline{OE}$) feature (CY7B195 and CY7B196 only)**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7B194, CY7B195, and CY7B196 are high-performance BiCMOS static RAMs organized as 65,536 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active LOW chip enable ($\overline{CE}_2$, CY7B196 only), an active LOW output enable ($\overline{OE}$, CY7B195 and CY7B196 only), and three-state drivers. Both devices have an automatic power-down feature that reduces power consumption by more than 75% when deselected.

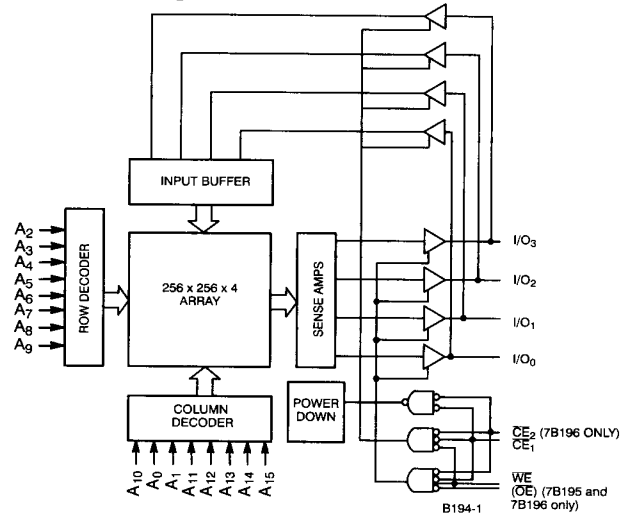
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two ($\overline{CE}_2$, CY7B196 only) input LOW. Data on the I/O pin (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$), chip enable two ($\overline{CE}_2$, CY7B196 only), and output enable ($\overline{OE}$) LOW, while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

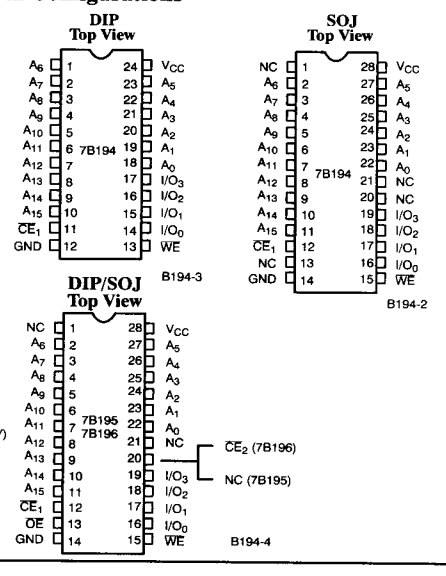
The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH, or $\overline{CE}_2$ HIGH, CY7B196 only), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$, $\overline{CE}_2$ CY7B196 only, and $\overline{WE}$ LOW).

The CY7B194, CY7B195, and CY7B196 are available in 300-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configurations



Selection Guide

		7B194–10 7B195–10 7B196–10	7B194–12 7B195–12 7B196–12	7B194–15 7B195–15 7B196–15	7B194–20 7B195–20 7B196–20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	170	160	150	
	Military		170	160	160
Maximum Standby Current (mA)	Commercial	40	35	30	
	Military		40	40	40

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... – 0.5V to +7.0V

DC Input Voltage[1] ..... – 0.5V to +7.0V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B194–10 7B195–10 7B196–10 Min.	7B194–10 7B195–10 7B196–10 Max.	7B194–12 7B195–12 7B196–12 Min.	7B194–12 7B195–12 7B196–12 Max.	7B194–15, 20 7B195–15, 20 7B196–15, 20 Min.	7B194–15, 20 7B195–15, 20 7B196–15, 20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			– 0.3	0.8	– 0.3	0.8	– 0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 10	+10	– 10	+10	– 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		– 10	+10	– 10	+10	– 10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			– 300		– 300		– 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		170		160		150	mA
			Mil				170		160	
I_{SB}	Automatic CE Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		40		35		30	mA
			Mil				40		40	

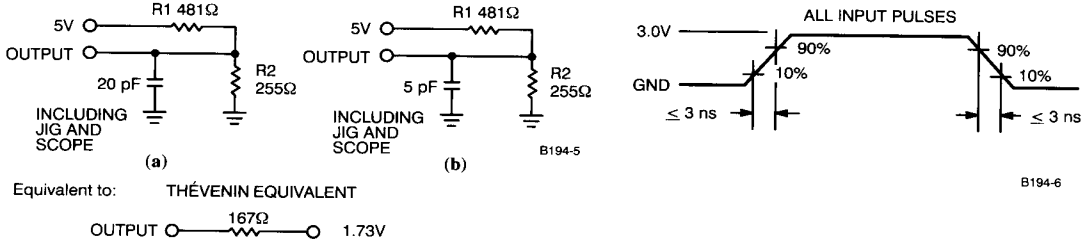
Capacitance[5]

Parameter	Description	Test Conditions	Max.[6]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}, $C_{I/O}$	Output Capacitance		8	pF

Notes:

1. $V_{IL\,(min.)}$ = – 3.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. For PDIP (P13, P21) AND CDIP (D14, D22), C_{IN} = C_{OUT} = 10 pF.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3, 7]

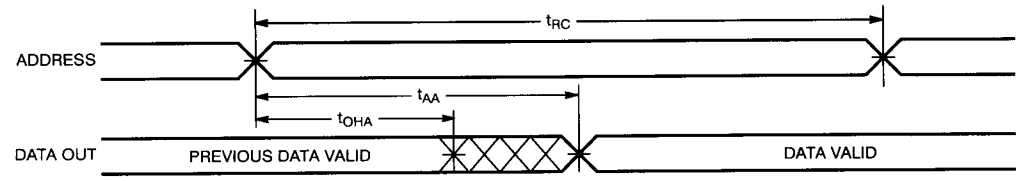
Parameter	Description	7B194–10 7B195–10 7B196–10		7B194–12 7B195–12 7B196–12		7B194–15 7B195–15 7B196–15		7B194–20 7B195–20 7B196–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		6		7		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	2		2		2		2		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]		6		7		8		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		6		7		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE[10, 11]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		15		ns
t_{AW}	Address Set-Up to Write End	8		9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		10		15		ns
t_{SD}	Data Set-Up to Write End	6		7		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	2		2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]		6		7		7		10	ns

Notes:

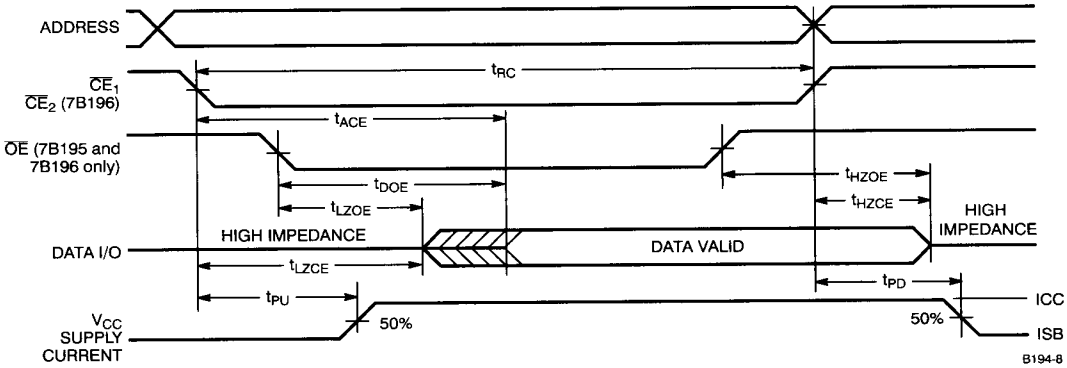
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 20-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal will terminate a write by going HIGH. The input data set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

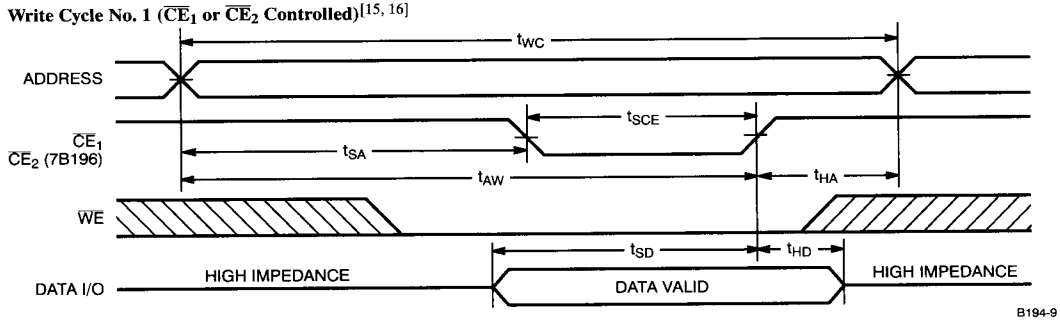
Read Cycle No. 1[12, 13]



Read Cycle No. 2[13, 14]



Write Cycle No. 1 ($\overline{CE}_1$ or $\overline{CE}_2$ Controlled)[15, 16]

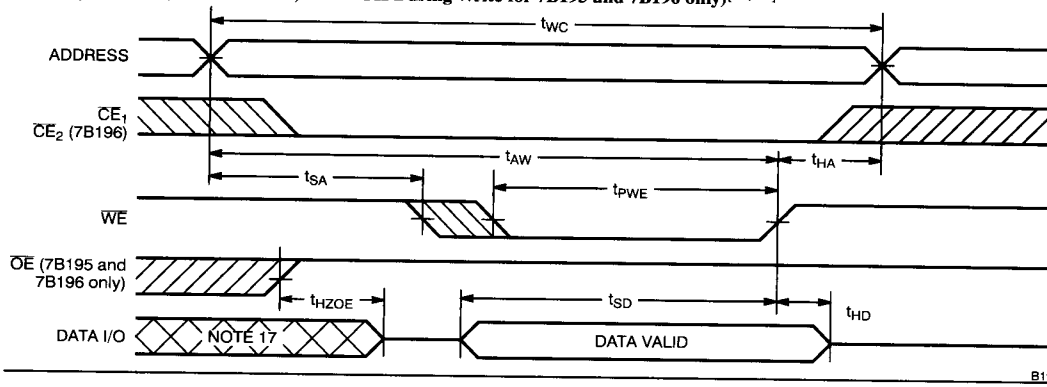


Notes:

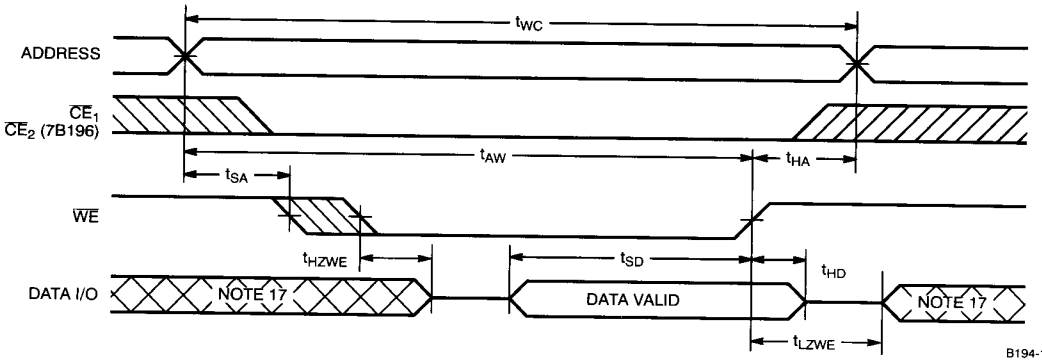
12. Device is continuously selected. $\overline{CE}_1$ ($\overline{OE}$: 7B195 and 7B196, $\overline{CE}_2$: 7B196 only) = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}_1$ and $\overline{CE}_2$ transition LOW.
15. Data I/O is HIGH impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}_1$ ($\overline{CE}_1$ or $\overline{CE}_2$ on the 7B196) goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write for 7B195 and 7B196 only)[15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]



Note:
17. During this period, the I/Os are in the output state and input signals should not be applied.

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7B194 Truth Table

$\overline{CE_1}$	$\overline{WE}$	$I/O_0 - I/O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

7B195 Truth Table

$\overline{CE_1}$	$\overline{WE}$	$\overline{OE}$	$I/O_0 - I/O_3$	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output Disabled	Active (I_{CC})

7B196 Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	Data Out	Read	Active (I_{CC})
L	L	L	X	Data In	Write	Active (I_{CC})
L	L	H	H	High Z	Selected, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B194–10PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7B194–10VC	V21	28-Lead (300-Mil) Molded SOJ	
12	CY7B194–12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7B194–12PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7B194–12VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B194–12DMB	D14	24-Lead (300-Mil) CerDIP	Military
15	CY7B194–15DC	D14	24-Lead (300-Mil) CerDIP	Commercial
	CY7B194–15PC	P13	24-Lead (300-Mil) Molded DIP	
	CY7B194–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B194–15DMB	D14	24-Lead (300-Mil) CerDIP	Military
20	CY7B194–20DMB	D14	24-Lead (300-Mil) CerDIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B196–10PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B196–10VC	V21	28-Lead (300-Mil) Molded SOJ	
12	CY7B196–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B196–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B196–12VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B196–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
15	CY7B196–15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B196–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B196–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B196–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7B196–20DMB	D22	28-Lead (300-Mil) CerDIP	Military

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Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7B195–10PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7B195–10VC	V21	28-Lead (300-Mil) Molded SOJ	
12	CY7B195–12DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B195–12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B195–12VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B195–12DMB	D22	28-Lead (300-Mil) CerDIP	Military
15	CY7B195–15DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7B195–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7B195–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7B195–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7B195–20DMB	D22	28-Lead (300-Mil) CerDIP	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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