Siliconix incorporated

VPDV SERIES DIE
P-Channel Enhancement-Mode MOS Transistors

T-37-25

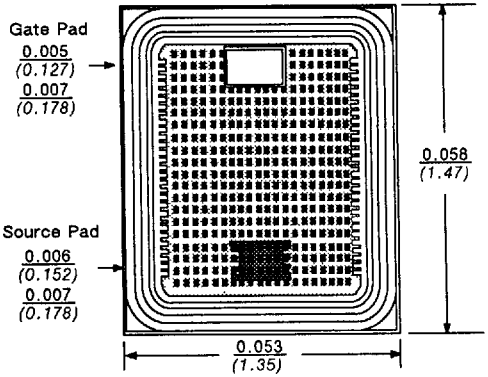
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	DEVICES	PERFORMANCE CURVES
VPDV1CHP	100	5	• VP0808B/L/M • VP1008B/L/M • VQ2004J (VPDV10 x 4) • VQ2006J (VPDV10 x 4)	VPDV10
VPDV2CHP	240	10	• TP2010L • TP2410L • VP2410L	VPDV24

DESIGNED FOR:

- Switching
- Amplification

FEATURES

- Low $r_{DS(ON)}$



Back of Chip Is Drain

Nominal Thickness
0.009 inches
0.228 mm

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		VPDV1CHP	VPDV2CHP	
Drain-Source Voltage	V_{DS}	-100	-240	V
Gate-Source Voltage	V_{GS}	±20	±30	
Operating and Storage Temperature	T_J, T_{stg}	-55 to 150		°C

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SPECIFICATIONS[a]			LIMITS			
				VPDV1CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = −10 µA, V_{GS} = 0 V	−110	−100		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −1 mA	−3.4	−2	−4.5	
Gate-Body Leakage[c]	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −100 V, V_{GS} = 0 V	−0.001			µA
		T_J = 125°C	−0.40			
On-State Drain Current	$I_{D(ON)}$	V_{DS} = −15 V, V_{GS} = −12 V	−2	−1.1		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = −10 V, I_D = −1 A	2.5		5	Ω
		T_J = 125°C	4.3			
Forward Transconductance[c]	g_{FS}	V_{DS} = −10 V, I_D = −0 5 A	325			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = −7.5 V, I_D = −0 1 A	450			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = −25 V, V_{GS} = 0 V f = 1 MHz	75			pF
Output Capacitance	C_{oss}		40			
Reverse Transfer Capacitance	C_{rss}		18			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = −25 V, R_L = 47 Ω I_D = −0.5 A, V_{GEN} = −10 V R_G = 25 Ω	11			ns
	t_r		30			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	20			
	t_f		20			

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c Pulse test; PW = ≤ 300 µS, duty cycle ≤ 3%.

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SPECIFICATIONS[a]			LIMITS			
				VPDV2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -5 µA , V_{GS} = 0 V	-255	-240		V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -2 5 mA	-2 25	-1 0	-2 4	
Gate-Body Leakage[c]	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	±1			nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -180 V, V_{GS} = 0 V	-0 001			µA
		T_J = 125°C	-0.40			
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4 5 V	-300	-150		mA
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -100 mA	7		10	Ω
		V_{GS} = -4.5 V, I_D = -100 mA	8.5		10	
		T_J = 125°C	15 5			
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -100 mA	175			mS
Common Source Output Conductance[c]	g_{OS}	V_{DS} = -10 V, I_D = -50 mA	125			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V f = 1 MHz	65			pF
Output Capacitance	C_{oss}		20			
Reverse Transfer Capacitance	C_{rss}		8			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 250 Ω I_D = -100 mA, V_{GEN} = -10 V R_G = 25 Ω	7			ns
	t_r		18			
Turn-Off Time	$t_{d(OFF)}$	(Switching time is essentially independent of operating temperature)	45			
	t_f		45			

NOTES:
a. T_A = 25°C unless otherwise noted
b For design aid only, not subject to production testing.
c Pulse test; PW = ≤ 300 µS, duty cycle ≤ 2%

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