# VQ2006 SERIES

Siliconix incorporated

T-43-25

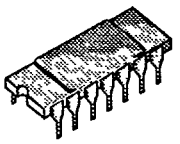
P-Channel Enhancement-Mode MOS Transistor Arrays

## PRODUCT SUMMARY

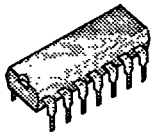
| PART NUMBER | $V_{(BR)DSS}$ (V) | $r_{DS(ON)}$ (Ω) | $I_D$ (A) | PACKAGE |
|---|---|---|---|---|
| VQ2006J | -90 | 5 | -0.41 | Plastic |
| VQ2006P | -90 | 5 | -0.41 | Side Braze |

Performance Curves: VPDV10 (See Section 7)

14-PIN DIP SIDE BRAZE

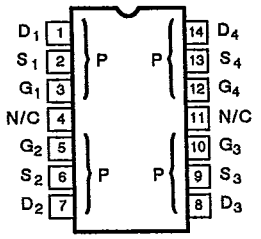


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package




## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| PARAMETERS/TEST CONDITIONS | | SYMBOL | VQ2006J | VQ2006P | UNITS |
|---|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -90 | -90 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±30 | ±20 | |
| Continuous Drain Current | $T_A$ = 25°C | $I_D$ | -0.41 | -0.41 | A |
| | $T_A$ = 100°C | | -0.23 | -0.23 | |
| Pulsed Drain Current[1] | | $I_{DM}$ | ±3 | ±3 | |
| Power Dissipation – Single | $T_A$ = 25°C | $P_D$ | 1.3 | 1.3 | W |
| | $T_A$ = 100°C | | 0.52 | 0.52 | |
| Power Dissipation – Quad | $T_A$ = 25°C | | 2 | 2 | |
| | $T_A$ = 100°C | | 0.8 | 0.8 | |
| Operating Junction and Storage Temperature | | $T_J$, $T_{stg}$ | -55 to 150 | | °C |
| Lead Temperature (1/16" from case for 10 seconds) | | $T_L$ | 300 | | |

## THERMAL RESISTANCE

| THERMAL RESISTANCE | SYMBOL | VQ2006J | VQ2006P | UNITS |
|---|---|---|---|---|
| Junction-to-Ambient – Single | $R_{thJA}$ | 96.2 | 96.2 | °C/W |
| Junction-to-Ambient – Quad | | 62.5 | 62.5 | |

[1]Pulse width limited by maximum junction temperature

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# VQ2006 SERIES

| ELECTRICAL CHARACTERISTICS [1] | | | LIMITS | | | |
|---|---|---|---|---|---|---|
| | | | | VQ2006 [4] | | |
| PARAMETER | SYMBOL | TEST CONDITIONS | TYP [2] | MIN | MAX | UNIT |
| **STATIC** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = −10 µA | −110 | −90 | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = −1 mA | −3.4 | −2 | −4.5 | V |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±30 V | ±1 | | ±100 | nA |
| | | $T_J$ = 125°C | ±5 | | ±500 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = −90 V, $V_{GS}$ = 0 V | −0.0005 | | −10 | µA |
| | | $T_J$ = 125°C | −0.1 | | −500 | µA |
| On-State Drain Current [3] | $I_{D(ON)}$ | $V_{DS}$ = −10 V, $V_{GS}$ = −10 V | −2 | −1 | | A |
| Drain-Source On-Resistance [3] | $r_{DS(ON)}$ | $V_{GS}$ = −10 V, $I_D$ = −1 A | 2.5 | | 5 | Ω |
| | | $T_J$ = 125°C | 4.3 | | 8 | Ω |
| Forward Transconductance [3] | $g_{FS}$ | $V_{DS}$ = −10 V, $I_D$ = −0.5 A | 325 | 200 | | mS |
| Common Source Output Conductance [3] | $g_{OS}$ | $V_{DS}$ = −7.5 V, $I_D$ = −0.1 A | 450 | | | µS |
| **DYNAMIC** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = −25 V, $V_{GS}$ = 0 V, f = 1 MHz | 75 | | 150 | pF |
| Output Capacitance | $C_{oss}$ | | 40 | | 60 | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | 18 | | 25 | pF |
| **SWITCHING** | | | | | | |
| Turn-On Time | $t_{d(ON)}$ | $V_{DD}$ = −25 V, $R_L$ = 47 Ω, $I_D$ = −0.5 A, $V_{GEN}$ = −10 V, $R_G$ = 25 Ω (Switching time is essentially independent of operating temperature) | 11 | | 15 | ns |
| | $t_r$ | | 30 | | 40 | ns |
| Turn-Off Time | $t_{d(OFF)}$ | | 20 | | 30 | ns |
| | $t_f$ | | 20 | | 30 | ns |

NOTES:
1. $T_A$ = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test: PW = 300 µs, duty cycle ≤ 2%.
4. Data sheet limits have been revised.

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