



CYPRESS
SEMICONDUCTOR

PRELIMINARY

CY7B339

Features

- Very high performance decoder with latched outputs
 - $t_{PD} = 7 \text{ ns}$
 - $t_{LEO} = 5.5 \text{ ns}$
 - $t_{IS} = 4 \text{ ns}$
- 12 inputs
- 8 latched outputs
- 4 product terms per output
- Asynchronous output enable
- Power-on reset
- High noise immunity
- >2001V input protection from electrostatic discharge
- Advanced BiCMOS technology

- Available in 28-pin 300-mil PDIP and CerDIP, and in SOJ, PLCC, and LCC packages

Functional Description

The CY7B339 is a 7-ns, 28-pin programmable logic device specially designed for decoding applications with high-performance general-purpose processors and fast state machines.

There are twelve inputs that feed into the 24 by 32 programmable array. Processed data from the programmable array is delivered to the eight output latches. When the latch enable input is HIGH, the output latches are transparent and data from the array is available to the output buffers. When the latch enable input goes from HIGH to LOW, the latch contents are frozen.

7-ns BiCMOS PAL® with Output Latches

There are four product terms per output and all outputs can be three-stated using the output enable signal.

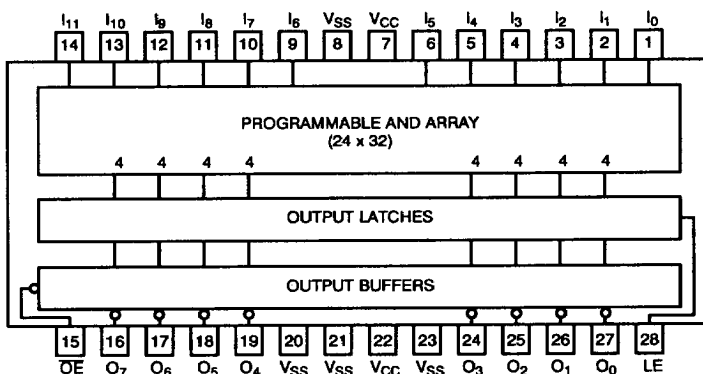
Additional features of the CY7B339 include a power-on reset circuit that initializes all output latches to a "0" upon power-up, and six centrally located power pins (two V_{CC} pins and four ground pins), which improve noise margins.

The CY7B339 is available in a wide variety of package types including 28-pin, 300-mil plastic and ceramic DIPs, SOJs, LCCs, and PLCCs.

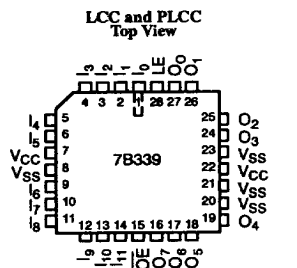
4

PLDS

Logic Block Diagram and DIP/SOJ Pinout



Pin Configuration



B339-2

B339-1

Selection Guide

Generic Part Number	t_{PD} (ns)		t_{LEO} (ns)		I_{CC} (mA)		t_{IS} (ns)	
	Com'l	Mil	Com'l	Mil	Com'l	Mil	Com'l	Mil
7B339-7	7		5.5		180		4	
7B339-8		8		6.5		180		5
7B339-9	9		7.5		180		6	
7B339-10		10		8		180		6
7B339-12		12		9.5		180		7

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to +150°C

Ambient Temperature with Power Applied - 55°C to +125°C

Supply Voltage to Ground Potential (Pins 7 and 22 to Pins 8, 20, 21, and 23) - 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State - 0.5V to +V_{CC} Max.

DC Input Voltage - 0.5V to +V_{CC} + 0.5V

Output Current into Outputs (LOW) 12 mA

DC Input Current - 30 mA to +5 mA (Except during programming)

DC Programming Voltage 9.5V

Static Discharge Voltage > 2001V (per MIL-STD-883 Method 3015)

Latch-Up Current > 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[1]	- 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7B339		Units
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA, Com'l I _{OH} = -3 mA, Mil	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} I _{OL} = 12 mA, Com'l I _{OL} = 8 mA, Mil		0.4	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.2		V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8	V
I _{Ix}	Input Leakage Current	V _{CC} = Max., 0.4V ≤ V _{IN} ≤ 2.7V	- 250	25	μA
I _{OZ}	Output Leakage Current	V _{CC} = Max., 0.4V ≤ V _{OUT} ≤ 2.7V	- 100	100	μA
I _{SC}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.5V ^[2]	- 30	- 130	mA
I _{CC}	Power Supply Current	V _{CC} = Max., Outputs Disabled (in High Z State), Device Operating at f _{MAX} Com'l Mil		180	mA

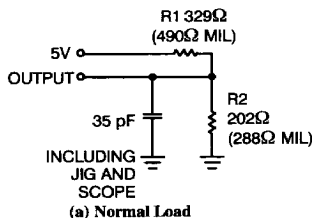
Capacitance^[3]

Parameters	Description	Typ.	Max.	Units
C _{IN}	Input Capacitance	11	10	pF
C _{OUT}	Output Capacitance	9	10	pF

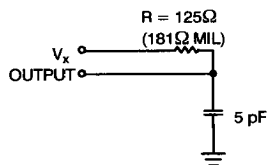
Notes:

1. T_A is the "instant on" case temperature.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. The normal test load is used for all parameters except for t_{pxz} and t_{pzx}, which are tested using the three-state load.

AC Test Loads and Waveforms^[4]

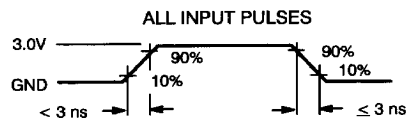


B339-3



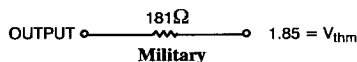
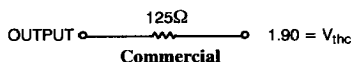
(b) Three-State Load

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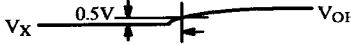
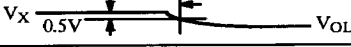


B339-4

Equivalent to: THEVENIN EQUIVALENTS



AC Test Loads and Waveforms (continued)

Parameter	V _X	Output Waveform—Measurement Level
t _{PXZ} (–)	1.5V	
t _{PXZ} (+)	2.6V	
t _{PZX} (+)	V _{thc}	
t _{PZX} (–)	V _{thc}	

Switching Characteristics Over the Operating Range^[5]

Parameters	Description	Commercial				Military						Units
		7		9		8		10		12		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Input to Output Propagation Delay		7		9		8		10		12	ns
t _P	Clock Period (t _{WH} +t _{WL})[3]	6.4		8.8		7.6		10.4		12.4		ns
f _{MAXD}	Maximum Frequency Data Path (Lower of 1/t _p and 1/t _{PD})[3,6]		142		111		125		96		80	MHz
t _{WH}	Latch Enable HIGH[3]	3.2		4.4		3.8		5.2		6.2		ns
t _{WL}	Latch Enable LOW[3]	3.2		4.4		3.8		5.2		6.2		ns
t _{LEO}	Latch Enable to Output Delay		5.5		7.5		6.5		8		9.5	ns
t _{LOH}	Output Hold After Latch Enable	0		0		0		0		0		ns
t _{IS}	Input Set-Up Time	4		6		5		6		7		ns
t _{IH}	Input Hold Time	0.5		0.5		0.5		0.5		0.5		ns
t _{PXZ}	Pin 15 to Output Disable Delay[7]		7		10		8.5		11.5		14.5	ns
t _{PZX}	Pin 15 to Output Enable Delay		7		10		8.5		11.5		14.5	ns
t _{PR}	Power-Up Reset Time[8]		1		1		1		1		1	μs

Notes:

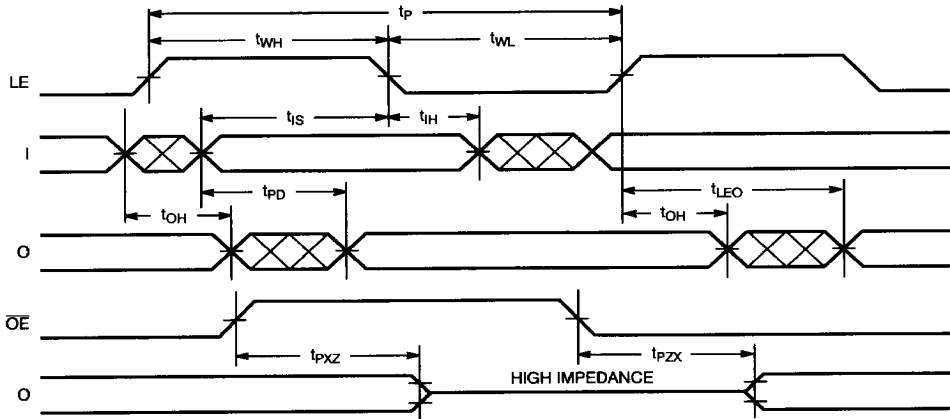
5. AC test load is used for all parameters except where noted.

6. Maximum frequency data path (f_{MAXD}) is limited by 1/t_{PD} for the 7- and 9-ns commercial and the 8-ns military versions. Maximum frequency data path (f_{MAXD}) is limited by 1/t_P for the 10- and 12-ns military versions.

7. This parameter is measured as the time that the previous output data state remains stable after the output disable signal is received. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} Min. or a previous LOW level has risen to 0.5 volts above V_{OL} Max.

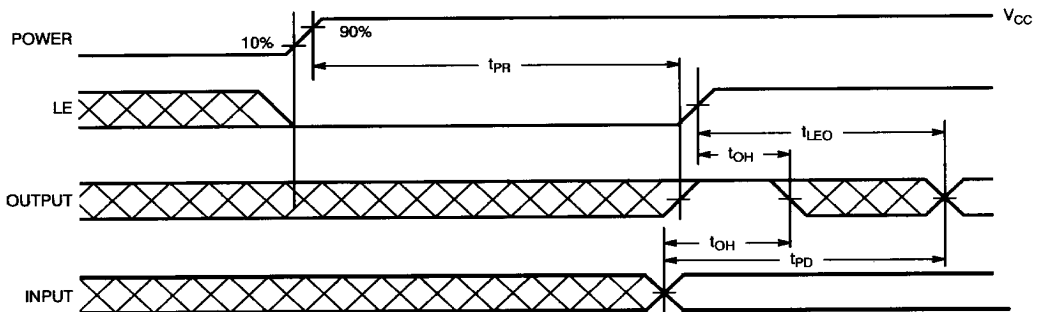
8. This part has been designed with the capability to reset during system power-up. Following power-up, the output latches will be reset to a logic LOW state. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied. The latch enable input must be in a valid LOW state (V_{IN} less than 0.8V) prior to occurrence of the 10% level on the monotonically rising power supply voltage. In addition, the latch enable signal must remain stable in that valid LOW state, as indicated, until the 90% level on the power supply voltage has been reached. The latch enable is allowed to change from its LOW state only after the indicated delay (t_{PR}) has been observed.

Switching Waveform



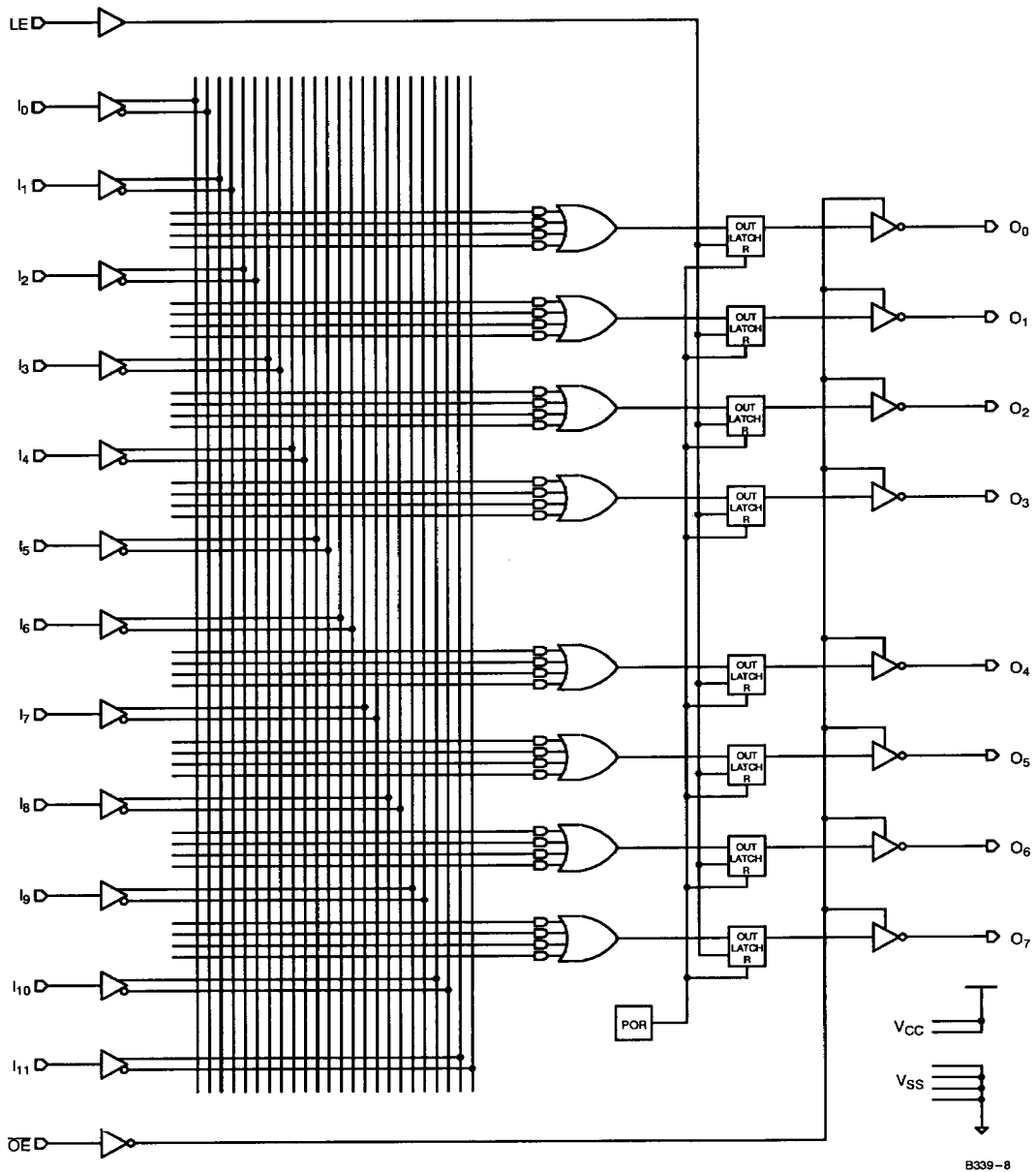
B339-7

Power-Up Reset Waveform^[7]



B339-6

CY7B339 Logic Diagram



Ordering Information

t_{PD} (ns)	t_{LEO} (ns)	Ordering Code	Package Type	Operating Range
7	5.5	CY7B339-7PC	P21	Commercial
		CY7B339-7DC	D22	
		CY7B339-7JC	J64	
		CY7B339-7VC	V21	
8	6.5	CY7B339-8DMB	D22	Military
		CY7B339-8LMB	L64	
9	7.5	CY7B339-9PC	P21	Commercial
		CY7B339-9DC	D22	
		CY7B339-9JC	J64	
		CY7B339-9VC	V21	
10	8	CY7B339-10DMB	D22	Military
		CY7B339-10LMB	L64	
12	9.5	CY7B339-12DMB	D22	Military
		CY7B339-12LMB	L64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{LEO}	7, 8, 9, 10, 11
t_{PXZ}	7, 8, 9, 10, 11
t_{PZX}	7, 8, 9, 10, 11

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