FEATURES

- 256 words by 4-bit static RAM for cache and control store applications
- Very fast: Choice of 4, 5, and 6 ns maximum address access times
- TTL compatible inputs and outputs
- Single +5.0 Volt power supply
- Very low sensitivity to radiation
- Standard 22-pin DIP
- Fully static operation - equal access and cycle times
- Pin compatible with standard silicon -422 and -122 products

FUNCTIONAL DESCRIPTION

The Vitesse VS12G422T is a very high speed, fully decoded 1024-bit read write static random access memory organized as 256 words by 4 bits. All inputs and outputs of this RAM are TTL compatible and operation is from a standard +5.0 Volt power supply.

Fully static asynchronous internal circuits are used, which require no clocks or refreshing for operation. Memory expansion is provided by an active LOW chip select input ($\overline{CS}_1$), an active HIGH chip select input (CS_2) and three-state outputs. Due to its static operation, the VS12G422T offers equal read and write cycle times, which further simplifies system design.

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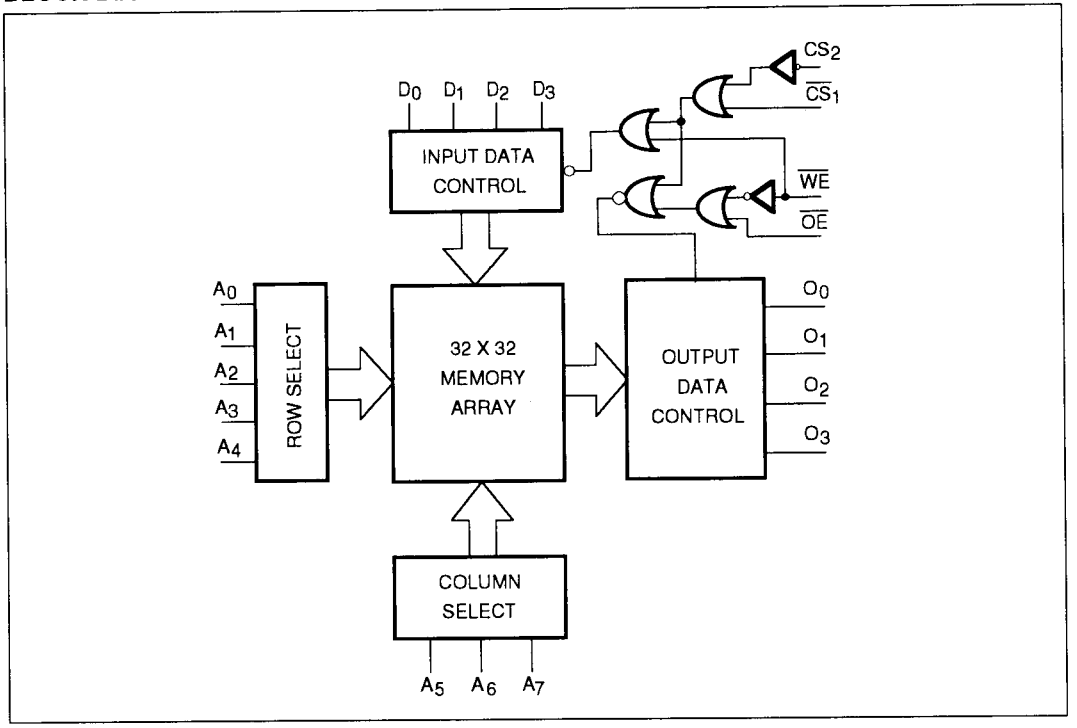
BLOCK DIAGRAM



TRUTH TABLE

Inputs				Output	Mode
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$		
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level (2.4 V) *X = Don't Care (HIGH or LOW)*
L = LOW Voltage Level (0.4 V) *HIGH Z = High-Impedence*

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage *(V_{CC})* ..... -0.5 V to +6.0 V
Input Voltage Applied, *(V_{IN})* ..... -1.0 V to +7.0 V
Input Current, *(I_{IN})*, (DC, output LOW) ..... -30 to +30 mA
Output Current, *(I_{OUT})*, (DC, output LOW) ..... 20 mA
Case Temperature Under Bias, *(T_C)* ..... -55° to +125°C
Storage Temperature(2), *(T_{STG})* ..... -65° to +150°C

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage, *(V_{CC})* ..... 4.75 to 5.25 V
Operating Temperature Range (2). ..... 0° to +70°C

NOTES: *(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
(2) Lower limit is ambient temperature and upper limit is case temperature.

DC CHARACTERISTICS *(Over recommended operating conditions)*

Parameters	Description	Commercial Range				Test Conditions
		5,6 ns		4 ns		
		Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	2.4 V	—	2.4 V	—	V_{CC} = MIN, I_{OH} = -5.2 mA
V_{OL}	Output LOW voltage	—	0.5 V	—	0.5 V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{IH}	Input HIGH voltage	2.0 V	—	2.0 V	—	—
V_{IL}	Input LOW voltage	—	0.8 V	—	0.8 V	—
I_{IX}	Input LOAD current	-100 µA	100 µA	-100 µA	100 µA	V_{IN} = 3.3 V
I_{OZ}	Output current (HIGH-Z)	-1.0 mA	1.0 mA	-1.0 mA	1.0 mA	$V_{OL} \leq V_{OUT} \leq V_{OH}$ *Output Disabled*
I_{CC}	Power supply current (from V_{CC})	—	300 mA	—	300 mA	V_{CC} = MAX, I_{OUT} = 0 mA

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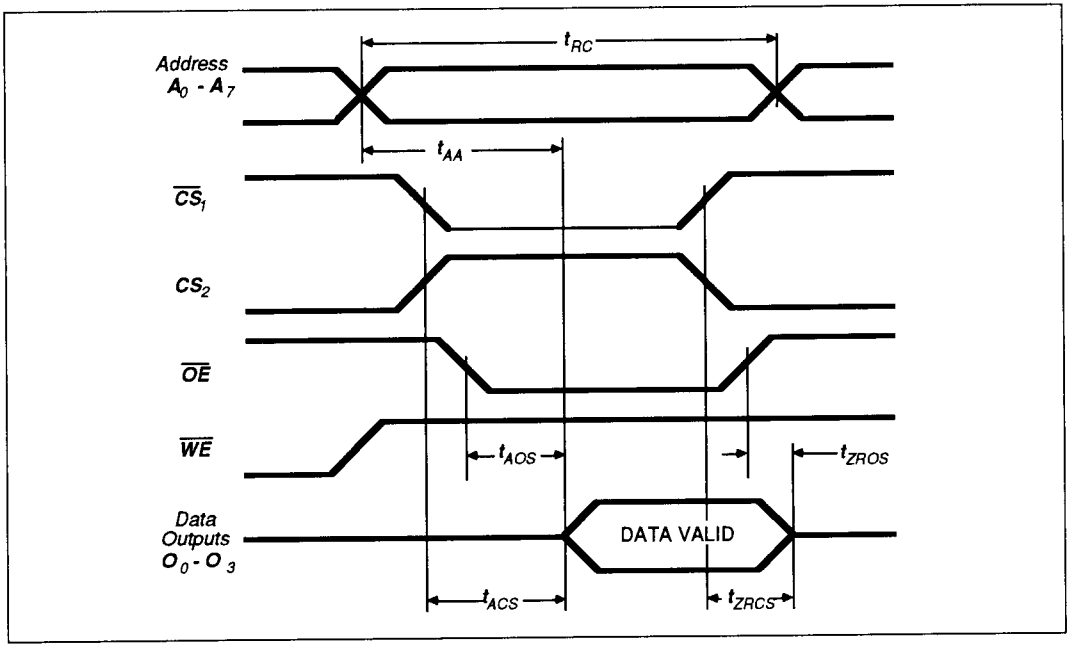
AC PERFORMANCE CHARACTERISTICS [1]

(Over guaranteed operating conditions, GND = 0 V)

Read Mode



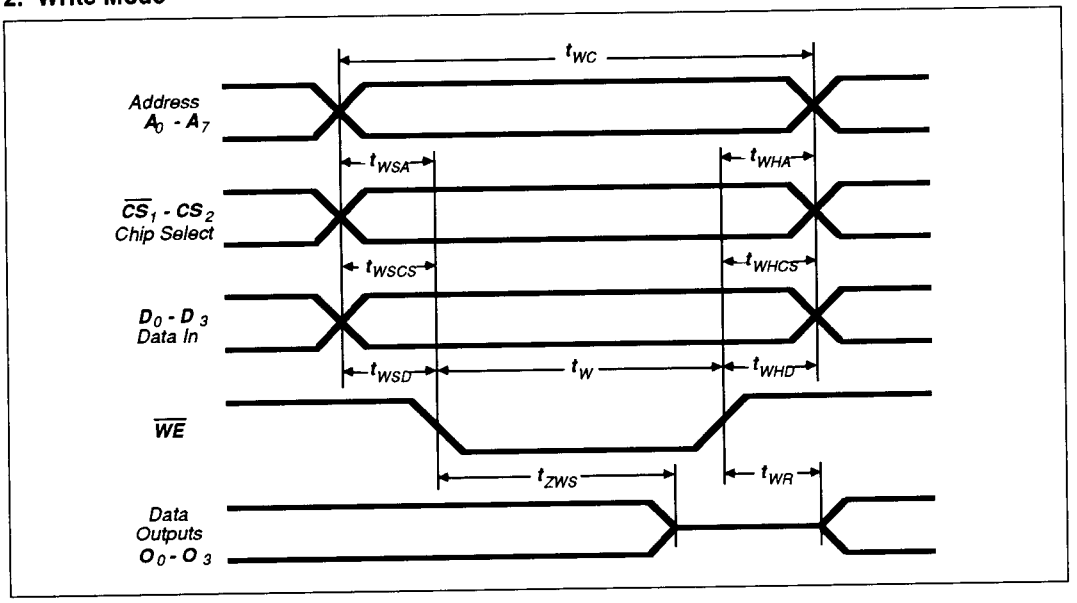
Parameters	Description	6 ns		5 ns		4 ns		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	6	—	5	—	4	—	ns
t_{ACS}	Chip select time	—	4	—	3.5	—	2.5	ns
t_{ZRCS} [2]	Chip select to HIGH Z	—	5	—	4	—	3.5	ns
t_{AOS}	Output enable time	—	4	—	3.5	—	2.5	ns
t_{ZROS} [2]	Output enable to HIGH Z	—	5	—	4	—	3.5	ns
t_{AA}	Address access time	—	6	—	5	—	4	ns

NOTES: 1) Test conditions assume signal transition times of 3 ns or less. Timing reference levels of 1.5 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in Figure 1 on ***page X.***
2) Transition is measured at steady state HIGH level -250 mV or steady state LOW level +250 mV on the output from 1.5 V level on the input with load shown in Figure 1 on ***page X.***

AC PERFORMANCE CHARACTERISTICS (con't) (1)

(Over guaranteed operating conditions, GND = 0V)

2. Write Mode



Paramters	Description	6 ns		5 ns		4ns		
		Min	Max	Min	Max	Min	Max	Units
t_{WC}	Write cycle time	6	—	5	—	4	—	ns
t_{ZWS} (2)	Write disable to HIGH Z	—	5	—	4	—	3.5	ns
t_{WR}	Write recovery time	—	4.5	—	3.5	—	3	ns
t_W (3)	Write pulse width	4	—	3	—	2.5	—	ns
t_{WSD}	Data setup time prior to write	0	—	0	—	0	—	ns
t_{WHD}	Data hold time after write	2	—	2	—	1.5	—	ns
t_{WSA} (3)	Address setup time	0	—	0	—	0	—	ns
t_{WHA}	Address hold time	2	—	2	—	1.5	—	ns
t_{WSCS}	Chip select setup time	0	—	0	—	0	—	ns
t_{WHCS}	Chip select hold time	2	—	2	—	1.5	—	ns

NOTES: 1) Test conditions assume signal transition times of 3 ns or less. Timing reference levels of 1.5 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in Figure 1 on ***page X***
2) Transition is measured at steady state HIGH level -250 mV or steady state LOW level +250 mV on the output from 1.5 V level on the input with load shown in Figure 1 on ***page X***
3) t_W measured at t_{WSA} = min; t_{WSA} measured at t_W = min

FIGURE 1: AC TEST LOADING CONDITION

The following conditions apply to the "AC Performance Characteristics" indicated on **pages X and X.**

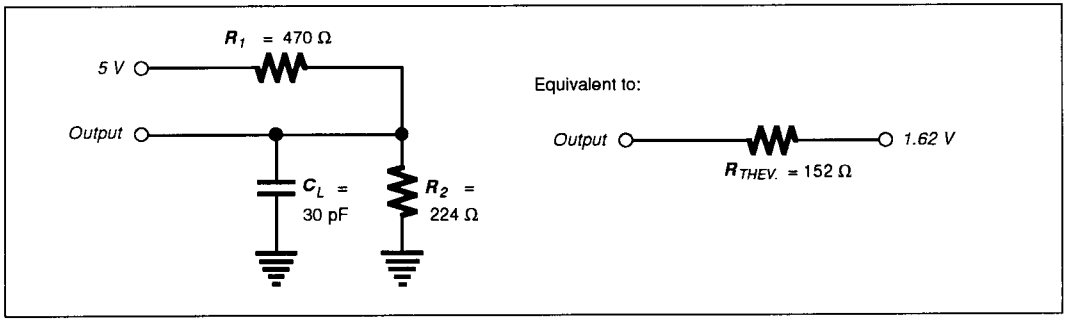
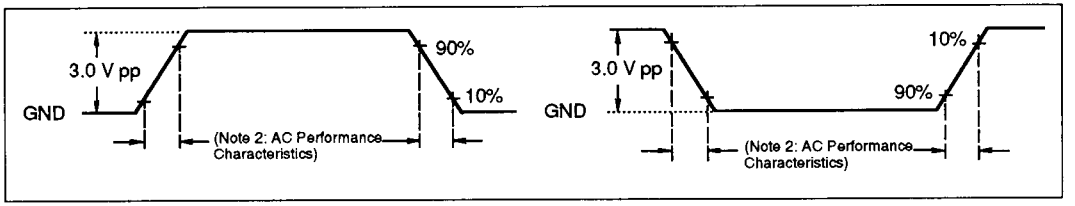


FIGURE 2: AC TEST INPUT LEVELS

The following conditions apply to the "AC Performance Characteristics" indicated on **pages X and X.**

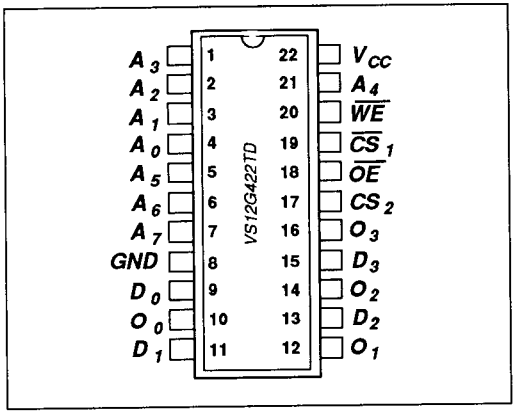


ADDRESS DESIGNATORS

Address Name	*Address Function*	*Pin # (22-pin DIP)*
A_0	AX_0	4
A_1	AX_1	3
A_2	AX_2	2
A_3	AX_3	1
A_4	AX_4	21
A_5	AY_5	5
A_6	AY_6	6
A_7	AY_7	7

CONNECTION DIAGRAM

(22-pin DIP - Top View)



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PIN DESCRIPTION

Pin #	Name	I/O	Description
1-7, 21	A_0 - A_7	I	Address inputs
9, 11, 13, 15	D_0 - D_3	I	Data Inputs
19	$\overline{CS}_1$	I	Chip select input (Active LOW)
10, 12, 14, 16	O_0 - O_3	O	Data outputs
17	CS_2	I	Chip select input (Active HIGH)
20	$\overline{WE}$	I	Write enable input (Active LOW)
18	$\overline{OE}$	I	Output enable input (Active LOW)
22	V_{CC}		5.0 V supply connection
8	GND		Ground connection (0 V)