# VITESSE

# VS8001/VS8002

## 12:1 Multiplexer – 1:12 Demultiplexer Chip Set

T-51-12

### FEATURES

- Serial data: up to 1.25 Gb/s
- ECL 100K/10KH compatible parallel data inputs/outputs
- Set input on VS8001 synchronizes external and internal clocks
- Skip input on VS8002 for alignment of 12-bit output to word boundaries
- Standard ECL power supplies: $V_{EE}$ = -5.2 V ± 0.26 V, $V_{TT}$ = -2.0 V ± 0.1 V
- Available in commercial or industrial temperature ranges

### FUNCTIONAL DESCRIPTION

#### Introduction

The VS8001 and VS8002 are data conversion devices capable of serial data rates up to 1.25 Gb/s, transforming 12-bit wide parallel data to serial data and serial data to 12-bit wide parallel data. Evaluation of the parts is facilitated by on-chip self-test circuitry.

The VS8001 and VS8002 are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 52-pin leadless or leaded chip carrier. Refer to Section 6, "Packaging" for a complete description of these packages.

#### VS8001

The VS8001 is a 12-bit parallel to serial data converter. A fully synchronous internal design receives 12 parallel single-ended ECL bit streams ***($D_0$ - $D_{11}$)*** and converts these to a single differential bit stream ***(MUXDATA, NMUXDATA)*** up to 1.25 Gb/s. To accommodate various system timing constraints, both the high frequency clock ***(CLK, NCLK)*** and low frequency divide by 12 clock ***(CLOCK12)*** are driven off chip. A synchronizing input ***(SET)*** allows alignment of the internal low frequency clock to an externally supplied clock ***(DCLOCK)***.

#### VS8002

The VS8002 is a serial to 12-bit parallel data converter. A fully synchronous internal design receives a single bit stream ***(MUXDATA, NMUXDATA)*** operating at data rates up to 1.25 Gb/s and converts it to 12 parallel single-ended ECL bit streams ***($D_0$ - $D_{11}$)***. The high frequency clock ***(CLK, NCLK)*** is externally supplied. The low frequency divide by 12 clock ***(DCLOCK)*** is driven off chip synchronous with the parallel data. An external signal ***(SKIP)*** may be used to slip the low frequency clock by one serial data bit for alignment of the 12-bit output to word boundaries. A ***SKIP*** input causes output to be invalid for up to 3 ***DCLOCK*** cycles.

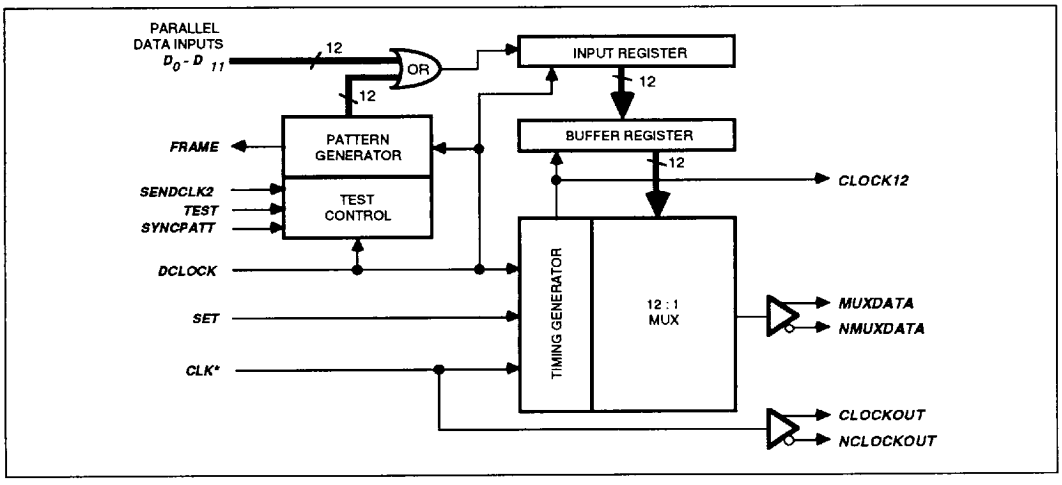
#### Self-Test Feature

In addition to normal parallel to serial and serial to parallel data conversion hardware, the VS8001 and VS8002 contain features which allow the user to fully evaluate the at-speed functionality of the devices. Given some simple enabling signals ***(TEST, SYNCPATT)***, built in hardware causes the VS8001 to transmit multiplexed internally generated data patterns via its high speed serial port to the high speed serial input on the VS8002. These signals allow the VS8002 to align itself to word boundaries and compare incoming data to its own internally generated, pseudo-random test patterns. Test enabling pins on the VS8002 consist of the ***TEST*** and ***SYNCPATT***. Test is confirmed on the ***ALIGNED, ERROR, FRAME*** and ***MATCH*** pins on the VS8002.

## APPLICATIONS

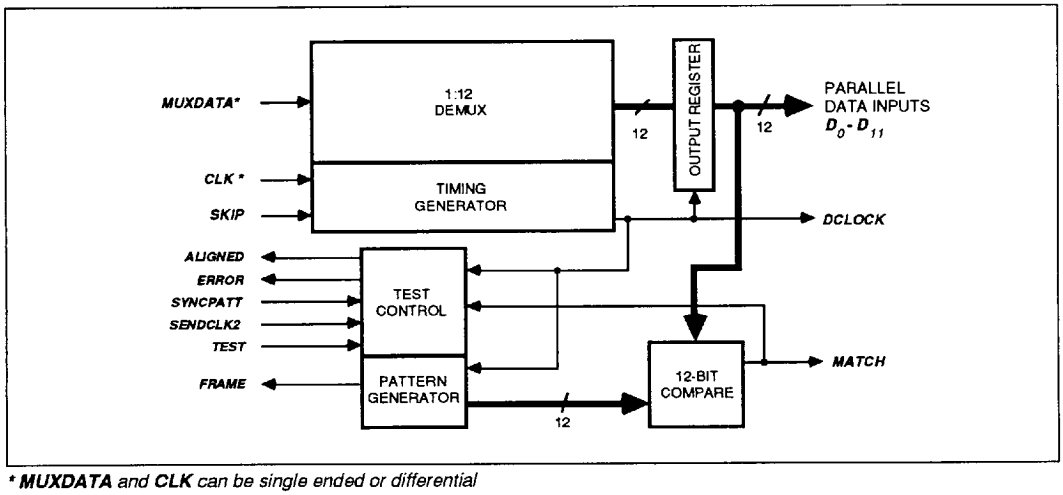
- High speed instrumentation and test equipment
- Fiber optic communication
- Local area networks
- Serialization of computer backplanes
- Computer to computer interfaces
- Serial control buses for aerospace environments

## VS8001 12:1 MULTIPLEXER BLOCK DIAGRAM




** **CLK** can be single ended or differential*

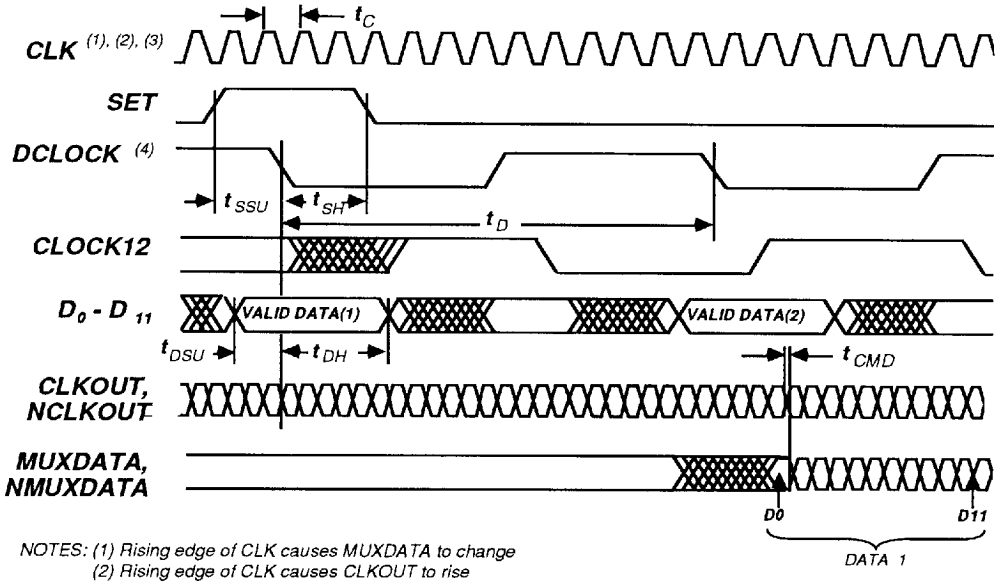
## VS8002 1:12 DEMULTIPLEXER BLOCK DIAGRAM




** **MUXDATA** and **CLK** can be single ended or differential*

## VS8001 12:1 MULTIPLEXER WAVEFORMS

T-51-12



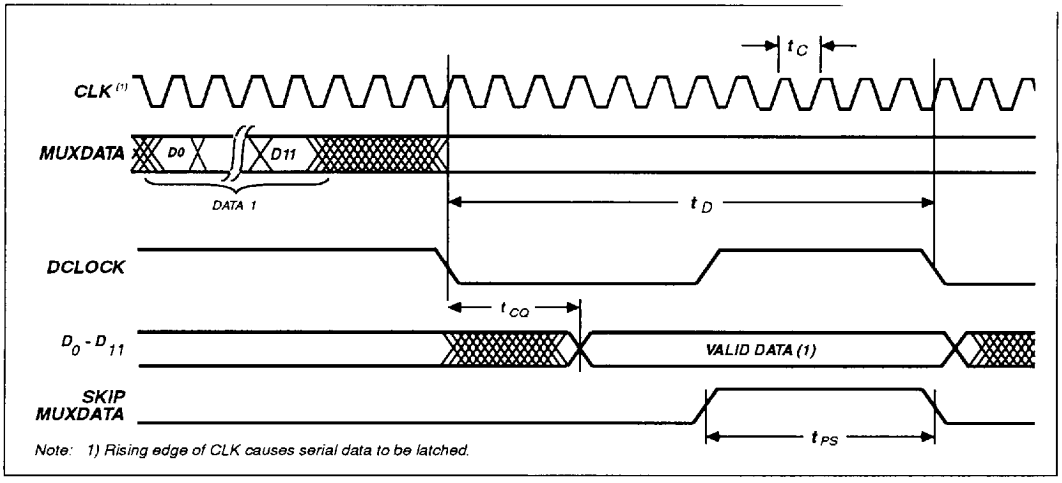

NOTES: (1) Rising edge of CLK causes MUXDATA to change
(2) Rising edge of CLK causes CLKOUT to rise
(3) Falling edge of CLK causes CLOCK12 to change
(4) Falling edge of DCLOCK latches parallel data

## VS8001 AC CHARACTERISTICS *(Over recommended operating conditions.)*

| Parameter | Description | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|
| $t_C$ | CLK period | 0.80 | — | — | ns |
| $t_D$ | DCLOCK period | 9.6 | — | — | ns |
| $t_{SSU}$ | Set set-up time | 2.0 | — | — | ns |
| $t_H$ | Set hold time | 3.0 | — | — | ns |
| $t_{DSU}$ | Data set-up time | 2.0 | — | — | ns |
| $t_{DH}$ | Data hold time | 3.0 | — | — | ns |
| $t_{CMD}$ | Clock output (CLKOUT, NCLKOUT) to muxed data output (MUXDATA, NMUXDATA) timing | -50 | — | +150 | ps |
| *jitter* | CLK to MUXDATA, NMUXDATA (max-min), (HIGH to LOW) same part, same pin as constant conditions | — | <50 | — | ps |

## VS8002 1:12 DEMULTIPLEXER WAVEFORMS

T-51-12




Note: 1) Rising edge of CLK causes serial data to be latched.

## VS8002 AC CHARACTERISTICS: *(Over recommended operating conditions.)*

| Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_C$ | CLK period | 0.80 | — | — | ns |
| $t_D$ | DCLOCK period | 9.6 | — | — | ns |
| $t_{CQ}$ | Clock to Q data | 0.5 | — | 2.5 | ns |
| $t_{PS}$ | Minimum pulse skip | 3.0 | — | — | ns |
| *Phase Margin* | MUXDATA phase timing margin with respect to CLK input: $Phase\ Margin = \left( \frac{t_{SU} + t_H}{t_C} \right) 360^\circ$ | 135 | — | — | degrees |

## ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Voltage ($V_{TT}$) ..... -3.0 V to +0.5 V
Power Supply Voltage ($V_{EE}$) ..... $V_{TT}$ + 0.7 V to -6.0 V
ECL Input Voltage Applied (2), ($V_{ECLIN}$) ..... -2.5 V to +0.5 V
High Speed Input Voltage Applied (2), ($V_{HSIN}$) ..... $V_{EE}$ - 0.7 V to $V_{CC}$ + 0.7 V
Output Current, $I_{OUT}$, (DC, output HIGH) ..... -50 mA
Case Temperature Under Bias, ($T_C$) ..... -55° to +125°C
Storage Temperature (3), ($T_{STG}$) ..... -65° to +150°C

## RECOMMENDED OPERATING CONDITIONS

ECL Power Supply Voltage, ($V_{TT}$) ..... -2.0 V ± 0.1 V
Power Supply Voltage, ($V_{EE}$) ..... -5.2 V ± 0.26 V
Operating Temperature Range (3), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C

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*NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
*(2) $V_{TT}$ must be applied before any input signal voltage ($V_{ECLIN}$ and $V_{HSIN}$) must be greater than $V_{TT}$ - 0.5 V.*
*(3) Lower limit of specification is ambient temperature and upper limit is case temperature.*

## DC CHARACTERISTICS

### ECL Inputs/Outputs

*(Over recommended operating conditions with internal $V_{REF}$. $V_{CC} = V_{CCA}$ = GND, Output load = 50 Ω to -2.0 V.)*

| Parameters | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage | -925 | — | -700 | mV | $V_{IN} = V_{IH}$ (max) or $V_{IL}$ (min) |
| $V_{OL}$ | Output LOW voltage | $V_{TT}$ | — | -1750 | mV | |
| $V_{IH}$ | Input HIGH voltage | -1040 | — | -600 | mV | Guaranteed HIGH signal for all inputs |
| $V_{IL}$ | Input LOW voltage | $V_{TT}$ | — | -1600 | mV | Guaranteed LOW signal for all inputs |
| $I_{IH}$ | Input HIGH current | — | 10 | 200 | µA | $V_{IN} = V_{IH}$ max |
| $I_{IL}$ | Input LOW current | -50 | — | — | µA | $V_{IN} = V_{IL}$ min |
| $V_{REF}$ | ECL input reference, $V_{BB}$ (2) | — | -1.29 | — | V | — |

*NOTE: 1) Differential ECL output pins must be terminated identically.*
*2) $V_{REF}$ input is used to supply external $V_{BB}$ on chip for ECL 10K ECL compatibility.*

## HIGH SPEED INPUTS/OUTPUTS

*($V_{EE}$ = -5.2V, $V_{CC}$ = GND, $V_{TT}$ = -2.0V, $T_C$ = 25°C. Input reference level ($V_{REF}$) = -3.5 V Typ.)*
*Complementary high speed output pins must be terminated equally.*

| Parameters | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH voltage | — | -0.9 | — | V | Output load: 50 Ω to -2.0 V |
| $V_{OL}$ | Output LOW voltage | — | -1.8 | — | V | |
| $\Delta V_{OUT}$ | Output voltage swing | 0.62 | 0.9 | 1.3 | V | |
| $V_{IH}$ | Input HIGH voltage | -3.1 | -3.0 | -2.9 | V | Guaranteed HIGH signal for all inputs |
| $V_{IL}$ | Input LOW voltage | -4.1 | -4.0 | -3.9 | V | Guaranteed LOW signal for all inputs |

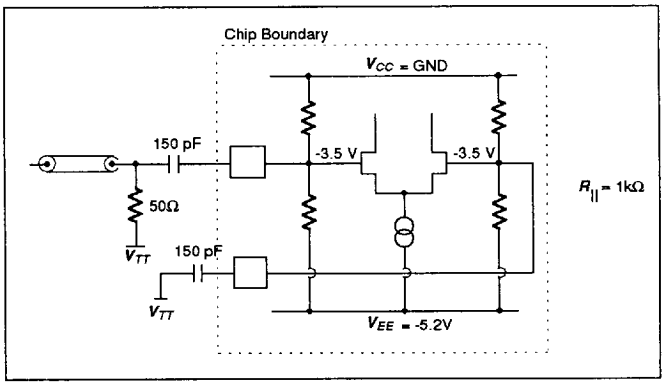
*NOTES: 1) A reference generator is built into each high speed input, and these inputs are designed to be AC coupled.*
*2) If a high speed input is used single-ended, a 150 pF capacitor must be connected between the unused high speed or complement input and $V_{EE}$.*
*3) Differential high speed output pins must be terminated identically.*
*4) ESD protection is not provided for the high speed input pins, therefore, proper procedures should be used when handling this product.*

## POWER DISSIPATION *(Over recommended operating conditions, $V_{CC}$ = GND, outputs open circuit)*

| Parameter | Description | VS8001 | | | VS8002 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power supply current from $V_{EE}$ | — | 415 | 520 | — | 435 | 550 | mA |
| $I_{TT}$ | Power supply current from $V_{TT}$ | — | 200 | 300 | — | 270 | 400 | mA |
| $P_D$ | Power dissipation | — | 2.6 | 3.5 | — | 2.8 | 3.9 | W |

## HIGH SPEED INPUTS

High speed inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approxiamtely -3.5 Volts on both the true and complementary inputs. Single-ended, AC coupled operation is illustrated at right.



## VS8001 PIN DIAGRAM

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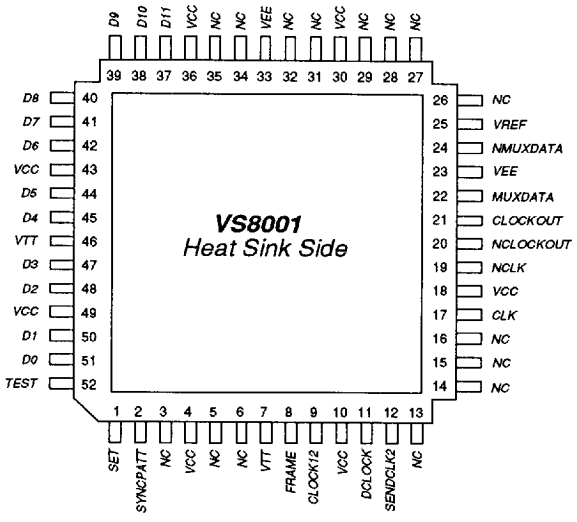
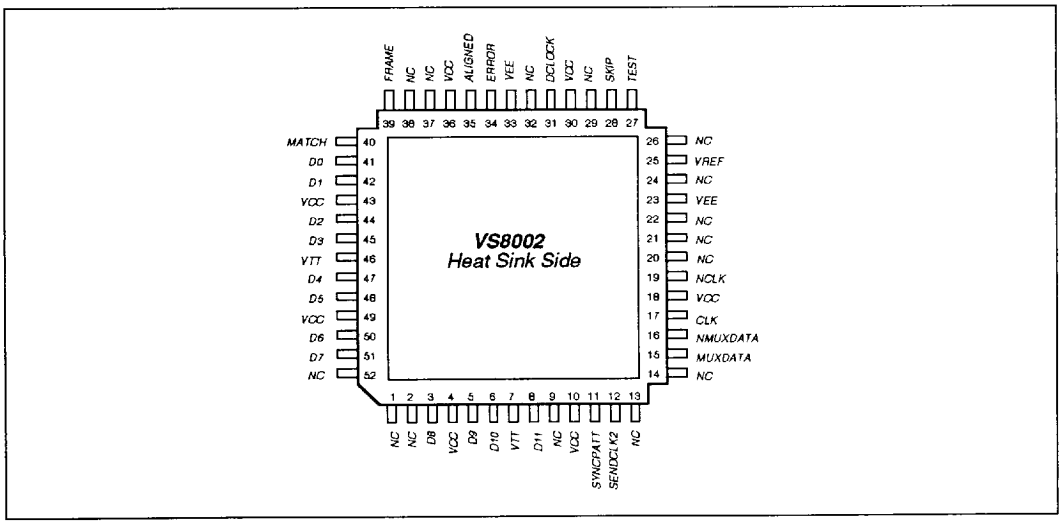



## VS8001 PIN DESCRIPTION

| Pin # | Name | I/O | Description |
|---|---|---|---|
| 17, 19 | ***CLK, NCLK*** | I | High speed clock input (capacitively coupled) |
| 21, 20 | ***CLOCKOUT, NCLOCKOUT*** | O | High speed clock output |
| 22, 24 | ***MUXDATA, NMUXDATA*** | O | High speed serial data output |
| 37-42, 44, 45, 47, 48, 50, 51 | ***DO-D11*** | I | Parallel data inputs (ECL) |
| 9 | ***CLOCK12*** | O | Internally generated divide by 12 clock output (ECL) |
| 11 | ***DCLOCK*** | I | External divide by 12 clock input (ECL) |
| 1 | ***SET*** | I | Synchronization input (ECL) |
| 52 | ***TEST*** | I | Test hardware enable (ECL input). LOW for normal operation. |
| 8 | ***FRAME*** | O | Test pattern repeat confirmation (ECL output). Float or VCC for normal operation. |
| 2 | ***SYNCPATT*** | I | Test pattern alignment enable (ECL input). LOW for nornal operation. |
| 12 | ***SENDCLOCK2*** | I | "CLK2" pattern enable (ECL input). LOW for normal operation. |
| 25 | $V_{REF}$ | | ECL reference level input. |
| 4, 10, 18, 30, 36, 43, 49 | $V_{CC}$ | | Ground connection. |
| 7, 46 | $V_{TT}$ | | -2.0 V supply for internal reference generation & low power logic. |
| 23, 33 | $V_{EE}$ | | -5.2 V supply for high speed logic. |
| 3, 5, 6, 13-16, 26-29, 31, 32, 34, 35 | ***NC*** | | No connection. |

## VS8002 PIN DIAGRAM




## VS8002 PIN DESCRIPTION

| Pin # | Name | I/O | Description |
|---|---|---|---|
| 17, 19 | ***CLK, NCLK*** | I | High speed clock input (capacitively coupled) |
| 15, 16 | ***MUXDATA, NMUXDATA*** | I | High speed serial data input |
| 41, 42, 44, 45, 47, 48, 50, 51, 3, 5, 6, 8 | ***DO-D11*** | O | Parallel data outputs (ECL) |
| 31 | ***DCLOCK*** | I | Internally generated divide by 12 clock output (ECL) |
| 28 | ***SKIP*** | I | Causes one high speed serial bit to be skipped for word boundary shifting. A SKIP input causes data to become invalid for up to 3 DCLOCK periods. (ECL input) |
| 35 | ***ALIGNED*** | O | Indicates that the demux has found a match on three consecutive DCLOCK cycles (ECL output). Float or VCC for normal operation. |
| 34 | ***ERROR*** | O | Indicates that the internally generated pattern did not match the incoming data on at least one DCLOCK cycle since the error latch was reset (ECL output). Float or VCC for normal operation. |
| 27 | ***TEST*** | I | Test hardware enable (ECL input). LOW for normal operation. |
| 39 | ***FRAME*** | O | Test pattern repeat confirmation (ECL output). Float or VCC for nornal operation. |
| 40 | ***MATCH*** | O | Indicates that the internally generated pattern matched the incoming demultiplexed data (ECL output). Float or VCC for normal operation. |
| 11 | ***SYNCPATT*** | I | Test pattern enable (ECL input). LOW for nornal operation. |
| 12 | ***SENDCLOCK2*** | I | "CLK2" pattern enable (ECL input). LOW for normal operation. |
| 25 | $V_{REF}$ | I | ECL reference level input. |
| 4, 10, 18, 30, 36, 43, 49 | $V_{CC}$ | | Ground connection. |

**VS8002 PIN DESCRIPTION** (con't)

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| Pin # | Name | I/O | Description |
|---|---|---|---|
| 7, 46 | $V_{TT}$ | I | -2.0 V supply for internal reference generation & low power logic. |
| 23, 33 | $V_{EE}$ | I | -5.2 V supply for high speed logic. |
| 1, 2, 9, 13, 14, 20-22, 24, 26, 29, 32, 38, 52 | NC | | No connection. |

## SELF-TEST FEATURE

### Test Description

The following is a description of the circuitry and method used to implement the self-test feature incorporated in the VS8001 and VS8002.

Because of the difficulty and cost associated with manually generating and detecting high speed data streams, the VS8001 and VS8002 have been designed with circuitry which enables the user to perform an at-speed functional evaluation of the parts in a system environment by using a single external stimulus: the high speed clock. The test circuitry, distributed between the two parts, consists of two pattern generators, control logic, and a twelve-bit comparator. The multiplexer generates a serial data pattern, and the demultiplexer detects the pattern and compares it for correctness.

The pattern generator on the VS8001 creates twelve-bit patterns for the multiplexer, which then converts these twelve-bit words into a serial data stream. The serial output of the multiplexer is connected to the serial input of the demultiplexer. The demultiplexer converts this high speed serial data bit stream into twelve bit parallel data and compares the incoming data to patterns created by its own test pattern generator.

The pattern generators can make three different patterns: a synchronizing pattern (called *"SYNC"*), a transition pattern (called *"CLK2"*), and a pseudo-random pattern that repeats every 4095 words. The *SYNC* pattern is sent first to allow the demultiplexer to find word boundaries. During synchronization, the ***ALIGNED*** pin on the demultiplexer signals that the comparator has found a match on three successive words. This is followed by the *CLK2* pattern which signals the demultiplexer that the pattern is about to change to the 4095 word pseudo-random pattern. This allows the demultiplexer to start its pseudo-random pattern at the appropriate time to match the pattern being received on the incoming data stream from the multiplexer.

The incoming data pattern and the locally generated test pattern go to a twelve-bit comparator. The result of the comparison appears at the ***MATCH*** pin of the demultiplexer. A latch, which is reset upon entering the pseudo-random mode, detects any mismatch between the incoming data pattern and the locally generated test pattern. The latch state appears at the ***ERROR*** pin of the demultiplexer. On both parts, a one period pulse on the ***FRAME*** pin signals that the pseudo-random pattern is repeating.

The test is controlled with the ***TEST*** and ***SYNCPATT*** pins on both parts. The diagram on the following page shows the self-test setup in more detail.

## TEST HARDWARE BLOCKS

### VS8001

The test hardware on the MUX consists of a 12-bit pattern generator with control logic. The individual blocks are described below.

## SELF-TEST SETUP

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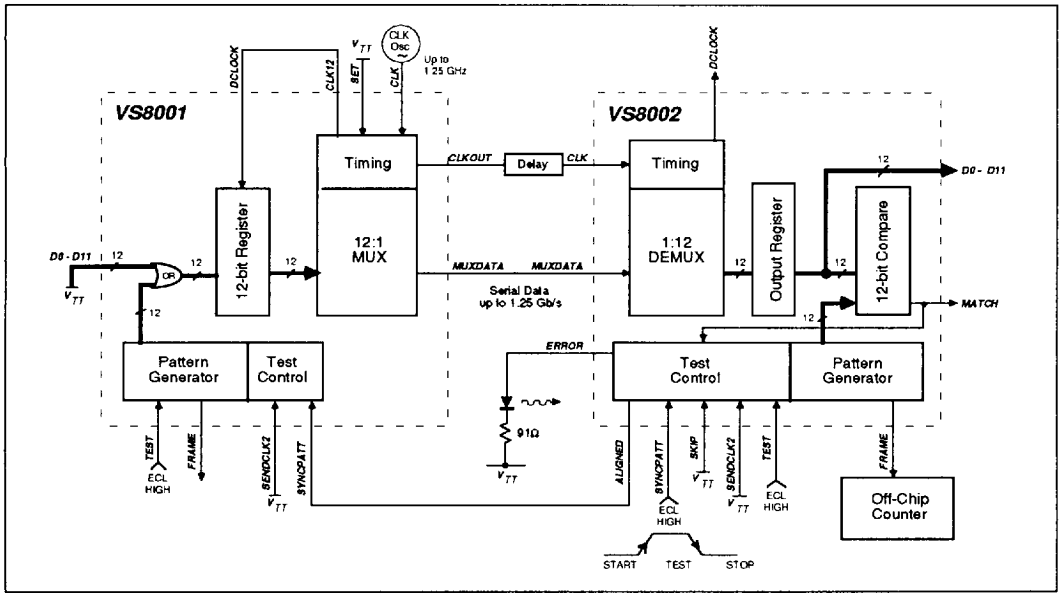



### Pattern Selector FSM

The pattern selector state machine selects the pattern generated by the MUX pattern generator. When ***SYNCPATT*** is LOW, the pattern selector state machine is reset and the pattern generator generates the *SYNC* pattern.

### Pattern Generator

The pattern generator contains logic for static generation of two different 12-bit patterns and dynamic generation of a pseudo-random 12-bit pattern. The static patterns are the *"SYNC"* pattern (100101010110) and the *"CLK2"* pattern (101010101010). The pseudo-random pattern provides a pattern length of 4095 ***DCLOCK*** cycles. The first pattern in the sequence (001010101010) is explicitly detected. The result appears at the ***FRAME*** pin as a HIGH signal for one ***DCLOCK*** period out of every 4095 while in pseudo-random mode.

### VS8002

The test hardware on the DEMUX consists of a 12-bit pattern generator with control logic and a 12-bit comparator. The individual blocks are described briefly below.

### Pattern Selector FSM

The pattern selector state machine selects the pattern generated by the DEMUX pattern generator. It also resets the error latch upon entering the pseudo-random test mode. When ***SYNCPATT*** is LOW, the pattern selector state machine is reset and the pattern generator generates the *SYNC* pattern.

### Aligned FSM

When ***SYNCPATT*** is LOW and ***MATCH*** is HIGH for three consecutive ***DCLOCK*** cycles, the ***ALIGNED*** signal will go HIGH on the next cycle. This is called the "aligned" state. Once aligned the ***ALIGNED*** pin will stay HIGH until ***SYNCPATT*** goes LOW, forcing a reset of the aligned state

machine. When aligned the DEMUX will not issue internally generated skip signals.

### *ERROR* Latch

The *ERROR* latch is set if *TEST* is HIGH and *MATCH* is LOW. It is reset when entering the aligned state or when the *TEST* pin is LOW. The purpose is to latch any mismatch detected during the pseudo-random test.

### *SKIP* Edge Generator FSM

If an internally generated skip is requested, this state machine translates the request to a rising edge and locks out internally generated skip signals for four *DCLOCK* cycles.

### Pattern Generator

The pattern generator contains logic for static generation of two different 12-bit patterns and dynamic generation of a pseudo-random 12-bit pattern. The static patterns are the *"SYNC"* pattern (100101010110) and the *"CLK2"* pattern (101010101010). The pseudo-random pattern provides a pattern length of 4095 *DCLOCK* cycles. The first pattern in the sequence (001010101010) is explicitly detected. The result appears at the *FRAME* pin as a HIGH signal for one *DCLOCK* period out of each 4095 while in the pseudo-random mode.

## TEST PINS

### VS8001

There are 4 pins on the VS8001 which are used only for testing the part. The input pins used only for testing are *TEST, SYNCPATT,* and *SENDCLK2*. For normal operation, the *TEST* pin must be forced to ECL LOW or tied to $V_{TT}$. The one output pin used only for testing is *FRAME*. For normal operation, the termination of the *FRAME* pin is not critical. Usually, the output driver will be off. This pin may be properly terminated to $V_{TT}$, left floating, or tied to the $V_{CC}$ supply. In test operations, all of the test pins should be properly terminated to $V_{TT}$.

### *TEST* (ECL input pin)

The input, *TEST,* may be driven asynchronously. When *TEST* is LOW, all effects of the self-test hardware on the results of the MUX are asynchronously disabled. Explicitly, when the *TEST* pin is LOW, the output of the pattern generator is all zeros (000000000000).

When the *TEST* pin is HIGH and the high speed *CLK* and *DCLOCK* inputs are driven appropriately, the part is in *"test"* mode. In test mode, the self-test hardware is allowed to sequence and may effect the results on the output pins of the MUX chip. In test mode the 12 parallel data input pins must be driven to ECL LOW or tied to the $V_{TT}$ power supply.

### *SYNCPATT* (ECL input pin)

The input pin, *SYNCPATT,* should be driven synchronously with respect to *DCLOCK*. When *SYNCPATT* is LOW, the pattern selector state machine will be forced to the zero state. If in test mode and *SYNCPATT*= LOW, the MUX pattern generator will generate the *"SYNC"* pattern (100101010110). This pattern will appear at the high speed serial output port of the MUX (left bit first). The DEMUX expects to receive this pattern for word boundary alignment.

When in test mode and *SYNCPATT* goes HIGH, the MUX pattern generator will change the pattern on the next *DCLOCK* cycle. The *CLK2* pattern (101010101010) will be generated for 3 *DCLOCK* periods to signal a change in test mode. The next *DCLOCK* cycle will start a pseudo-random pattern that repeats every 4095 *DCLOCK* cycles. In test mode, the pseudo-random pattern sequence continues until *SYNCPATT* goes LOW or *SENDCLK2* goes HIGH.

In the intended test flow, the *ALIGNED* signal from the DEMUX is used to drive the *SYNCPATT* input on the MUX chip. This allows the DEMUX to determine the time necessary for alignment using the *SYNC* pattern before the MUX changes to the pseudo-random test mode.

### *SENDCLK2* (ECL input pin)

The input pin, ***SENDCLK2***, is provided to force the pattern generator to generate the ***CLK2*** pattern instead of the pseudo-random pattern. This feature is not intended for use within the typical test flow.

### *FRAME* (ECL output pin)

***FRAME***=HIGH indicates that the internally generated pattern (001010101010) was sent to the multiplexer's parallel data input register on the previous ***DCLOCK*** cycle. This pattern is the first word of the 4095 word pseudo-random sequence. While in the pseudo-random mode, the ***FRAME*** pin has a HIGH signal for one ***DCLOCK*** period out of every 4095.

### VS8002

There are some pins on the VS8002 which are used only for testing the part. The input pins used only for testing are ***TEST, SYNCPATT***, and ***SENDCLK2***. For normal operation, the ***TEST*** pin must be forced to ECL LOW or tied to the $V_{TT}$ supply. For normal operation, ***SYNCPATT*** and ***SENDCLK2*** may be left floating, forced to ECL LOW, or tied to the $V_{TT}$ supply. The output pins used only for testing are ***MATCH, ALIGNED, ERROR***, and ***FRAME***. For normal operation, the termination of these output pins is not critical. Usually, the output drivers will be off. These pins may be properly terminated to $V_{TT}$, left floating, or tied to the $V_{CC}$ supply. In test operations, all of the test pins should be properly terminated to $V_{TT}$

### TEST (ECL input pin)

The input pin, ***TEST***, may be driven asynchronously. When ***TEST*** is LOW, all effects of the self-test hardware on the results of the DEMUX are asynchronously disabled. Explicitly, when the ***TEST*** pin is LOW, no ***SKIPs*** (word rotation) will be internally generated and the error latch input will be forced LOW.

When the ***TEST*** pin is HIGH and the high speed ***CLK*** inputs are driven appropriately, the part is in *"test"* mode. In test mode, the self-test hardware is allowed to sequence and may effect the results on the output pins of the DEMUX chip.

### SYNCPATT

The input pin, ***SYNCPATT***, should be driven synchronously with respect to ***DCLOCK***. When ***SYNCPATT*** is LOW, the pattern selector, word alignment selector, and ***SKIP*** edge generator state machines will all be forced to their zero states. In this state, the DEMUX pattern generator will generate the *SYNC* pattern (100101010110). This allows external word alignment using the ***MATCH*** output pin and the ***SKIP*** input pin.

When in test mode and ***SYNCPATT*** goes HIGH, the DEMUX pattern generator will continue to generate the *SYNC* pattern until certain conditions are met. If the generated pattern matches the demultiplexed input data, then ***MATCH*** will go HIGH. If no match is detected, then the DEMUX will issue itself a ***SKIP*** signal (through the ***SKIP*** edge generator state machine). After a ***SKIP*** has been issued in this manner, the ***MATCH*** signal will be ignored for four ***DCLOCK*** cycles so that transient data during word boundary rotation cannot cause an unintended ***SKIP*** to occur. In this state, the DEMUX will react normally to externally driven ***SKIP*** signals, so the ***SKIP*** pin should be held LOW for this test. Then, the DEMUX will issue ***SKIP*** signals until ***MATCH*** is HIGH for three consecutive ***DCLOCK*** cycles. On the following ***DCLOCK*** cycle the ***ALIGNED*** signal will go HIGH. Call this the *"aligned"* state. Once aligned, the DEMUX will not issue internally generated ***SKIP*** signals unless the aligned state machine is reset by cycling the ***SYNCPATT*** input.

The expected test sequence is that the *SYNC* pattern will be received until the DEMUX is aligned. Then a *CLK* divide-by-2 pattern (101010101010) will be received for 3 ***DCLOCK*** cycles to signal a change in test mode. The next ***DCLOCK*** cycle will start a pseudo-random pattern that repeats every 4095 ***DCLOCK*** cycles. The DEMUX pattern selector state machine looks for ***ALIGNED*** to be HIGH and ***MATCH*** to be LOW.

This signals a change in test pattern on the input data stream. Notice the ***CLK2*** pattern is not specifically detected, only a mis-match. Thus, once aligned, an error in detecting the *SYNC* pattern will put the DEMUX in pseudo-random test mode.

**SENDCLK2** (ECL input pin)

The input pin, ***SENDCLK2***, is provided to force the pattern generator to generate the ***CLK2*** pattern instead of the pseudo-random pattern. This feature is not intended for use within the typical test flow.

**MATCH** (ECL output pin)

The ***MATCH*** pin is the registered output of the 12-bit comparator. ***MATCH***= HIGH indicates that the internally generated pattern matched the incoming demultiplexed data on the previous ***DCLOCK*** cycle.

**ALIGNED** (ECL output pin)

***ALIGNED***= HIGH indicates that the DEMUX has found a match on three consecutive ***DCLOCK*** cycles. When ***ALIGNED*** first goes HIGH the DEMUX is ready to transition to the pseudo-random pattern mode. In the intended test flow ***ALIGNED*** is used to drive the ***SYNCPATT*** input on the MUX chip.

**ERROR** (ECL output pin)

***ERROR***= HIGH indicates that the internally generated pattern did not match the incoming demultiplexed data on at least one ***DCLOCK*** cycle since the ***ERROR*** latch was reset.

**FRAME** (ECL output pin)

***FRAME***= HIGH indicates that the internally generated pattern (001010101010) was sent to the 12-bit comparator on the previous ***DCLOCK*** cycle. This pattern is the first word of the 4095 word pseudo-random sequence. While in the pseudo-random mode, the ***FRAME*** pin has a HIGH signal for one ***DCLOCK*** period out of every 4095.

## VS8001/VS8002 DUT BOARDS

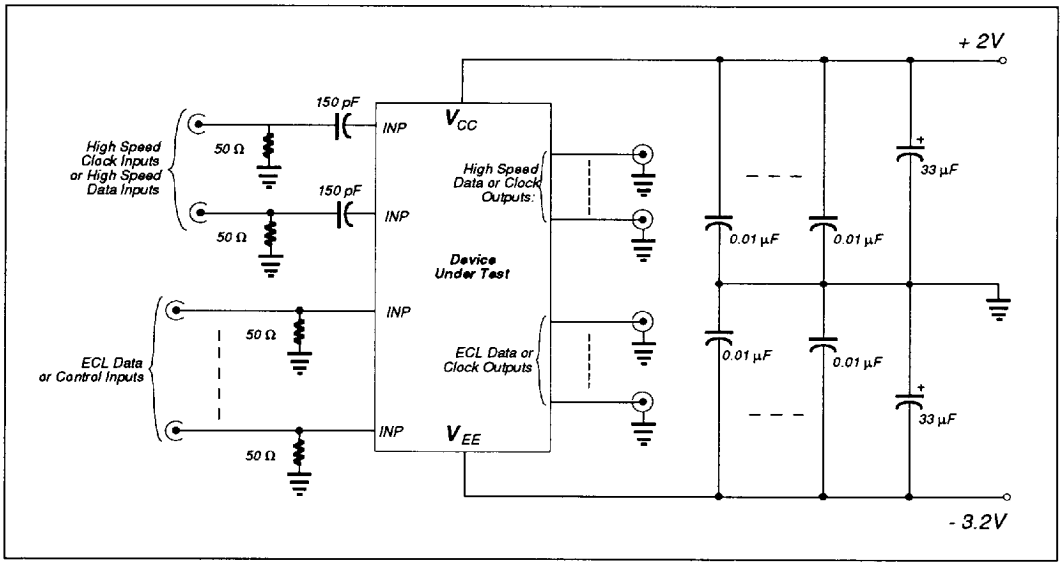
The VS8001DUT and VS8002DUT are circuit boards which provide a test bed suitable for evaluating the performance characteristics of the VS8001 12:1 Multiplexer and the VS8002 1:12 Demultiplexer in 52 pin leadless chip carriers (LCC).

A schematic of the evaluation board is shown below. This board provides controlled impedance transmission lines for all signals and decoupling for the power supplies. The signal traces have a characteristic impedance of 50 Ω. All ECL input lines are terminated with 50 Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150 pF blocking capacitors. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated with 50 Ω in the measuring instrument.

Normally, the VS8001 and VS8002 operate in an ECL environment with standard ECL power forms (Ø V, -2.0 V, and -5.2 V). In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus.

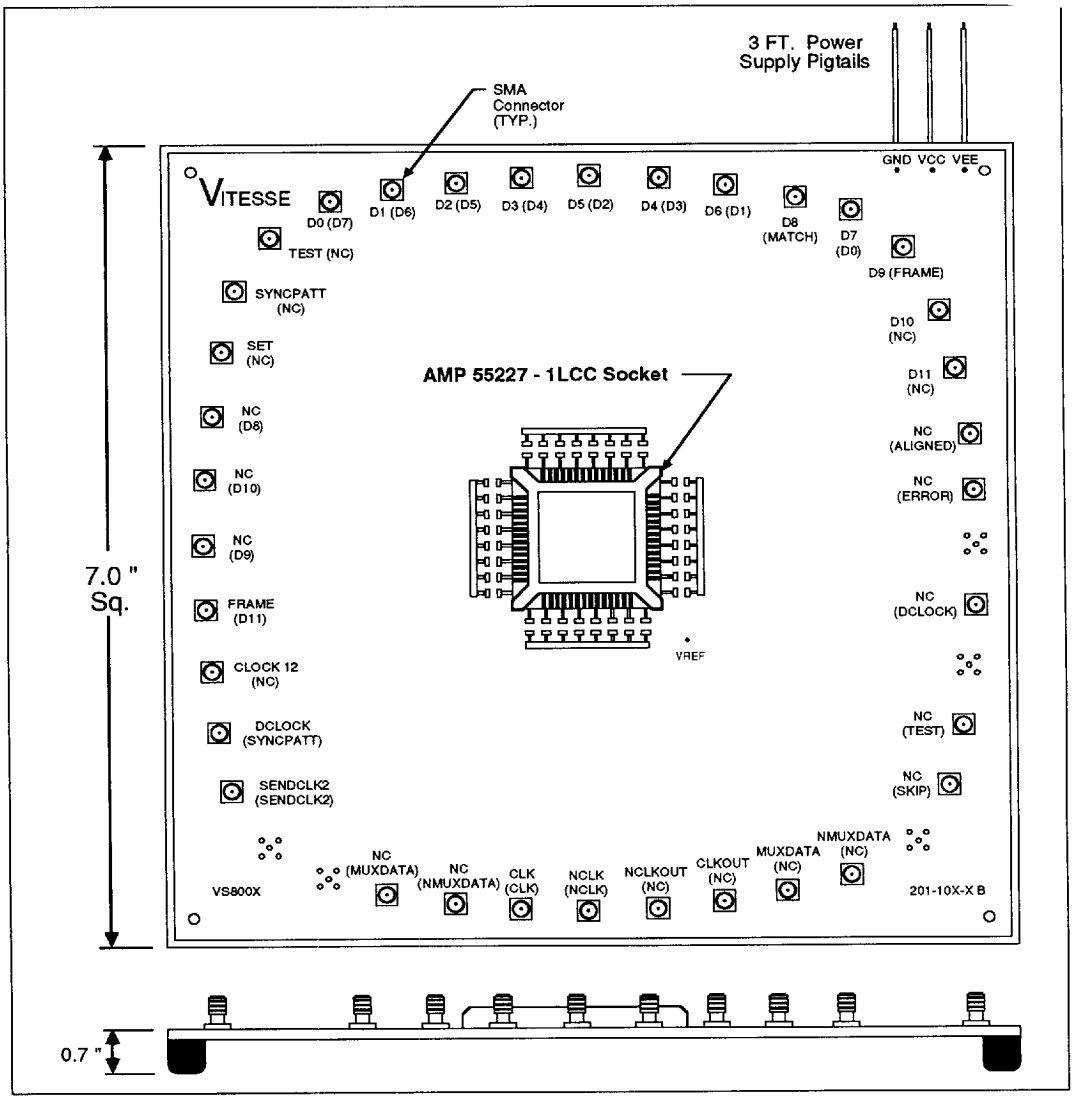
The device socket is an AMP 55227-1LCC socket and was chosen for minimum inductance and shortest possible stub length. The figures on the next page show the physical dimensions as well as the names of the connectors on the evaluation boards.

## VS8001/VS8002 DUT BOARD SCHEMATIC



## VS8001/VS8002 DUT BOARDS

T-51-12




*NOTES:* *1) This drawing represents both the VS8001 and VS8002 configurations. (Connection labels given in parentheses are for the VS8002.)*
*2) NC = No connection.*