Data Sheet
VSC7120

1.0625 Gbit/sec Channel Repeater / Hub Circuit

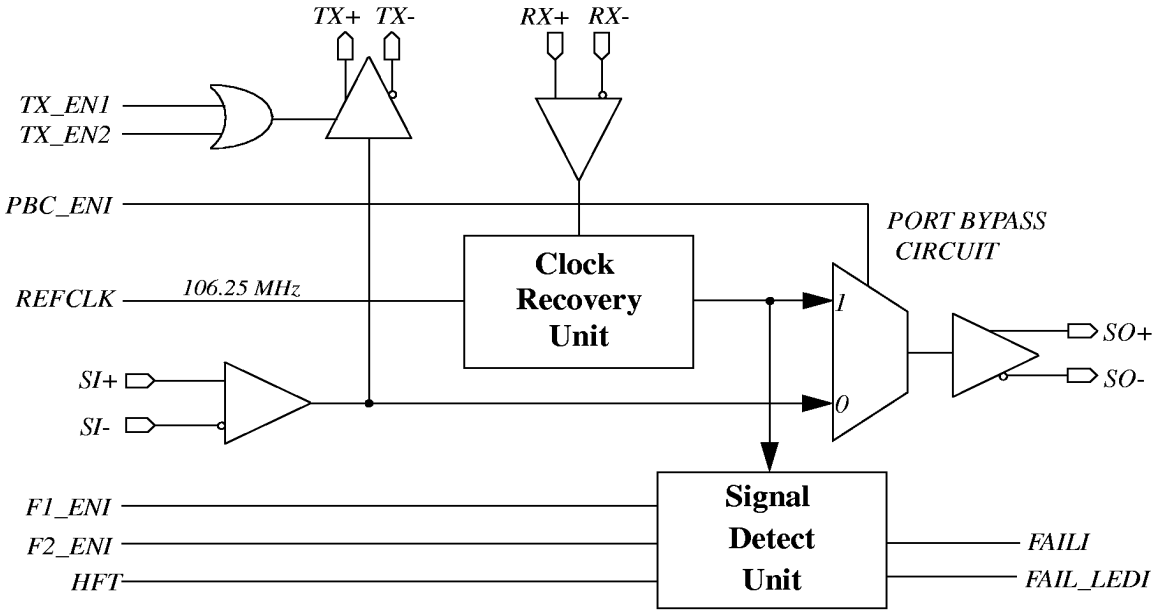
Features

- ANSI X3T11 Fibre Channel Compatible
- Monolithic Clock Recovery Unit
  - Retimes & Buffers Received Data
  - No External Components
- Digital Signal Detect Unit
  - Run Length Violation Detector
  - K28.5 Detector
  - Power-Down Feature
- Port Bypass Circuit
- Suitable for Both Coaxial and Optical Link Applications
- Low Power Operation
  - < 1.3W, Typical, for Hub Mode
  - < 1.0W, Typical, for Repeater Mode
- 106.25 MHz Reference Clock
- 52-Pin, 10x10mm Thermally Enhanced PQFP
- Single 3.3V Supply

General Description

The Fibre Channel Repeater / Hub Circuit is used in full-speed (1.0625 Gb/s) Disk Arrays, Hubs and Switches. It contains a monolithic Clock Recovery Unit (CRU), a digital Signal Detect Unit (SDU) and a Port Bypass Circuit (PBC). The CRU may be used alone to implement a general purpose Repeater needed for many Disk Array and Switch applications where a retimed and buffered signal is required. The CRU, SDU and PBC may also be used together to implement a single-chip Arbitrated Loop Hub Node. As a Hub node, the VSC7120 retimes/buffers incoming serial data, detects whether a valid signal is present and allows isolation of non-functional devices from the Loop.

VSC7120 Block Diagram



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Functional Description

The VSC7120 contains three functional blocks: a Clock Recovery Unit (CRU), a Signal Detect Unit (SDU), and a Port Bypass Circuit (PBC). These circuits operate at the full 1.0625 Gb/s serial data rate and perform functions useful in Disk Arrays, Switches or Fibre Channel Arbitrated Loop (FC-AL) Hubs as repeaters and fault isolators.

The CRU is a low jitter-peaking PLL which recovers the baud rate clock from the RX serial data input, retimes the RX data then retransmits it through the embedded PBC to the SO outputs. The CRU retimes the incoming data in order to attenuate jitter and increase the amplitude of the signal at the SO outputs. This provides downstream users of this data with a signal of known amplitude and jitter.

The SDU performs two digital checks for valid data transmission to indicate whether the external node is functional. The first check, enabled by F1_ENI being LOW, monitors the RX inputs for Fibre Channel 8B/10B run length violations. All valid 8B/10B codes have less than six consecutive identical bits so if incoming data has six or more consecutive identical bits, an error will be indicated on the FAILI/FAIL_LEDI outputs. The second method, enabled by F2_ENI, monitors the RX inputs for a bit pattern ('1111010') found in Fibre Channel Ordered Sets which should be present at least once every 20 microseconds. The SDU provides the building blocks needed by Hubs to implement an extremely reliable and repeatable mechanism for determining when to isolate the external node from the Loop and when to reconnect it to the Loop.

The PBC is a 2:1 Multiplexer which passes recovered data from the CRU to the SO outputs (if PBC_ENI is HIGH) or passes SI data to the SO outputs (if PBC_ENI is LOW). The SI inputs are always routed to the TX outputs which are gated by the TX_EN1 and TX_EN2 inputs. If both TX_EN1 and TX_EN2 are LOW, then TX+ will be HIGH and TX- will be LOW. Otherwise, the TX outputs will be enabled.

The VSC7120 has two modes of operation as follows:

Repeater Mode
Hub Mode

Repeater Mode

In Repeater Mode, the VSC7120 operates only to retime and buffer serial data from the RX inputs onto the SO output in order to attenuate jitter and amplify the signal. This mode is useful to remove high frequency jitter from the serial data and to amplify the signal to its full voltage swing. For FC-AL storage subsystems, the VSC7120 Repeater is useful in insulating the disk drive array subsystem (i.e. JBOD - Just a Bunch Of Disks) from the node connected to it as shown in Figure 1. A more detailed application example is shown in Figure 2. Input data from the upstream node may be noisy and degraded due to long cabling but the VSC7120 Repeater cleans the incoming Fibre Channel serial data prior to its use by the first disk drive. Similarly, accumulated noise inside the array may be eliminated by using a VSC7120 between the array and the downstream FC-AL device. In very large disk arrays, repeaters may be required periodically within the array to remove serial data degradation as a result of data transported over connectors, board traces, and port bypass circuits.

The Clock Recovery Unit in the VSC7120 uses an automatic lock-to-ref technique that eliminates the need for any external control logic to lock the CRU's PLL to REFCLK when data is not present on the RX input. When the RX inputs are removed, the PLL will drift away from the REFCLK frequency (i.e. 106.25 MHz +/- 100 ppm). Internal circuitry halts this drift when the PLL reaches approximately +/- 1.5% of the REFCLK fre-

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quency. When RX data is reapplied, the CRU is able to lock onto the new data very quickly since the PLL is quite near the frequency of the data. This automatic Lock-to-Reference feature is extremely important in repeater applications because an intelligent state machine or microcontroller is usually not present to control this function.

Figure 1: FC-AL JBOD Application for Repeaters

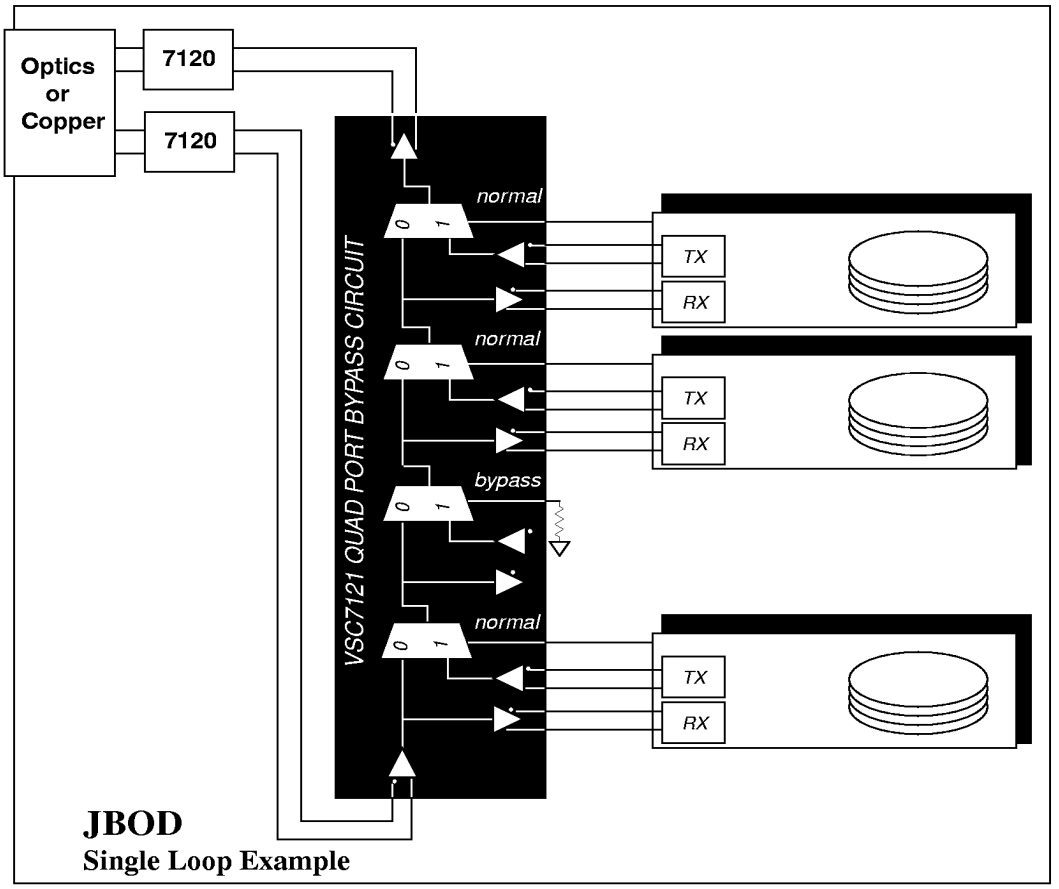

Figure 1 shows the VSC7120 being used in a repeater application. The PBC_ENI is set HIGH to pass the re-timed RX data to the SO outputs. The TX outputs would normally be disabled (TX_EN1=TX_EN2=LOW) to reduce power and noise. The SI inputs would be unused and should be terminated in order to eliminate oscillations. The SDU circuit can be powered down by disconnecting its supply pins (VSS_SDU and VDD_SDU) as shown in Figure 2.

Two styles of output buffers are provided on the VSC7120 to allow the user to optimize their system design. The TX outputs are full powered buffers capable of driving long cables or other Fibre Channel devices. The SO outputs are half-powered buffers which are not optimized for driving long cables but can drive Fibre

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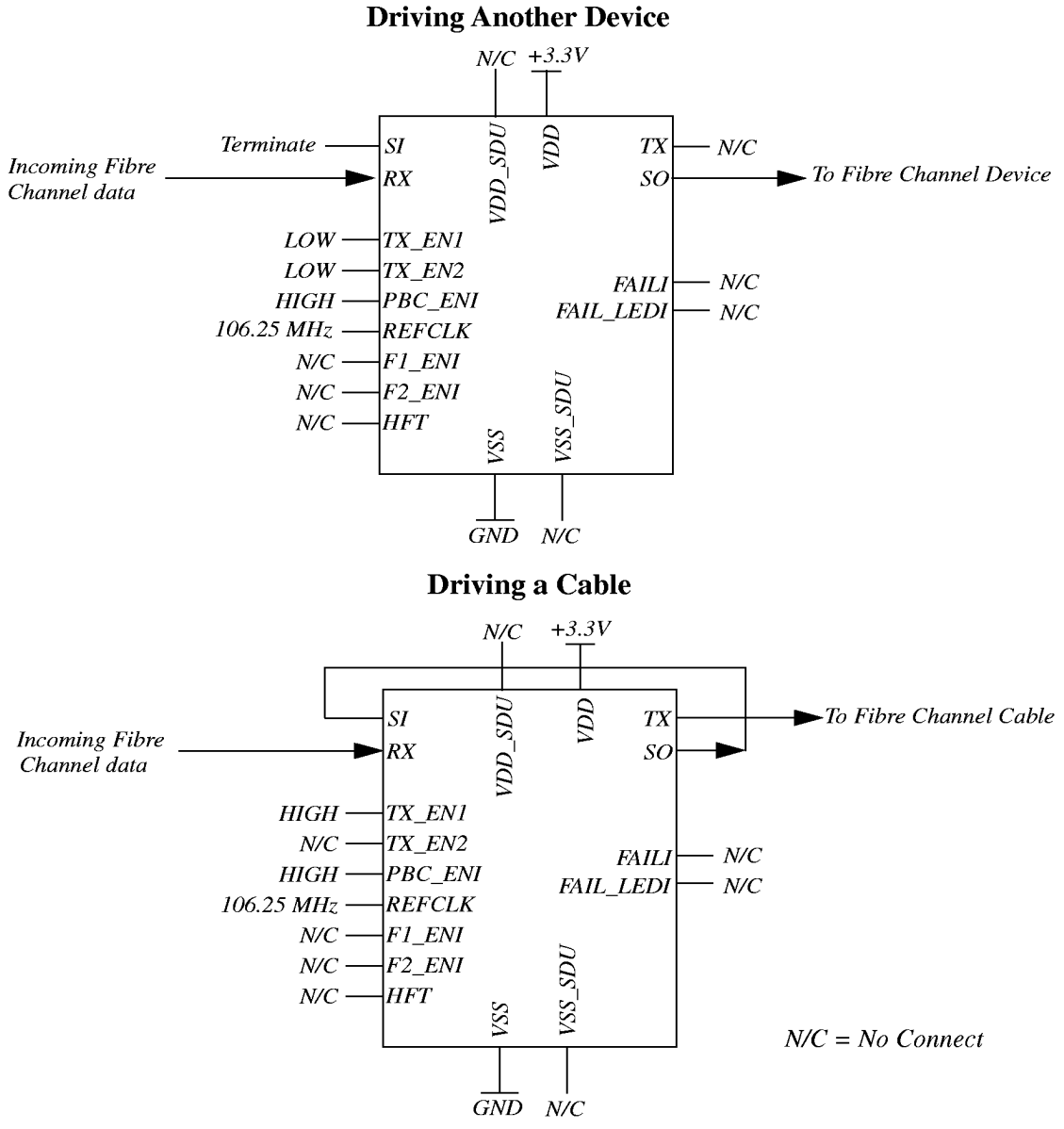
Channel devices such as O/E Modules, board traces and disk drives. In most repeater applications, SO would be adequate. However, in applications where the VSC7120 would drive long cables, the SO outputs should be connected to the SI inputs where the data will be routed to the TX outputs. This allows the user to optimize the design to reduce power and maximize signal quality.

Figure 2: VSC7120 in Repeater Mode



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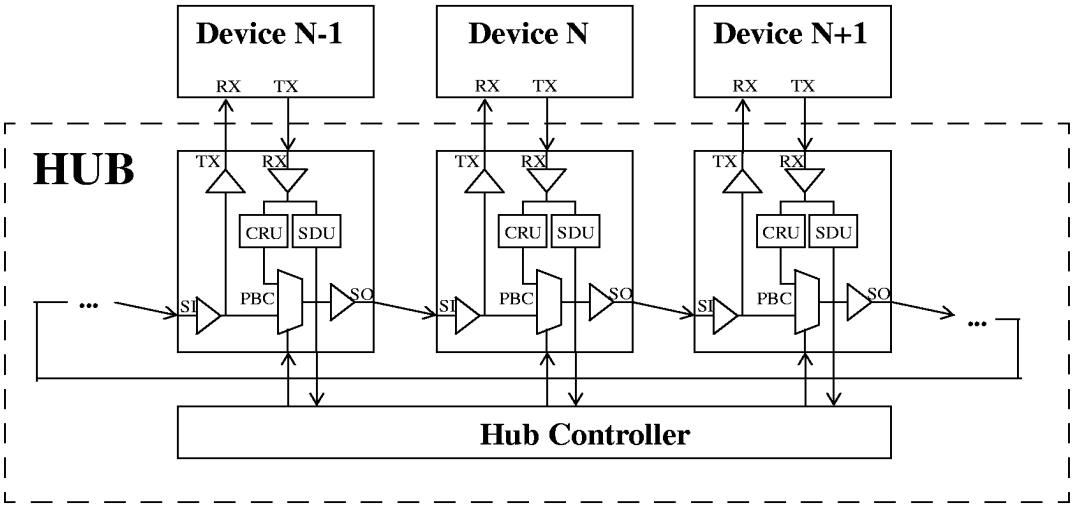
Hub Mode

The VSC7120 can act as a single-chip Hub node as shown in Figure 3. In this figure, only three Fibre Channel Arbitrated Loop nodes are shown, with each connected to external devices using point-to-point links. This implements a "Virtual Loop" using a "Physical Star" configuration. The functions of a Hub node are:

- Send data from the previous Hub node, N-1, to the external device, N (SI to TX)
- Retime / Rebuffer incoming data from the external device (RX & CRU)
- Monitor incoming data for valid Fibre Channel signals (SDU)
- Pass recovered external data to next Hub node, N+1, if valid (CRU to SO)
- Pass data from previous Hub node, N-1, to next Hub node, N+1, if external data is invalid (SI to SO)

Figure 3: FC-AL Hub Application



The VSC7120 implements most of the Hub node function but requires an external Hub Controller to use the SDU's outputs to control the PBC. The SDU and PBC provide the building blocks needed to isolate non-functioning external devices from the "Loop" but most customers wish to implement their own algorithms for determining when to isolate a device and when to reconnect a device. An FC-AL Hub should react only to catastrophic events such as open lines or shorts but should not respond to bit errors which are handled through standardized Fibre Channel protocols. This "Hub Controller" may be a microcontroller, FPGA or even a simple PLD-based state machine.

A more detailed view of the VSC7120 in Hub Mode is shown in Figure 4. In order to pass SI input data to TX, TX_EN1 is tied HIGH and TX_EN2 is left open. The CRU continuously locks onto RX data, retimes it and passes the recovered data to the PBC. The SDU monitors the recovered RX data under control of F1_ENI, F2_ENI and HFT (more about these signals later). The FAIL_LEDI is intended to drive an Activity LED. The FAILI output is used by the Hub Controller to configure the PBC with the PBC_ENI input. If FAILI is negated,

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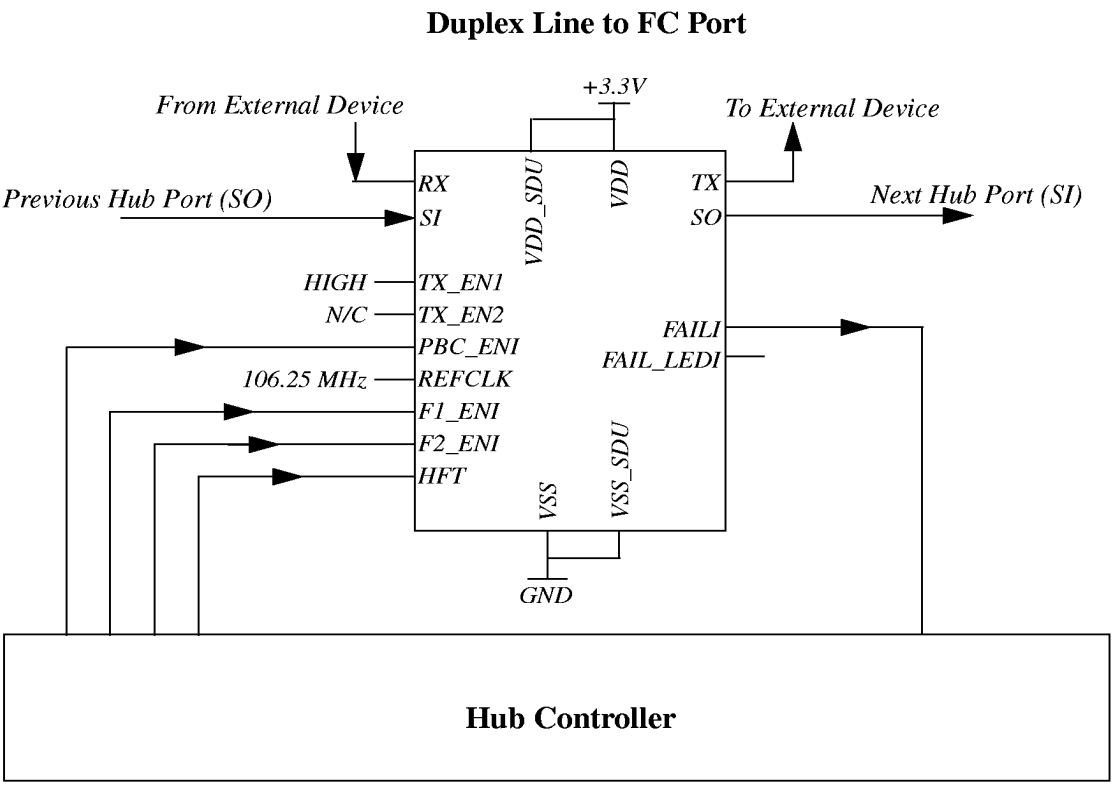
then the Hub would normally pass recovered RX data to the next Hub Node via the SO outputs. If FAILI is asserted, then the previous Hub Node's data on SI would normally be passed to the next Hub Node via the SO outputs. The Hub Controller should implement some sort of algorithm to qualify or filter FAILI before changing the state of PBC_ENI.

Figure 4: Fibre Channel Hub Port



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Signal Detect Unit Behavior

The Signal Detect Unit indicates to the Hub Controller whether the RX input has valid Fibre Channel data. Two digital mechanisms exist to detect valid data. The first, called F1, is enabled when F1_ENI is LOW. This monitors incoming RX data for more than six consecutive ones or zeros. Valid 8B/10B data will have no more than five consecutive ones or zeros. If more than six consecutive ones or zeros are encountered, then the SDU will assert the fail outputs (FAILI and FAIL_LEDI). The second method, called F2, is enabled when F2_ENI is LOW. Valid Fibre Channel data contains K28.5 characters at least every 20 microseconds. The F2 function within the SDU looks for a 7-bit pattern found in the K28.5 ('1111010') and asserts the fail outputs if this pattern is not encountered within the 20 microsecond period.

A Fibre Channel active Hub should react only to catastrophic failure events, such as open lines, since the Fibre Channel protocol handles frame level error conditions. For this reason, the VSC7120's SDU fail outputs are designed to be asynchronously polled and processed by the Hub Controller to develop a high-level, intelligent Link Status in order to control the PBC. This allows the Hub controller, which could be a microprocessor, FPGA or even a PLD, to process all the nodes in the Hub with a common clock and simple control logic. The designer can "program" the sensitivity of the Hub Nodes to various error conditions and error rates.

The HFT, High Frequency Timer, input to the SDU controls the F1 and F2 Registers (see the Block Diagram in Figure 6). HFT is debounced internally with a clock that is one eighth of the REFCLK frequency. The HFT input is considered asynchronous to the VSC7120 since the user cannot access this internal clock but HFT does have a minimum pulse width (250 nsec). The F1_ENI and F2_ENI gate the F1 and F2 register outputs to FAILI and FAIL_LEDI.

When HFT goes low, the F1 and F2 registers are reset. The F1 detector output goes HIGH when a run length violation occurs. The F2 detector output goes LOW (indicating failure) until the K28.5 7-bit pattern is encountered within the prescribed period. F1 and F2 fault detection have different reaction times with F1 reacting quickly (<0.5 microseconds) and F2 reacting slowly (20 microseconds). Moreover, F1 and F2 operate in an opposing manner. The rising edge of HFT is commonly used to sample the fail outputs in the Hub Controller. The user must sample at the lowest rate if both are simultaneously enabled or the user may alternately poll F1 and F2 to benefit from both fast reaction time and protection from oscillating signal failures. The VSC7120 allows flexibility for the system designer to tailor fault detection for their particular system environment, failure mechanisms, and reaction requirements.

Figure 5: REFCLK Timing Waveforms

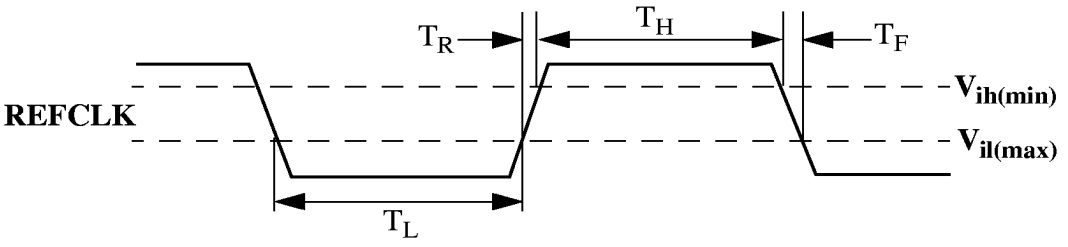

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Figure 6: Block Diagram: Signal Detect Unit

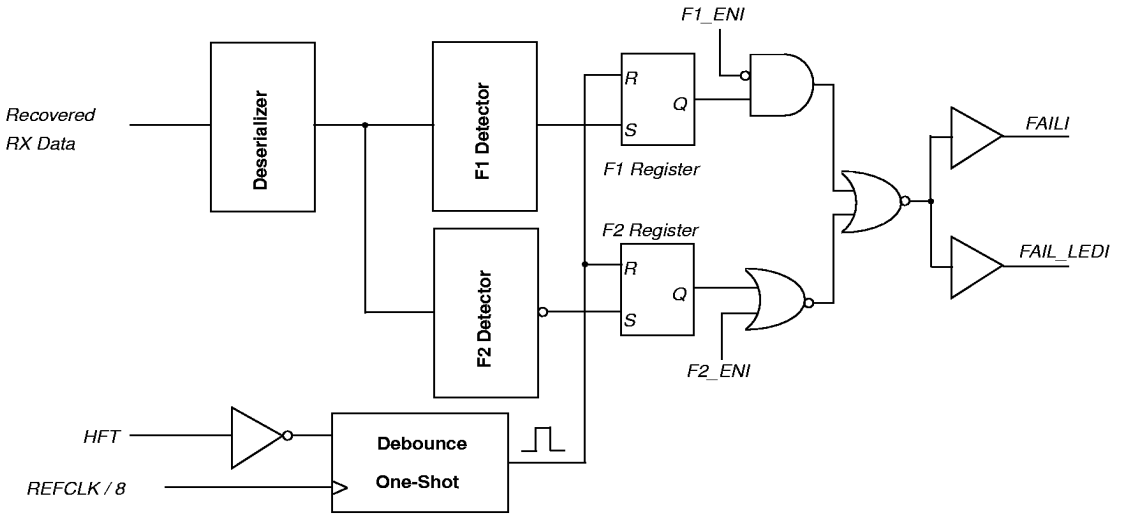
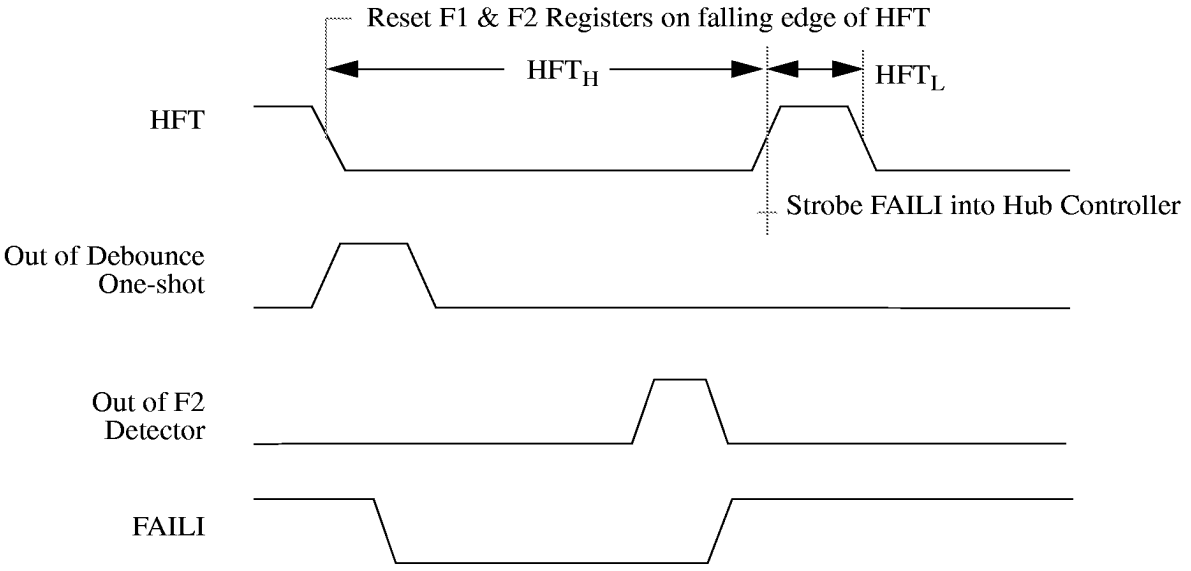


Figure 7: VSC7120 HFT Timing Waveforms



Note: Nominal Fibre Channel signal at RX input.
If only F1 is enabled, High and Low times should be greater than 0.5 usec.
If F2 is enabled, High and Low times should be greater than 20 usec.

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AC Characteristics

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
HFT_H, HFT_L	HFT High and Low Time	250	—	ns	
T_H,T_L	REFCLK High and Low Time	2.5	—	ns	
T_R,T_F	REFCLK Rise and Fall Time	—	3.5	ns	
FR	REFCLK Frequency Range	105	107	MHz	
FT	REFCLK Frequency Tolerance	-100	+100	PPM	Difference between REFCLK and RX data frequency.
DC	REFCLK Duty Cycle	40/60	—	%	
SO Jitter Allocation					
RJ	SO Random Jitter (RMS)	—	20	ps	RMS, tested on a sample basis
DJ	SO Deterministic Jitter (p-p)	—	100	ps	Peak to peak, tested on a sample basis
JT	Jitter Transfer from RX to SO	—	0.5	dB	

DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.2 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.2 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	—	—	V	
V_{IL}	Input LOW voltage (TTL)	—	—	0.8	V	
I_{IH}	Input HIGH current (TTL)	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current (TTL)	- 500	—	-50	µA	V_{IN} = 0.5 V
V_{DD}	Supply voltage	3.14	—	3.47	V	V_{DD} = 3.30V±5%
$I_{DD(Hub)}$	Supply Current (SDU Enabled)	—	340	450	mA	Outputs open, V_{DD} = V_{DD} max
$I_{DD(RPT)}$	Supply Current (SDU not powered)		260	350	mA	Outputs open, V_{DD} = V_{DD} max
$P_{D(HUB)}$	Power dissipation (SDU Enabled)	—	1.35	1.56	W	Outputs open, V_{DD} = V_{DD} max
$P_{D(RPT)}$	Power dissipation (SDU not powered)		0.96	1.22	W	Outputs open, V_{DD}=V_{DD} max
$\Delta V_{OUT(SO)}$	SO Output differential peak-to-peak voltage swing	1000	—	2200	mVp-p	50Ω to V_{DD} – 2.0 V
$\Delta V_{OUT(TX)}$	TX Output differential peak-to-peak voltage Swing	1200		2200	mVp-p	50Ω to V_{DD} – 2.0 V
ΔV_{IN}	RX and SI Receiver differential peak-to-peak Input Sensitivity	300	—	2600	mVp-p	V_{DD} = 3.30V, direct coupled, single ended drive, other input open

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Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD}) ..... -0.5V to +4V
PECL DC Input Voltage, (V_{INP}) ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage, (V_{INT}) ..... -0.5V to V_{DD} + 2.5V
TTL Output Voltage, (V_{OUTT}) ..... -0.5V to V_{DD} + 0.5V
TTL Output Current (I_{OUT}), (0V < V_{OUT} < V_{DD}) ..... +/-50mA
PECL Output Current, (I_{OUT}), (0V < V_{OUT} < V_{DD}) ..... -50mA
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to + 150°C
Maximum Input ESD (Human Body Model) ..... 1500 V

Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) ..... +3.3V ± 5%
Operating Temperature Range, (T) ..... 0°C Ambient to +110°C Case Temperature

Notes: (1) *CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*

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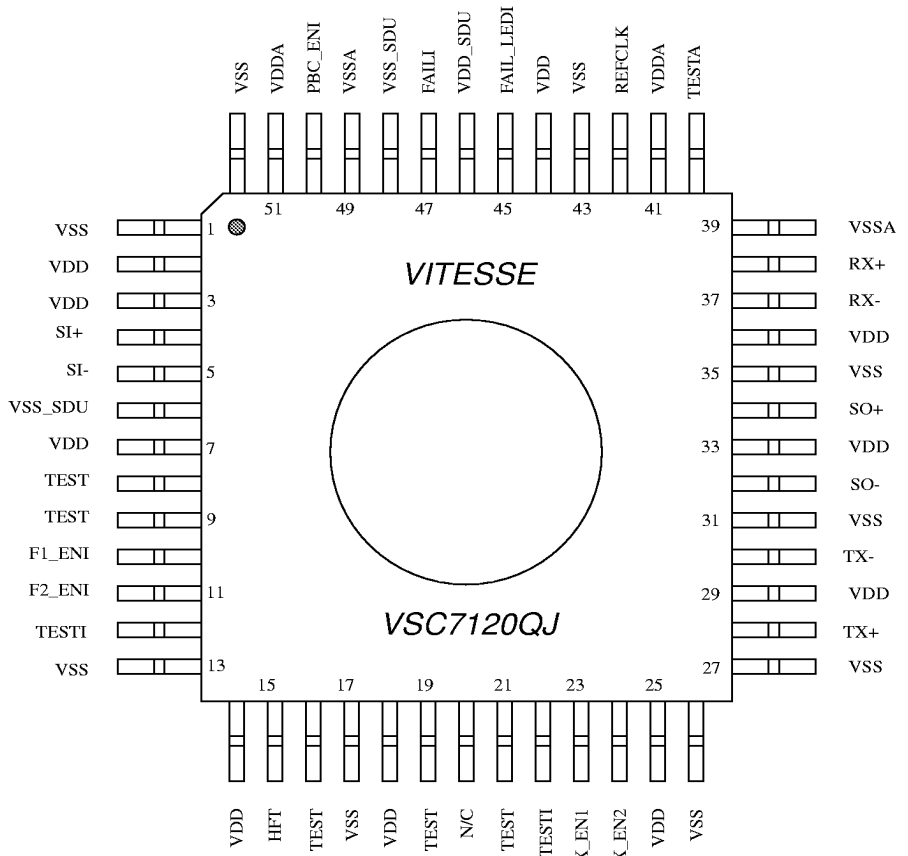
Package Pin Descriptions

Figure 8: Pin Diagram



Heat spreader is electrically connected to V_{SS}

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Table 1: Pin Identification

Pin #	*Name*	*Description*
4, 5	SI+ SI-	INPUT - Differential Serial Input to TX and to the Port Bypass Circuit.
38, 37	RX+ RX-	INPUT - Differential Serial Input to the Clock Recovery Unit.
34, 32	SO+ SO-	OUTPUT - Half Power Differential (AC coupling recommended) Port Bypass Circuit output. This re-timed RX data if PBC_ENI is HIGH or SI if PBC_ENI is LOW.
28, 30	TX+ TX-	OUTPUT - Full Power Differential (AC coupling recommended) Buffered SI if TX_EN1 or TX_EN2 is HIGH. If both are LOW then TX+ is HIGH, TX- is LOW.
42	REFCLK	INPUT - TTL Reference Clock for the PLL nominally at 106.25 MHz. Rising edge active.
10	F1_ENI	INPUT - TTL Enables the F1 Detector when LOW. F1 checks RX for Run Length violations.
11	F2_ENI	INPUT - TTL Enables the F2 Detector when LOW. F2 checks RX for the presence of K28.5 Characters.
50	PBC_ENI	INPUT - TTL Controls the Port Bypass Circuit. Steers SI to SO when LOW or Recovered RX to SO when HIGH.
15	HFT	INPUT - TTL High Frequency Timer which resets the fault detection circuits to a known state. The falling edge of HFT resets the F1 and F2 RS Registers. The FAILI and FAIL_LEDI signals must be strobed prior to resetting the fault detection registers.
47, 45	FAILI FAIL_LEDI	OUTPUT - TTL When LOW, these signals indicate that the F1 or F2 Fault Detectors have detected invalid Fibre Channel data at the RX inputs. Outputs from the F1 and F2 Fault Detectors are gated by F1_ENI and F2_ENI respectively. Two identical outputs provided for fanout purposes.
23, 24	TX_EN1, TX_EN2	INPUT - TTL Disables TX outputs when both TX_EN1 and TX_EN2 are LOW. TX_EN1 has a 20K pull-up resistor and TX_EN2 has a 20K pull-down resistor.
8, 9, 16, 19, 21, 12	TEST	INPUT - TTL Factory TEST Function when HIGH. Normal operating mode when LOW.
22	TESTI	INPUT - TTL Factory Test Function when LOW. Normal operating mode when HIGH.
1,13,17,26,27, 31,35,43,52	VSS	Ground
39,49	VSSA	Analog Ground for the CRU
6,48	VSS_SDU	Ground for SDU. Leave open during SDU power-down mode.
2,3,7,14,18,25, 29,33,36,44	VDD	+3.3V Power Supply
41,51	VDDA	Analog +3.3V Power Supply for the CRU
46	VDD_SDU	3.3V Power Supply for SDU. Leave open during SDU power-down mode
40	TESTA	Tie LOW with a pull down of 300 ohm.
20	N/C	User No Connect pin. Do not connect these pins.

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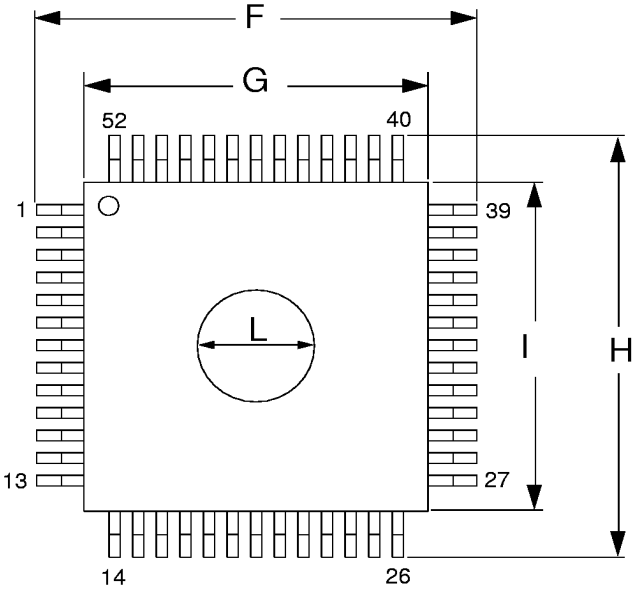
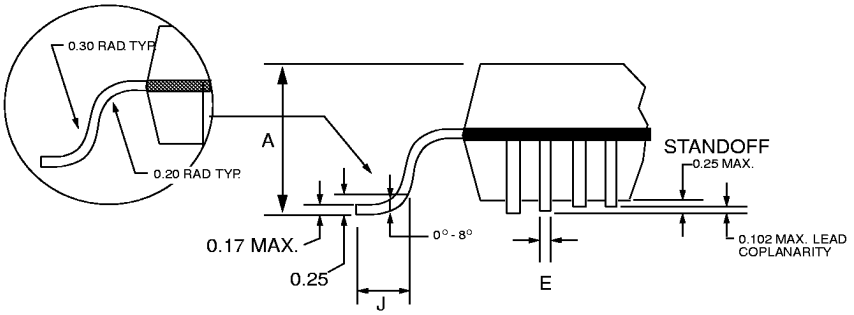
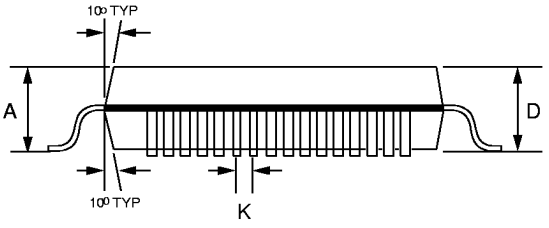
Package Information

52 (QJ) PQFP Package Drawing



Dims	*mm*	*Tol.*
A	2.45	MAX
D	2.00	+.15/-.10
E	0.30	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	+.15/-.10
K	0.65	BASIC
L	3.56	±.50 DIA





Notes:
Heat spreader up
All units in mm unless otherwise noted
Drawings not to scale.
Package Drawing #101-224-5 Issue #1

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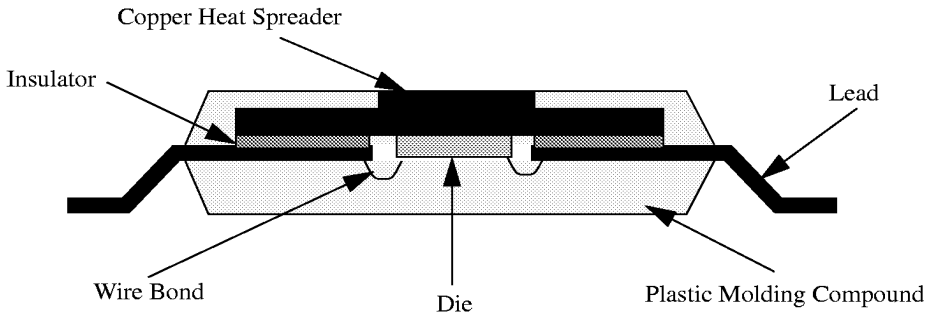
Package Thermal Characteristics

The VSC7120 is packaged into a thermally-enhanced plastic quad flatpack. This package adheres to the industry-standard EIAJ footprint for a 10x10mm body but has been enhanced to improve thermal dissipation with the inclusion of an exposed Copper Heat Spreader. The package construction is as shown in Figure 9.

Figure 9: Package Cross Section



The thermal resistance for the VSC7120 package is improved through low thermal resistance paths from the die to the exposed surface of the heat spreader and from the die to the leadframe through the heat spreader overlap of the leadframe.

Table 2: 52 Pin PQFP Thermal Resistance

Symbol	*Description*	*Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	2.5	°C/W
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads for a non-thermally saturated board.	37.0	°C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient in 100 LPFM air	31.0	°C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient in 200 LPFM air	28.0	°C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient in 400 LPFM air	24.0	°C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient in 600 LPFM air	22.0	°C/W

The VSC7120 is designed to operate at a maximum case temperature of up to 110 °C. The user must guarantee that the maximum case temperature specification is not violated. Given the thermal resistance of the package in still air, the user can operate the VSC7120 in still air if the ambient temperature does notexceed 52 °C in Hub Mode (52°C=110°C - 1.56W * 37 °C/W) or 65°C in Repeater Mode (65°C=110°C - 1.22W * 37°C/W) .

If operation above these ambient temperatures is required, then an appropriate heatsink must be used with the part or adequate airflow must be provided.

Moisture Sensitivity Level

This device is rated with a moisture sensitivity level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

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Ordering Information

The order number for this product is formed by a combination of the device number and package type as shown below:

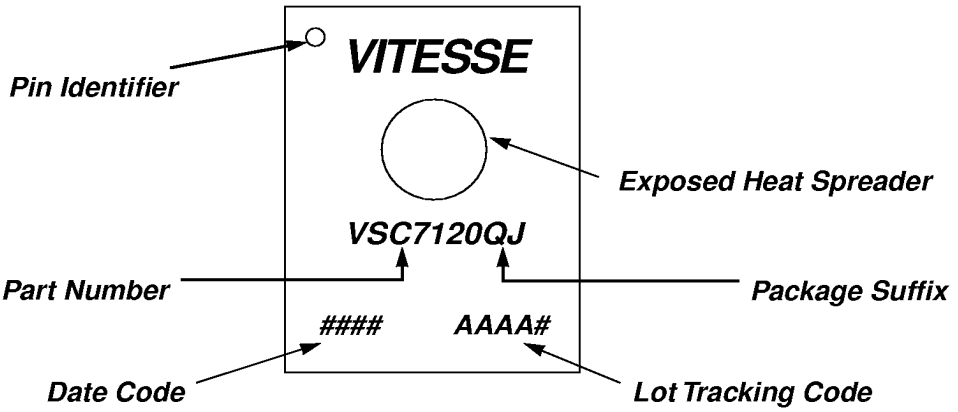
VSC7120 **QJ**

Device Type
VSC7120 - 1.0625 Gbits/sec Repeater

Package Type
QJ: 52 Pin Thermally Enhanced PQFP, 10mm Body

Marking Information

The package is marked with three lines of text as shown below (QJ Package):



Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products specifications or other information at any time without prior notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent of the appropriate Vitesse officer is prohibited.

741 Calle Plano, Camarillo, CA 93012 • 805/388-3700 • FAX: 805/987-5896