MULTIBUS II

LBX 2100 LBX II Reply Agent Address Error Generator

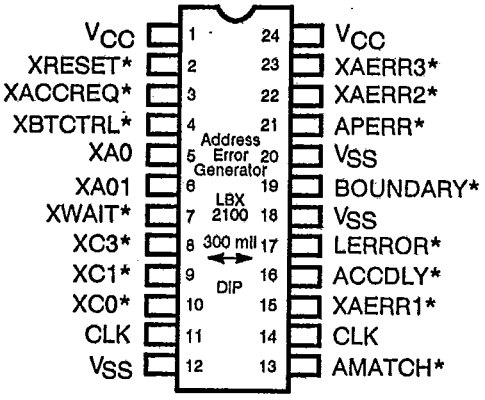
Distinctive Features

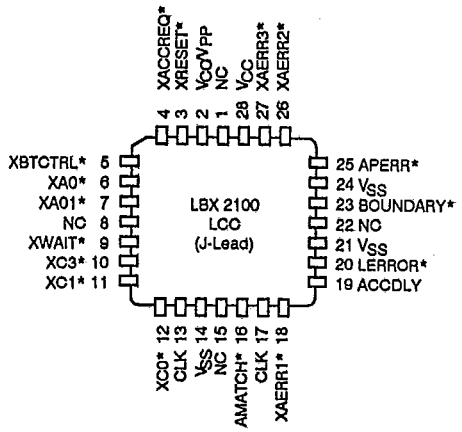
- Provides complete XAERR* (Address Error) signal generation including: alignment errors, width errors, transfer-not-understood errors, address portion bus errors, and continuation errors.
- Packaged in compact 300 mil 24 pin DIP or 28 pin J-lead LCC.
- Supports pipelined operations.
- Can be used separately or together with LBX 2000 to provide complete reply agent control interface to iLBX II bus.

Applications

- Bus Interface Circuitry for iLBX II reply agent modules such as I/O or memory devices.

Packages





LBX 2100 General Information

	Commercial (0°C to +70°C)
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic
High Drive Current Outputs (I_{OL})	To MBII spec (up to 64 mA, Open Collector or Three-state)

General Description

The LBX 2100 is a CMOS iLBX II reply agent address error generator packaged in a 300 mil 24 pin DIP or 28 pin J-lead LCC. The LBX 2100 provides complete reply agent address error generation and can drive the XAERR* signal directly (60 mA open collector). During specific cycles in a transaction the LBX 2100 will assert the XAERR* signal due to width errors, alignment errors, transfer-not-understood errors, address portion bus errors, and continuation errors. Other local errors can also be asserted to the LBX 2100 which will cause the XAERR* signal to be asserted.

The LBX 2100 conforms to the Rev C MULTIBUS II Bus Architecture Specification Handbook.

The LBX 2100 can also be used separately to generate the XAERR* signal for the reply agent module that does not use the LBX 2000 as the reply agent controller.

The LBX 2000 can be used in conjunction with the LBX 2100 where the 2100 is used to generate the XAERR* signal instead of the LBX 2000. In this manner, the two chip set provides a compact interface to the iLBX II bus.

Pin Descriptions

LBX 2100

Pin # LCC	Pin # DIP	Signal	I/O	Function
3	2	XRESET*	I	Active low; System bus reset.
4	3	XACCREQ*	I	Active low; Access request. Indicates valid address cycle on bus.
5	4	XBTCTRL*	I	Active low; Block transfer control. Indicates a block transfer cycle on bus.
6	5	XA0	I	Active high; Address bus bit 0.
7	6	XA01	I	Active high; Address bus bit 1.
9	7	XWAIT*	I	Active low; Wait state indicator.
10	8	XC3*	I	Active low; Command bit 3.
11	9	XC1*	I	Active low; Command bit 1.
12	10	XC0*	I	Active low; Command bit 0.
13	11	CLK	I	Inverted XBCLK*. Connect to pin 14 (DIP) or pin 17 (LCC).
14, 21, 24	12, 18, 20	VSS		Chip Ground
16	13	AMATCH*	O	Active low; Reply Agent match input. Indicates this module is being accessed.
17	14	CLK	I	Inverted XBCLK*. Connect to pin 11 (DIP) or pin 13 (LCC).
18	15	XAERR1*	O	Active low, 64 mA open collector; 0 WS address error output. Asserted if there is an address error during 0 WS accesses.
19	16	ACCDLY	O	Active high; Access delay. Indicates wait states during access.
20	17	LERROR*	O	Active low; Local errors. Used to indicates local address error (attempting to write to ROM).
23	19	BOUNDARY*	I	Active low; Address boundary exceeded. Indicates current transfer is over reply agent addressing limit for block transfers.
25	21	APERR*	O	Active low; Address parity error. Indicates parity error on address or command signals.
26	22	XAERR2*	O	Active low, 64 mA open collector; Non-0 WS address error output. Asserted if there is an address error during non-0 WS accesses.
27	23	XAERR3*	O	Active low, 64 mA open collector; Continuation error output. Asserted if there is a combination error during a block transfer.
2, 28	1, 24	VCC		+5V Chip Power
1, 8 15, 22	–	NC	–	No Connect