



512K x 8 Static RAM

Features

- **High speed**
— $t_{AA} = 15 \text{ ns}$
- **Low active power**
— 504 mW (max.)
- **Low CMOS standby power (Commercial L version)**
— 1.8 mW (max.)
- **2.0V Data Retention (660 μW at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**

Functional Description

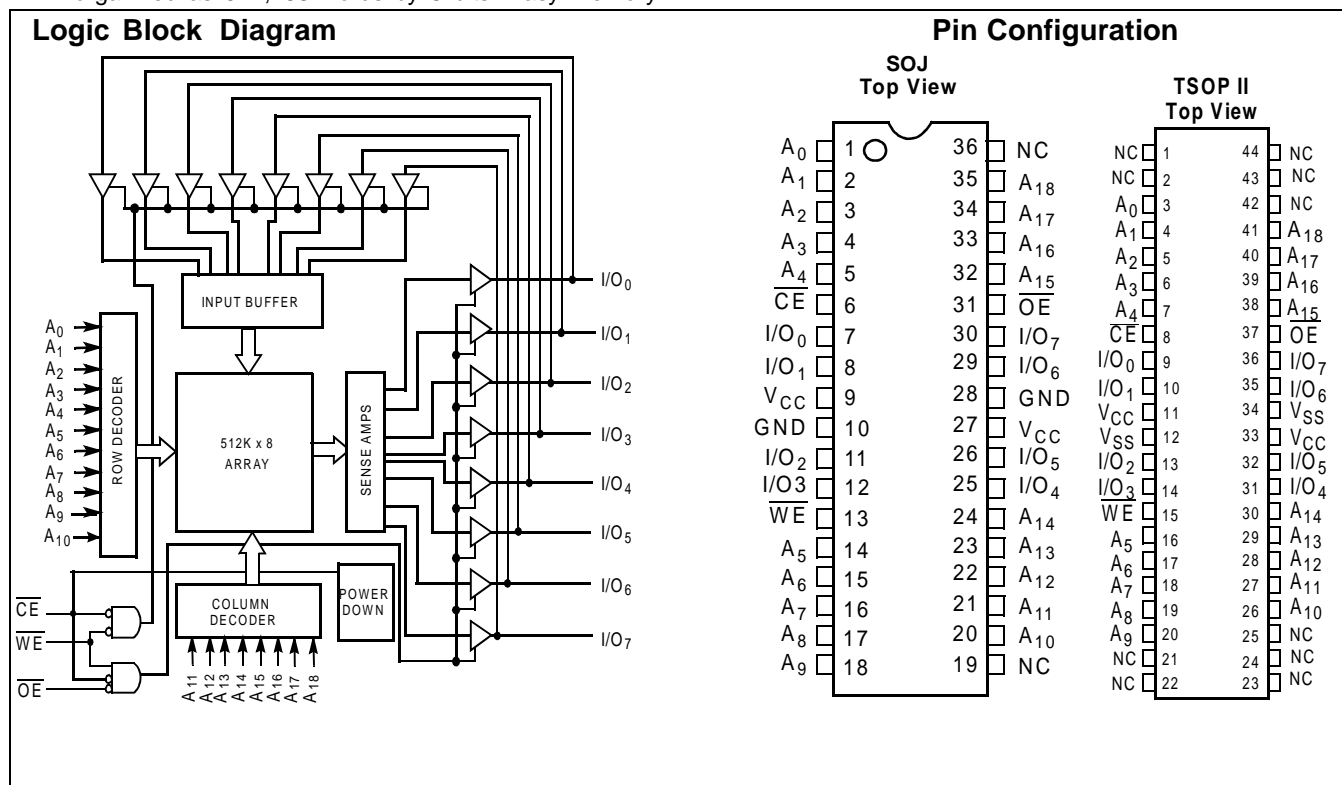
The CY7C1049BV33 is a high-performance CMOS Static RAM organized as 524,288 words by 8 bits. Easy memory

expansion is provided by an active LOW Chip Enable ($\overline{\text{CE}}$), an active LOW Output Enable ($\overline{\text{OE}}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing Write Enable ($\overline{\text{WE}}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

The CY7C1049BV33 is available in a standard 400-mil-wide 36-pin SOJ and 44-pin TSOPII packages with center power and ground (revolutionary) pinout.



Selection Guide

		-12	-15	-17	-20	-25
Maximum Access Time (ns)		12	15	17	20	25
Maximum Operating Current (mA)	Comm'l	200	180	170	160	150
	Ind'l	220	200	180	170	170
Maximum CMOS Standby Current (mA)	Com'l/Ind'l	8	8	8	8	8
	Com'l L	0.5	0.5	0.5	0.5	0.5

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with
Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to $+4.6\text{V}$

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5\text{V}$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5\text{V}$

Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$3.3\text{V} \pm 0.3\text{V}$
Industrial	-40°C to $+85^{\circ}\text{C}$	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-12		-15		-17		Unit	
				Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = −4.0 mA		2.4		2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA			0.4		0.4		0.4	V	
V _{IH}	Input HIGH Voltage			2.2	V _{CC} + 0.5	2.2	V _{CC} + 0.5	2.2	V _{CC} + 0.5	V	
V _{IL}	Input LOW Voltage ^[1]			−0.5	0.8	−0.5	0.8	−0.5	0.8	V	
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		−1	+1	−1	+1	−1	+1	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled		−1	+1	−1	+1	−1	+1	μA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., f = f _{MAX} = 1/t _{RC}	Comm'l		200		180		170	mA	
			Ind'l		220		200		180	mA	
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , $\overline{\text{CE}} \geq V_{IH}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}			30		30		30	mA	
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , $\overline{\text{CE}} \geq V_{CC} - 0.3\text{V}$, V _{IN} ≥ V _{CC} − 0.3V, or V _{IN} ≤ 0.3V, f = 0	Com'l/Ind'l			8		8		8	mA
			Com'l	L		0.5		0.5		0.5	mA

Notes:

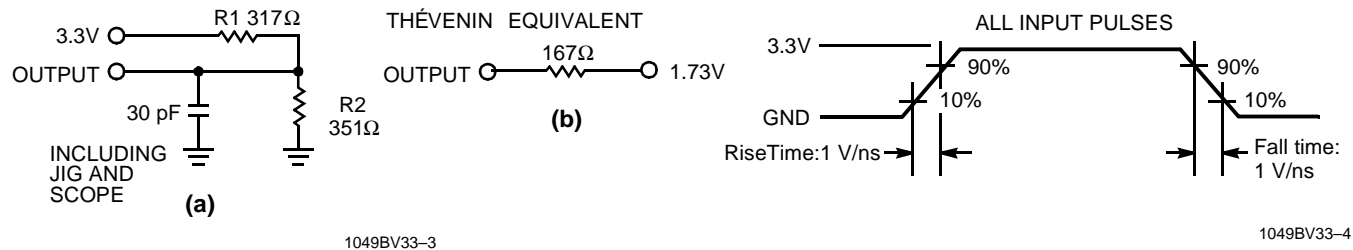
- $V_{IL}(\text{min.}) = -2.0\text{V}$ for pulse durations of less than 20 ns.
- T_A is the case temperature.

DC Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	-20		-25		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC},$ Output Disabled	-1	+1	-1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$	Com'l		160		mA
			Ind'l		170		mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}, \overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		30		30	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}, \overline{CE} \geq V_{CC} - 0.3\text{V},$ $V_{IN} \geq V_{CC} - 0.3\text{V},$ or $V_{IN} \leq 0.3\text{V}, f = 0$	Com'l/Ind'l		8		mA
			Com'l L		0.5		mA

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = 3.3\text{V}$	8	pF
C_{OUT}	I/O Capacitance		8	pF

AC Test Loads and Waveforms

Note:

- Tested initially and after any design or process changes that may affect these parameters.

AC Switching Characteristics^[4] Over the Operating Range

Parameter	Description	-12		-15		-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{power}	V _{CC} (typical) to the First Access ^[5]	1		1		1		μs
t _{RC}	Read Cycle Time	12		15		17		ns
t _{AA}	Address to Data Valid		12		15		17	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		12		15		17	ns
t _{DOE}	\overline{OE} LOW to Data Valid		6		7		8	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		6		7		8	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[7]	3		3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		6		7		8	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		12		15		17	ns
WRITE CYCLE ^[8, 9]								
t _{WC}	Write Cycle Time	12		15		17		ns
t _{SCE}	\overline{CE} LOW to Write End	10		12		13		ns
t _{AW}	Address Set-Up to Write End	10		12		13		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	10		12		13		ns
t _{SD}	Data Set-Up to Write End	7		8		9		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3		3		3		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		6		7		8	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally. t_{power} time has to be provided initially before a read/write operation is started.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

AC Switching Characteristics^[4] Over the Operating Range (continued)

Parameter	Description	-20		-25		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{power}	V _{CC} (typical) to the First Access ^[6]	1		1		μs
t _{RC}	Read Cycle Time	20		25		ns
t _{AA}	Address to Data Valid		20		25	ns
t _{OHA}	Data Hold from Address Change	3		3		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		20		25	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		8		10	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0		0		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[6, 7]		8		10	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[7]	3		3		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[6, 7]		8		10	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		20		25	ns
WRITE CYCLE ^[9]						
t _{WC}	Write Cycle Time	20		25		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	13		15		ns
t _{AW}	Address Set-Up to Write End	13		15		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	13		15		ns
t _{SD}	Data Set-Up to Write End	9		10		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[7]	3		3		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[6, 7]		8		10	ns

Data Retention Characteristics Over the Operating Range (For L version only)

Parameter	Description	Conditions ^[10]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{\text{CC}} = V_{\text{DR}} = 2.0\text{V}$, $\overline{\text{CE}} \geq V_{\text{CC}} - 0.3\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.3\text{V}$ or $V_{\text{IN}} \leq 0.3\text{V}$		330	μA
$t_{\text{CDR}}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_{\text{R}}^{[11]}$	Operation Recovery Time		t_{RC}		ns

Notes:

10. No input may exceed $V_{\text{CC}} + 0.5\text{V}$

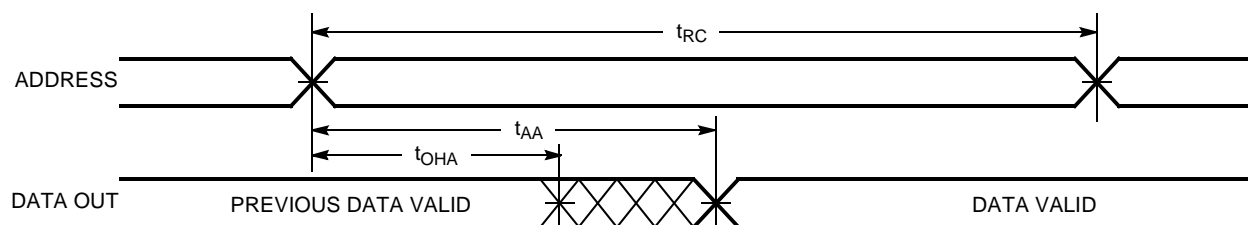
11. $t_{\text{r}} \leq 3\text{ ns}$ for the -12 and -15 speeds. $t_{\text{r}} \leq 5\text{ ns}$ for the -20 ns and slower speeds.



The diagram shows two signals over time: V_{CC} and \overline{CE} . The V_{CC} signal starts at 3.0V, then drops to a level where $V_{DR} \geq 2V$, and then returns to 3.0V. This period is labeled "DATA RETENTION MODE". The \overline{CE} signal is shown as a low pulse. The duration of the low pulse is labeled t_{CDR} . The time from the start of the \overline{CE} pulse to the start of the V_{CC} drop is labeled t_{CDR} . The time from the end of the V_{CC} drop to the end of the \overline{CE} pulse is labeled t_R .

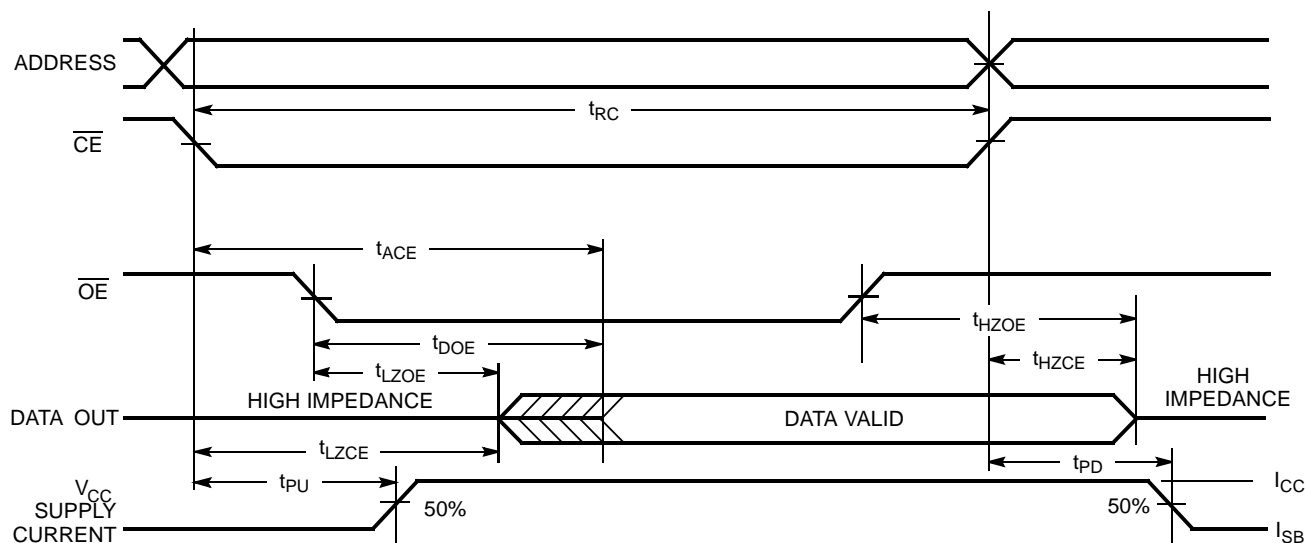
1049BV33-5

Read Cycle No. 1^[12, 13]



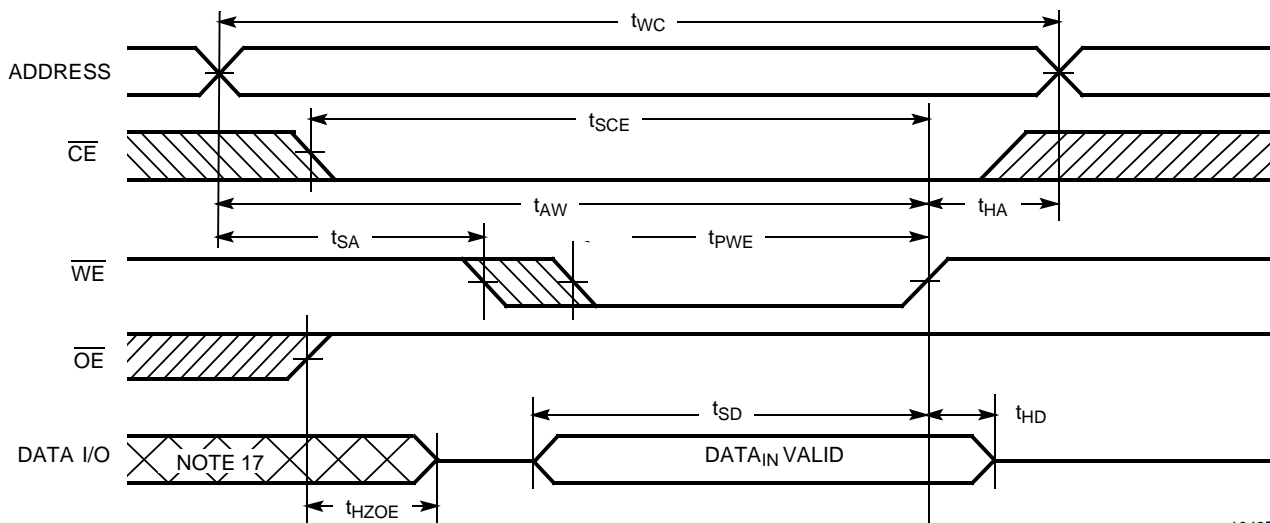
1049BV33-6

Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)^[13, 14]

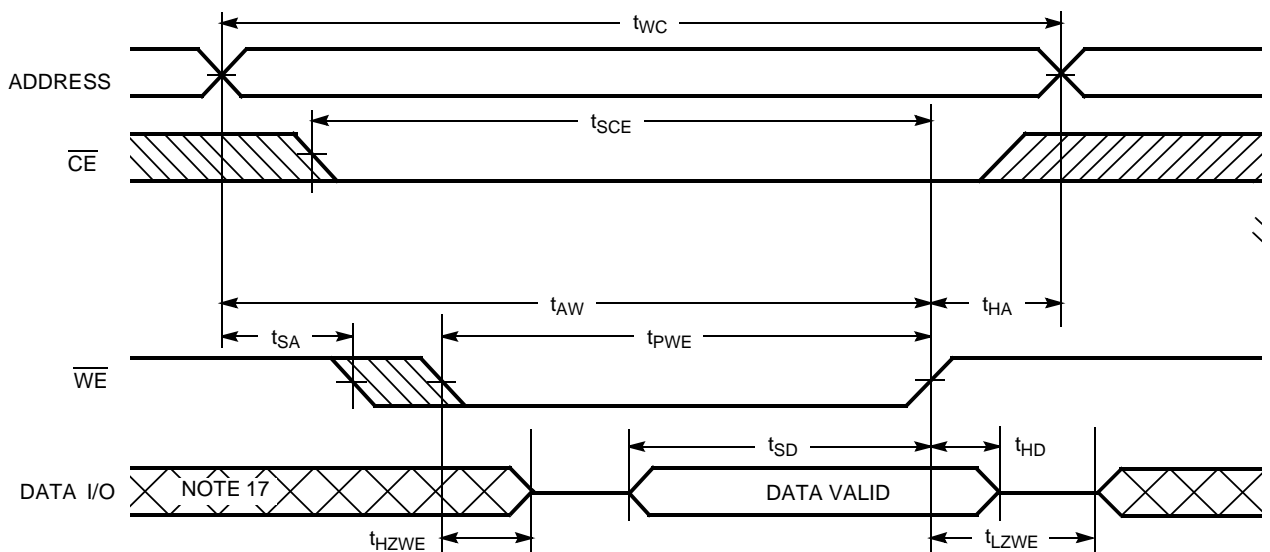


1049BV33-7

12. Device is continuously selected. $\overline{\text{OE}}, \overline{\text{CE}} = \text{V}_{\text{IL}}$.
13. $\overline{\text{WE}}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[15, 16]


1049BV33-8

Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW)^[16]


1049BV33-9

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ – I/O ₇	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Notes:

15. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.

16. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

17. During this period the I/Os are in the output state and input signals should not be applied.

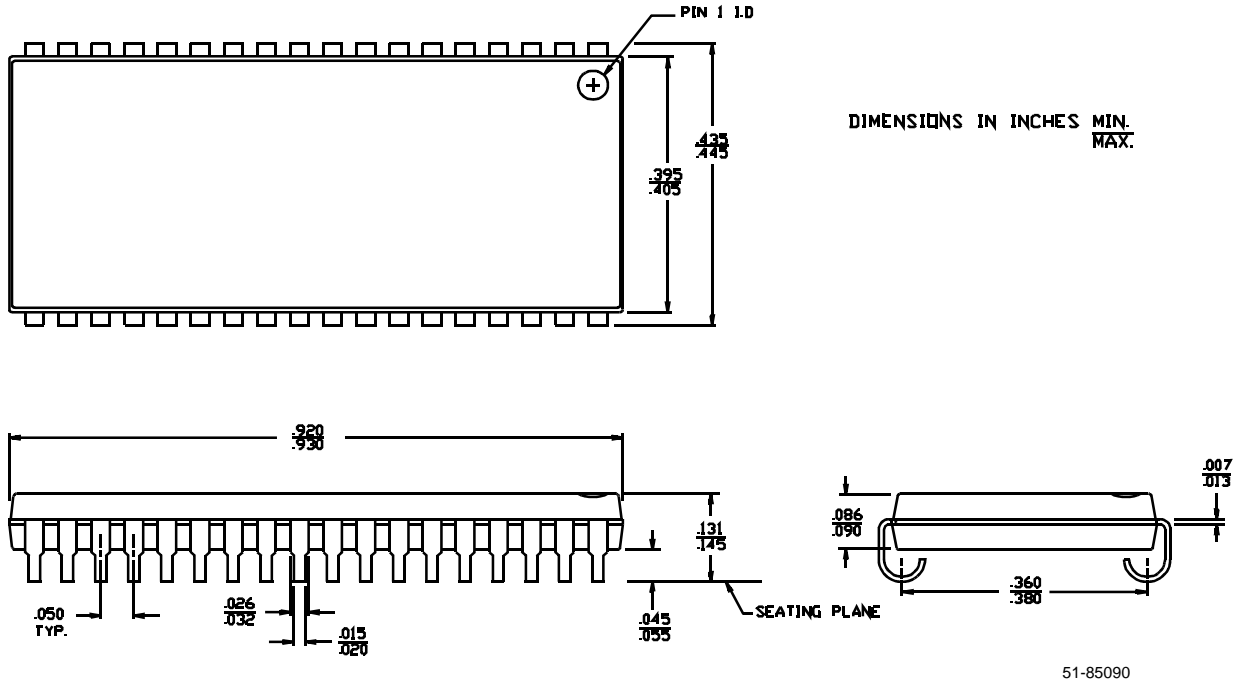
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1049BV33-12VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BV33-12ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33L-12VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-12VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
15	CY7C1049BV33-15VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BV33L-15VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-15ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33L-15ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33-15VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BV33-15ZI	Z44	44-Pin TSOP II Z44	
17	CY7C1049BV33-17VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BV33L-17VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-17ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33L-17ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33-17VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BV33L-17VI	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-17ZI	Z44	44-Pin TSOP II Z44	
20	CY7C1049BV33-20VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BV33L-20VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-20ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33L-20ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33-20VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BV33-20ZI	Z44	44-Pin TSOP II Z44	
25	CY7C1049BV33-25VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BV33L-25VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-25ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33L-25ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33-25VI	v36	36-Lead (400-Mil) Molded SOJ	Industrial

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Packaging Diagrams

36-Lead (400-Mil) Molded SOJ V36



44-Pin TSOP II Z44

DIMENSION IN MM (INCH)
MAX
MIN.

